Performance Analysis of Gate Driver Circuit for TFT – LCD
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Abstract
This paper presents Performance Analysis of Gate Driver Circuit for TFT-LCD. The output voltage of proposed Gate Driver circuit can be estimated as 40V by using Cadence, Microwind simulators. Measurement results indicate that better frequency response with reduced capacitive coupling effect by which driving speed of the gate driver circuit is improved.

Keywords: Gate driver circuit, capacitive coupling, TFT Switch.

I. Introduction
In past history of display technology having wide range like PMLCD, AMOLED, FPD, etc. but the AMLCD panels are widely used because of low cost, better uniform coverage, addressing and high driving capability [5]-[13]. Recently for getting better results display technology is used gate driver circuit. The conventional gate driver consists three major blocks inside it Shift register block, Level shifter block, Output Buffer block [8].

II. Proposed Circuit Operation
As shown in fig.2 three clocks are used two extended clock and one driving clock. Input is applied at out N-1, and output is calculated from out N port. This output voltage turns on TFT switches and charge the capacitor by which row lines are drive in the form of row by row succession[7]-[8], next row will receive input voltage from first row through discharging the capacitor [13].

Fig.3 shows schematic diagram, timing diagram, and layout diagram of the proposed gate driver circuit. Each stage of gate driver circuit consists of three types of clock signals (one driving clock, two extended clock), one pull-up network (N9, N4), one key pull-down network (N10, N11) and two alternative pull-down network (N8-N5 and N0-N3). Concept of gate driver is clear through circuit operation. The input signal is applied at Out (N-1) it starts circuit. Here charging and discharging of Out (N) node is controlled by Qn node. So Nth row line is received high voltage signal through Out (N) node, at this time Out (N-1) is discharged which enables next stage gate driver circuit.

On the basis of reference work capacitive coupling effect and output fluctuation is a severor problem due to charge trapping in a gate insulator at high gate voltage. To overcome this problem an AC driving method is used [8]-[10]. Alternative pull down network are used with gate capacitive coupling [2]-[10]. The driving speed can be improved by changing clk signal. The three main working steps are described below.
As in step1, when high voltage input is applied at Out \( N-1 \) node, the \( Q_N \) node becomes high and it turns on N7, N1. At this time Out \( N \) node becomes low through N4 because clk signal is low but the N7, N1 are turn on and they provide discharging path for N8,N0 to Vss through An, Bn node [13]-[14]. Due to this gate driver becomes free from any internal voltage which creates defects in output signal and output signal shows 40v swing without any fluctuation.

There is no high voltage available for N6, N5, N2, and N3, are then turned off. In the next step clk signal becomes high which boosted up \( Q_N \) node \((V_H+\Delta V)\) due to gate capacitor coupling of N4, which enhance the driving capability of N4. Therefore, row lines receive high voltage \( V_H \) through out\( N \) node. In the next step Out \( N+1 \) node becomes high and N10, N11 are turn on and discharge \( Q_N \) and Out\( N \) nodes at Vss [8],[14].

Notably, while EXCK is still \( V_H \) and ECK is still \( V_L \) as in step 1, it turns on N2, N3 by which \( Q_N \) and Out\( N \) nodes are maintain at Vss. Meanwhile reversed-bias stress in source nodes of N6, N5. Which receives a high voltage supply from the EXCK signal, facilitates recovery of \( \Delta V_{TH} \). Here ECK and EXCK signal suppress the excessive switching times of clock signals [14]. Therefore proposed gate driver circuit avoids the fluctuation in output waveform, and improves driving speed of the circuit.

### Table 1

<table>
<thead>
<tr>
<th>Sr.No.</th>
<th>Design Parameter</th>
<th>Reference Results</th>
<th>Proposed Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Design Technology</td>
<td>0.6µ</td>
<td>0.35µ</td>
</tr>
<tr>
<td>2.</td>
<td>Ton Time</td>
<td>50 µSec</td>
<td>25 µSec</td>
</tr>
<tr>
<td>3.</td>
<td>Duty Cycle</td>
<td>50%</td>
<td>33%</td>
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<td>4.</td>
<td>Test Temperature</td>
<td>120°C</td>
<td>135°C</td>
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<tr>
<td>5.</td>
<td>Output Voltage Swing</td>
<td>39.2 V</td>
<td>40 V</td>
</tr>
<tr>
<td>6.</td>
<td>Capacitive coupling</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>7.</td>
<td>Output Fluctuation</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

### III. Results and Discussions

Fig.3 shows schematic diagram and layout diagram of proposed gate driver circuit. It uses 12 TFTs and one R-C loading. The result of proposed gate driver verified through cadence and Microwind simulator.
Fig. 4 (b) shows the output voltage exactly follows applied input signal and there is no fluctuation. Moreover, according to fig. 5(a) and fig. 5(b) internal capacitive effects are removed from output this is possible via adopting reverse biased method with two extended clock. As mentioned above circuit operation internal capacitive voltage is maintained at Vss through alternative pull-down network and the switching of pull-down network is controlled by extended clocks [14]. As shown in figures output of gate driver plot between voltage (v) and time (μsec.) i.e. time is being calculated in microsecond which indicate the driving speed of the gate driver is just double in comparison to reference work via changing the clock frequency. Circuit operates stably at 135°C temperature. The improvements of proposed circuit are compared with previous work listed in table.1.

IV.Conclusion
This paper presents high speed gate driver circuit with no internal capacitive coupling effect due to this output voltage follows its input voltage. Proposed gate driver gives uniform output without fluctuation for large TFT-LCD, via using reverse biased method with change in clock frequency signal.

Acknowledgement
The author would like to thank Mr. Abhishek N. Tripathi, Assistant Professor (EC) of Bansal Institute of Science & Technology Bhopal. I also thankful Mr. K.K. Nayak HOD (EC), Mr. Manish Saxena M.Tech. The blessing of god, Teacher’s and my friends is the main cause behind the successful completion of this paper. I wish to acknowledge
great moral support given by management of Bansal Institute of Science and Technology, Bhopal.

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