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Wide Tuning Range with High-Q Active Inductor using Differential Active Inductor Based on Weak Inversion Transistors

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Abstract **- This paper presents a novel 2-port high-Q differential active inductor (DAI) in weak inversion(WI). The proposed 2-port differential active inductor consists of the differentials amplifier and source common amplifier. The novelty of the proposed structure can improve its Q-factor due to decrease of the Parasitic capacitances, series resistance and extend high power dissipation is in strong inversion except low in weak inversion. For an experimental validation, the 2- port differential active inductor DAI(WI) was fabricated within 130 nm BSIM3V3 CMOS technology. The fabricated circuit in weak inversion (designI) shows inductance L in the neighborhood of value18.01H and quality factor Q to the value approach 1.235E03 in the frequency range of 1.599KHz to 2.519 MHz but for circuit in weak inversion(designII) product inductance L in the neighborhood of value 0.1721H and quality factor Q to the value approach 26.07 in the frequency range of 1.599KHz to 59.589 KHz.**

Keywords: Circuit Simulation , Sub-Threshold Region, Differential Active Inductor DAI.

I. INTRODUCTION

Motivated by the growing market of wireless communications system, instrumentations and optical communications much effort have been devoted to the implementation of components in CMOS technology.

The broadband amplifier is the demanding block in broadband telecommunication system. The specifications of broadband amplifier must be satisfied simultaneously including, wide bandwidth, large power gain, good impedance matching, good linearity, low power consumption and low cost.

The tremendous improvement in the performance of the MOSFETs has enabled the RF applications [1]. Therefore, the RFCMOS technologies have been the technology of choice among the design engineers for designing circuits and systems for wireless applications [1-3]. The demands for cellular transceivers, transceivers for personal area communications, chips for UHF Radio frequency identification tag, Bluetooth transceivers, ZigBee transceivers etc. are increasing day by day. Most of the components like low noise amplifier, mixer, voltage controlled oscillator, active filter, power amplifier, RF band filter, that are being used in these transceivers need inductors that takes a large area in the chip. The main purpose of designing the active inductor is to reduce the area of the inductor compared to the passive inductor while maintaining reasonable quality factor of the device. Moreover, the poor performance of the passive inductors (spiral inductor) in the CMOS technologies is due to the poor quality factor. The quality factor of the spiral inductors on silicon substrate can be in the range of 3~10 using multilevel spirals [4]. The main advantage of the active inductor is improved quality factor, reduced chip area and tuned characteristics compared to the passive inductor which can be used in the RF circuits. However the power consumption and the operating frequency range have been the major shortcomings of active inductor which is reported in [5].The efforts are on to substitute the passive inductor using active inductor [6-8].Recently for broadband RF and Microwave applications, a new architecture for active inductor is proposed in [9]. The inductor less architecture has been studied in [10] for multistandard radio applications that uses active inductor design methodology. For multi standard wirelineSerDes applications, the differential active inductor was reported in [11].

This paper is organized as follows. Section II discusses about basic floating gyrator– C the proposed active inductor in weak inversion followed by simulation results using simulation study in [12] that is discussed in section III and conclusion is presented in section IV.

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II. DESIGN OF ACTIVE INDUCTOR

In this work, the designs of active inductor are studied which is based on using gyrator-C topology[13]as shown in Fig . 1.

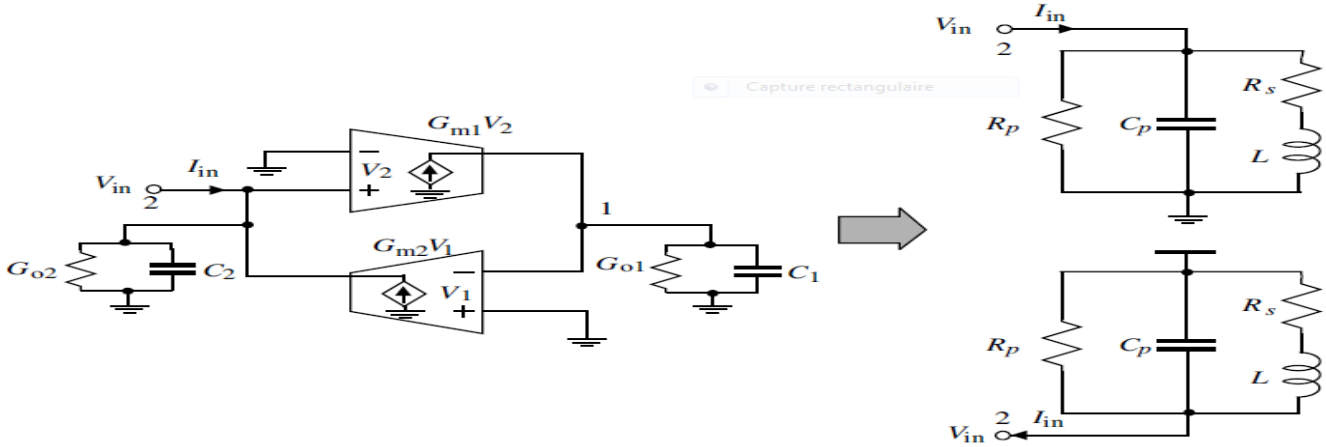

Fig. 1.Lossy gyrator-C Active Inductor Model and Equivalent [13]

The admittance looking into port 2 of the gyrator-C network is obtained from,

$$Y_{in} = sC_p + Y_p + \frac{1}{R_S + sL_S} \quad (1)$$

Eq.3 can be represented by the RLC networks shown in Fig.1

We comments on the preceding results :

■When the input and output conductances of the transconductors are considered, the gyrator-C network behaves as a lossy inductor. Rp should be maximized while Rs should be minimized to low the ohmic loss. The finite input and output impedances of the transconductors of the gyrator-C network, however, have no effect on the inductance of the active inductor.

$$Z_{in} = \frac{{}^{R_S}/_{C_pL_S} + {}^{s}/_{C_p}}{s^2 + s\frac{(C_pR_S + Y_pL_S)}{C_pL_S} + \frac{(Y_pR_S+1)}{C_pL_S}} = \frac{1}{Y_{in}} \text{ is impedance} \quad (2)$$

$$\omega_0 = \sqrt{\frac{(Y_pR_S+1)}{C_pL_S}}; \quad \omega_0 = f_{sr} * 2\pi = \frac{1}{\sqrt{LC}} \quad \text{with } f_{sr} \text{ self-resonant frequency} \quad (3)$$

$$\frac{\omega_0}{Q} = \frac{(C_pR_S + Y_pL_S)}{C_pL_S}. \quad (4)$$

$$Q = \frac{C_pL_S}{C_pR_S + Y_pL_S} \times \sqrt{\frac{(Y_pR_S+1)}{C_pL_S}}; \quad \text{is Quality factor (Q-factor)} \quad (5)$$

$$\omega_z = {}^{R_S}/_{L_S} \quad (6)$$

Where, L is inductance, Cp is parallel capacitance and Rs, Rp are series and parallel resistance respectively of gyrator-C equivalent model. When Rp>>Rs, the quality factor can be expressed as

$$Q = \frac{Rp}{\omega_0 L_p} \quad (7)$$

When Rs>>Rp, the quality factor can be expressed as

$$Q = \frac{\omega_0 L_S}{R_S} \quad (8)$$

$$L = \frac{C1}{Gm1Gm2} \quad (9)$$

From the expression it can be noted that the series resistance should be decreased and parallel resistance should be increased for a given value of inductance to get a good quality factor. Also, inductance value can be tuned by either changing the load capacitance (C1) or by varying the transconductance values of the transconductors (Gm1, Gm2) constituting the active inductors. A varactor will be required in the circuit to vary the capacitance value. Since varactor is a non-linear element, it degrades the linearity of the inductor at a large extent. So, changing the transconductance of the transconductors is the good choice to tune inductance value.

The kind and making principle of both designs are given below. was fabricated within 130 nm BSIM3V3 CMOS technologywas used to simulate the two designs and the results obtained from the simulation are analyzed. The transistors were biased into Weak Inversion (WI):for having low trans-conductance values.

Small signal analysis was carried out on the designs to obtain the impedance values. The impedance of the designs is studied and optimized for inductance values at 2.34 MHz frequency.

A. Active Inductor Design I in Weak Inversion (WI):

The MOS Transistor in Weak Inversion (WI):

In this section we will explore the behavior of the MOS transistor in the subthreshold regime where the channel in weakly inverted. This will allow us to model transistors operating with small gate voltages, where the strong inversion model erroneously predicts zero current. The expression (17) for drain current in a subthreshold MOSFET [14]:

*Drain current I_D: $I_D = I_{D_0} * \frac{W}{L} * \exp^{\left(\frac{V_{gs}}{nV_t}\right)}\left(1 - \exp^{\left(\frac{-V_{ds}}{V_t}\right)}\right)$ (10)

With $V_t = \frac{k*T}{q} \cong 26mV$ at T=300K ,

$n = \frac{C_{ox}+C_{dep}}{C_{ox}} \cong 1.5$ (11)

And $I_{D_0} = \mu_n * C_{ox}(n-1) * V_t^2 * \exp^{\left(\frac{-V_{TH}}{nV_t}\right)}$ (12)

Note: channel length modulation, i.e., λ is ignored here

The schematic of active inductor is shown in Fig. 2.

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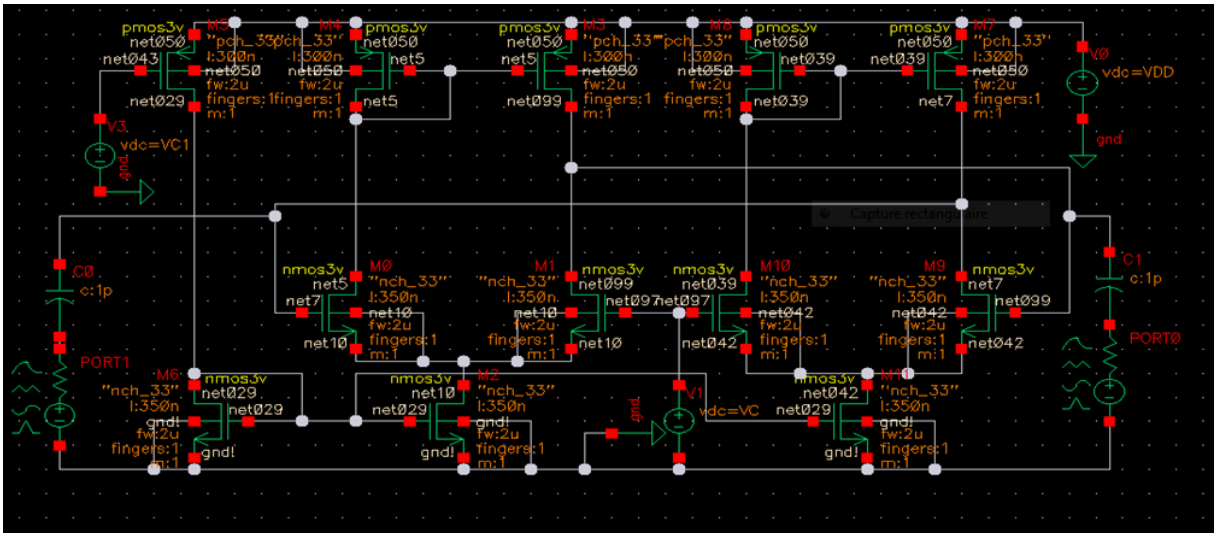

Fig. 2. Circuit schematic of Active inductor I in Sub-threshold region.

In this design differential amplifier, is used as a basic transconductor unit. So, here two differential amplifiers are connected in negative feedback configuration. The advantage of using differential amplifiers is that it eliminates the effect of noise present in the circuit which is a sensitive parameter for RF circuit applications. This design converts parasitic capacitances of M1, M3 and M9 to an equivalent inductance. M5 and M6 generate reference current so that all the transistors work in Sub-threshold region. Changing the value of reference current changes the performance of the circuit. M2 and M11 are acting as current source which are biased using M5 and M6. The value of Vdd and gnd are +3.3 V and 0.V respectively.

B. Active Inductor Design II in Sub-threshold region:

The schematic of active inductor is shown in Fig. 3. In this design a differential amplifier and a common source amplifier are connected in negative feedback configuration. This design converts parasitic capacitances of M1, M3 and M8 to an equivalent inductance. M5 and M6 generate reference current to bias M2, where M2 is a current source. In order to worse the performance of the inductor ,self-resonant frequency is increased and series equivalent resistance value is decreased.

and this is done by replacing one of the differential amplifiers by common source amplifier. M7 plays significant role to improve the quality factor of the active inductor. Also, the number of MOSFETs used in design II are less as compared to design I which makes design II more optimized in terms of space. In this design, the value of Vdd and gnd are kept same as in design I.

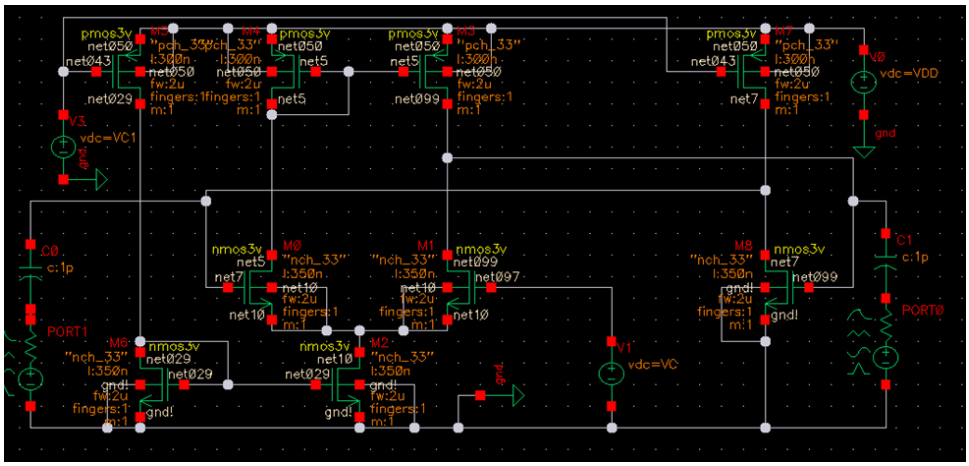

Fig.3. Circuit schematic of Active inductor II in Sub-threshold region.

III. RESULTS AND DISCUSSION

The performance of the active inductors shown in Fig.2 and Fig.3 have been analyzed by using simulation in Cadence spectre simulator. 130 nm CMOS technology from tsmc13rf foundry was used for the MOSFETs. The results of the circuits of design I and design II are obtained and compared. The aspect ratio for our designs is listed in table I. The reference current value for our design I and design II is kept at 100.73nA to 731nA. Total power dissipation drawn by design II and design I are 931.32nW to 6.6uW and 890.518nW to 6.088uW respectively, due to which design I is more optimized than design II in term of power consumption.

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Table 1 device size of the proposed ACTIVE INDUCTOR DESIGN in Sub-threshold region .

Transistors	size(um/um)	Fingers
M0 M1	2 /0.35	1
M2	2 /0.35	1
M4 M5 M3	0.3/0.35	1
M6	2/0.35	1
M7 M8	0.3/0.35	1
M9 M10 M11	2/0.35	1

From the simulation study, the parameters such as input impedance, bandwidth, inductance and quality factor are analysed. For the active inductor shown in Fig. 2 (design I), the input impedance value is obtained and the result is shown in Fig. 4.

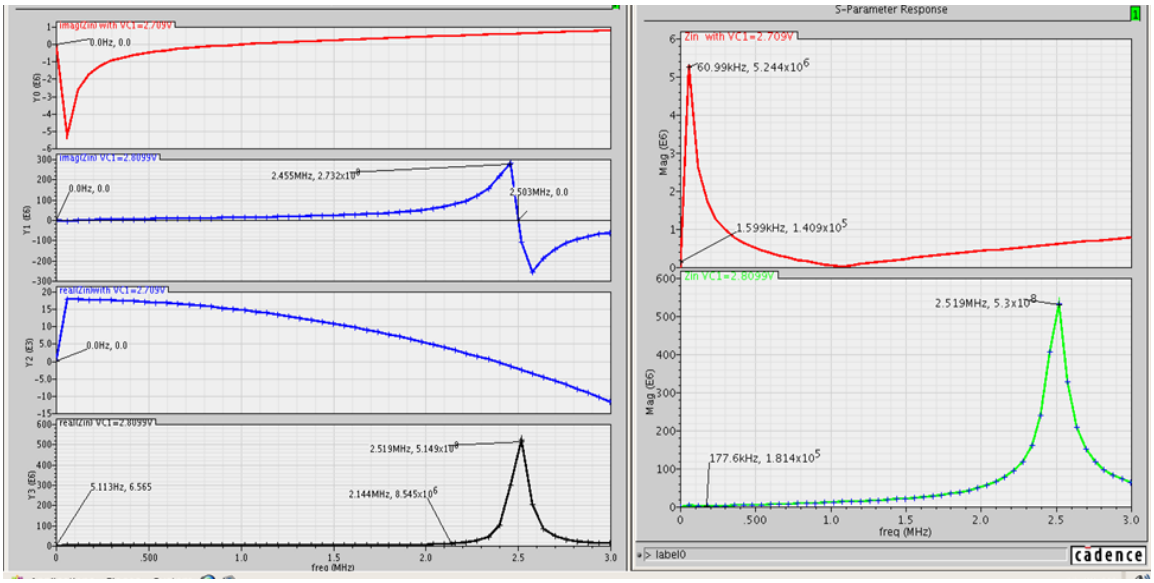

Fig. 4.Input impedance of Active inductor I in Sub-threshold region for VC1 varies of the 2.709V to 2.8099V.

From the results it has been observed that the operating frequency range of the active inductor is 1.599KHz to 2.519 MHz. The results suggest that the maximum quality factor can be achieved is 1.235E03 at 2.34MHz frequency.The range of the inductance value is from 0.01854H to 18.01H.

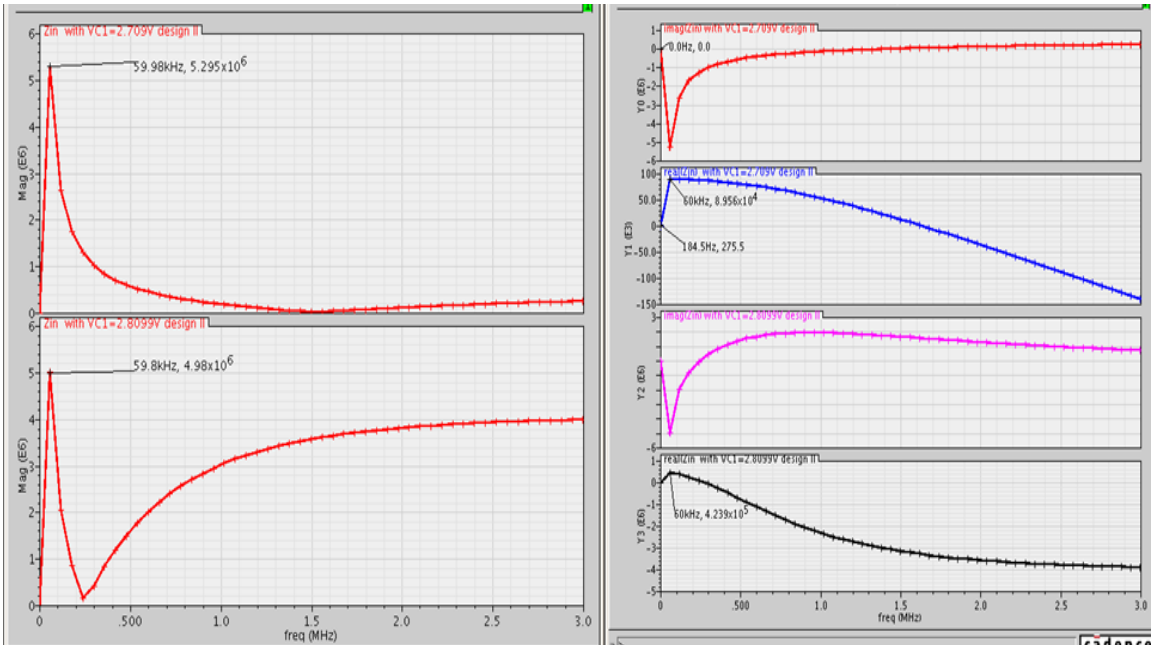

Fig. 5.Input impedance of Active inductor II in Sub-threshold region forVC1 varies of the 2.709V to 2.8099V.

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The active inductor shown in Fig. 3 (design II), is simulate using the same technology used for the design I. The simulation result for the input impedance of the active inductor is shown in Fig.5.The simulation results suggest that the operating frequency range of the active inductor can be from 1.599KHz to 59.589 KHz. The quality factor is obtained from the simulations and a maximum quality factor of 26.07 can be achieved at 1.62 MHz frequency. The range of the inductance value can be from 0.1nH to 0.1721H. From the simulation results it has been observed that the increase in value of quality factor decreases bandwidth which is also discussed in [15].

The self-resonant frequency of design I and design II are 59.589 KHz and 2.519 MHz respectively which is far from the operating frequency range.Based on the simulation result the quality factor and inductance of design I and design II are compared and plotted in Fig. 6 and Fig. 7respectively.Table II summarizes the performance of the active inductors with the results obtained in the literature [5, 16 and 17].

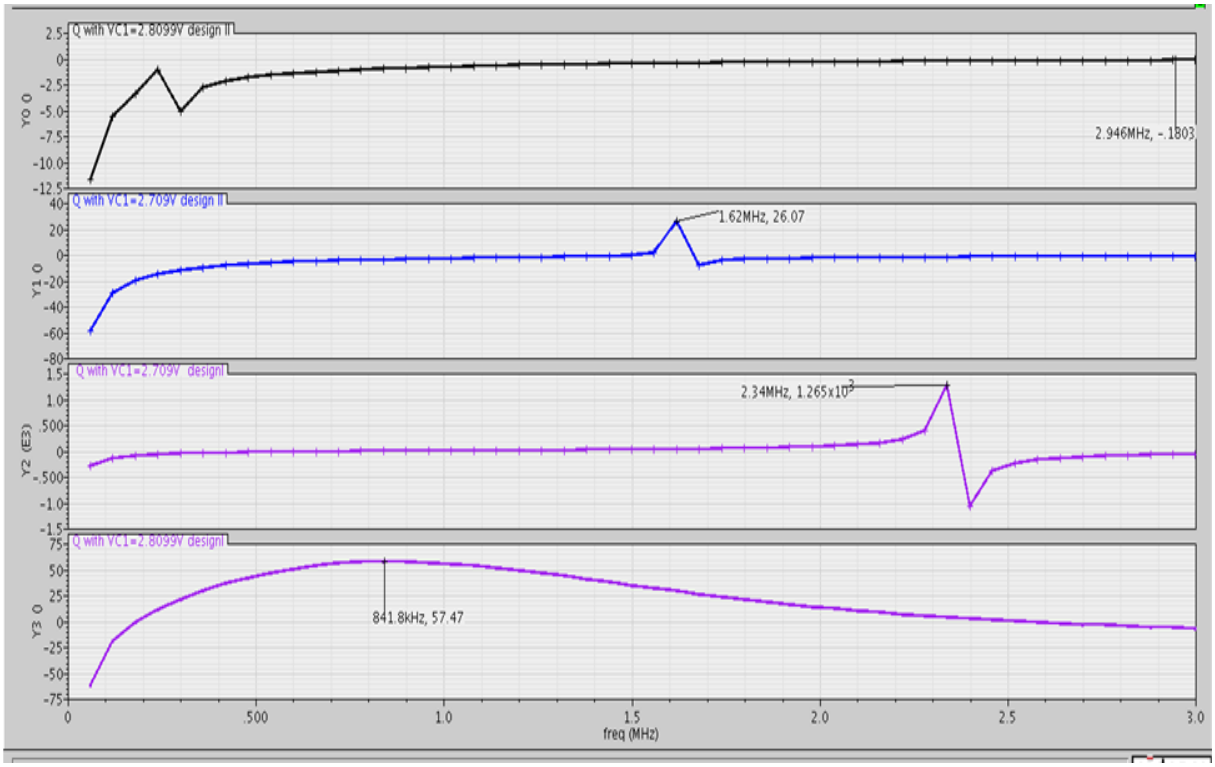

Fig. 6. Quality factor of Active inductors in Sub-threshold region forVC1 varies of the 2.709V to 2.8099V.

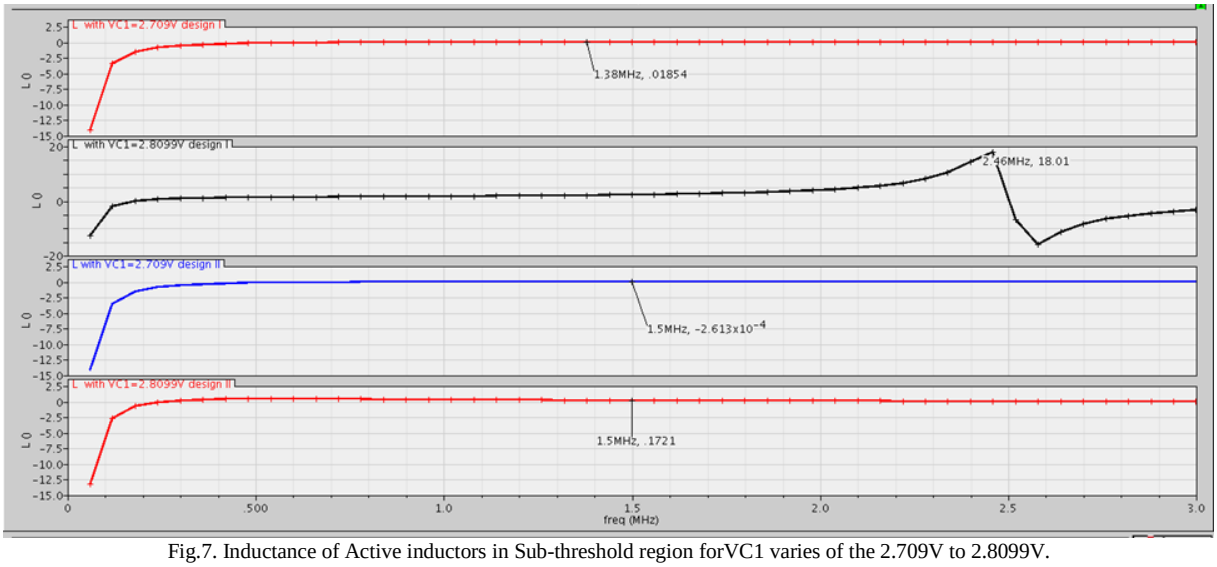

Fig.7. Inductance of Active inductors in Sub-threshold region forVC1 varies of the 2.709V to 2.8099V.

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Table 3 summarized performances of this DAI (WI) and its comparison with previously published data

Items\Ref.	[5]	[16]	[17]	This work	
				Design I	Design II
Technology (nm)	180	90	200	130	130
Inductive Bandwidth	0.1 GHz - 3.1 GHz	0.6 GHz –3.8 GHz	NA	1.599KHz to 2.519 MHz	1.599KHz to 59.589 KHz
Lmax	5.7 nH	165 nH - 530 nH	29 nH	18.01H	0.1721H
Q-factor	70	120 @3GHz	NA	1.235E03	26.07
PDC	8 mW	1.2 mW	4.4 mW	890.518nW to 6.088uW	931.32nW to 6.6uW

To worse the quality factor of design II, the number of MOSFETs is reduced so that the parasitic capacitance decreases which result to decrease in the imaginary part of the impedance value compared to the real part. Also aspect ratio of M7 is kept as minimum as possible to reduce the series resistance. Therefore, the quality factor of the active inductor improves which is reported in Table II. In our work, Design I and design II consumes lesser power than the reported literature [5, 16 , 17]. One designI have better maximum quality factor than the results reported in [5, 16].

IV. CONCLUSION

This work presents a differential active inductor DAI (WI) whose self- resonance frequency and quality factor parameters can be adjusted independently from each other. Additionally, MOSFET (M7) feedback is used to cancel series - loss resistance of the active inductor, which allows self- resonance frequency and quality factor enhancement as well.

The differential active inductor DAI(WI) achieves high quality factor than DAI(Strong inversion).Moreover lower power dissipating 890.518nW to 6.088uW from a single 3.3-V power supply voltage in DAI(designI)is obtained while high power dissipating 931.32nW to 6.6uW from a single 3.3-V power supply voltage is recorded in DAI(designII).canceling parasitic components and determining the properties of the DAI independently are salient feature of the design .We believe that the enhanced linearity renders the active inductor in more practical for realizing Low-voltage, low-power RF filter for wireless applications.

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