VTMOS Circuits Realization through DTMOS Circuits

Dr.K. Ragini,[1] Dr. M. Satyam,[2] and Dr. B.C. Jinaga,[3]

[1] G. Narayanamma Institute of Technology & Science ,

Department of Electronics and Communication Engineering, Hyderabad, India[2] International Institute of Information Technology, Hyderabad, India[3] School of Information Technology, Jawaharlal Nehru Technology University, Hyderabad, India

Abstract : Variable Threshold MOS (VTMOS) circuits have been proposed as a circuit style for low power VLSI systems. They are suitable for sub threshold digital circuit operations. Basically, the principal of sub threshold logic is operating MOSFET in sub threshold region and using the leakage current in that region for switching action, thereby drastically decreasing power. The present paper studies the VTMOS through Dynamic Threshold MOS (DTMOS) by connecting a bias voltage between gate and substrate. The new technique improves circuit performance over DTMOS and consumes less power. Simulations done using 65nm CMOS technology shows that the proposed technique improves inverter's logic levels, saving power over the DTMOS scheme at 0.2v supply voltage and upto 2Mhz operating frequency.

Introduction: In the past, the conventional sub threshold CMOS logic was proposed, which uses the leakage current for switching operation [1, 2, 3]. In DTMOS, the threshold voltage is altered, dynamically to suit the operating state of circuit. A high threshold voltage in the standby mode gives low leakage current, while a low threshold voltage allows higher current drives in active mode of operation. DTMOS can be achieved by connecting the gate and body together [4]. In variable threshold MOSFET, the gate is connected to substrate through a biasing voltage. This bias voltage causes large variation of threshold voltage, with gate voltage than in DTMOS.

In VTMOS circuits ,the ratio ($r = I_{on} / I_{off}$) increases with bias voltage, thus providing a good variation between high and low currents. This higher I_{on}/I_{off} results in good discrimination between V_{OH} and V_{OL} logic levels and reduces overall power dissipation [5]. In view of this, the performance of VTMOS has been studied and its implication on the performance of circuits using this operation is investigated.

This article is organised as follows - In section 1, the typical schematic structures of CMOS, DTMOS and VTMOSFETS are given. Section 2 has description of the various experiments (through simulation) carried out on current-voltage characteristics of N and PMOSFETS with VTMOS configuration. In section 3, estimation of I_{ds} as a function of V_{gs} and V_{AN} is made . The behavior of VTMOS inverter has been described in section 4 from the point of power dissipation, delay characteristics, power delay product and noise - margin. Section 5 shows the results and analysis where it has been found that VTMOS Inverters consume considerably low power with marginal change in the delay characteristics. Section 6 concludes the article.

Section 1:

Structure of MOS, DTMOS and VTMOS configuration.

Typical schematic structures of CMOS, DTMOS and VTMOSFETS are given in Fig 1 (a), 1 (b) and 1 (c). In conventional NMOS circuit, Fig. 1(a), the substrate is normally connected to ground or lowest potential in the circuit. In PMOS circuits, the substrate is connected to supply voltage or the highest potential in the circuit. In DTMOS, Fig 1 (b) the substrate is always kept at gate potential. So when gate potential is varied, substrate potential also varies [6, 7]. Variation in substrate potential results in variation in threshold voltage and hence the transfer characteristics of DTMOS are different from that of conventional CMOS devices [8].

VTMOS is nothing but an extension of DTMOS in the sense that the substrate voltage differs always by a constant voltage from the gate voltage as shown in Fig 1(c).

Section 2

I-V characteristics of MOS devices

To evaluate the behaviour of NMOS devices under VTMOS operating conditions, the I-V characteristics are measured and are given in Fig (2) and Fig (3) [9]. It may be observed from Fig (2) and Fig (3) that general current levels (I_{on} and I_{off}) get reduced with increase in bias voltage when NMOS gate is positively biased with respect to substrate and in the PMOS case, when gate is negatively biased with respect to substrate.

The ratio ($r = I_{on}/I_{off}$) has been calculated for bias voltages V_{AN} in the range of 0 to 0.2V, and is shown in Table (1).DTMOS is nothing but a special case of VTMOS with V_{AN} =0V. It may be seen that the ratio increases with V_{AN}, thus providing a good variation between high and low currents. In order to examine the effect of substrate bias on I-V output characteristics of VTMOS, I_{ds} verses V_{ds} for different substrate bias voltages, Keeping V_{gs} = 0.2v have been measured and are given in Fig (3).

It may be seen that the variation in I_{ds} with V_{ds}, becomes less as V_{AN} is made positive (deep sub threshold region). The characteristics may become flat, indicating that the output resistance becomes high. Thus the drain current is less sensitive to variations in drain voltages, which is a welcome feature for application of device in circuits.

An attempt has been made to estimate the I_{ds} - V_{gs} curve for typical V_{AN} for NMOS device and is described in section 3.

Section 3

Estimation of I_{ds} as a function of V_{gs} and V_{AN} for NMOS [10].

In the sub threshold region, the drain current, I_{ds} is exponentially related to gate volatage, V_{gs} and is shown in equation (1).

$$I_{ds} = I_o \exp\left[\frac{V_{gs} - V_{th}}{V_{tm}}\right]\left[1 - \exp^{\left(\frac{-V_{ds}}{V_{tm}}\right)}\right] \quad - (1)$$

where $Io = \frac{W}{L}\ \mu eff\ C_{ox}\ V_{tm2}$

Where $V_{tm} \rightarrow$ Thermal voltage, KT/q (=25 mv at 25^{o}C)

$\mu_{eff} \rightarrow$ effective mobility (0.06m^2/vs)

$W \rightarrow$ Transistor width (200N)

$L \rightarrow$ Transistor length (70N)

$$C_{ox} = \in_{ox} / t_{ox} = \frac{\in_o \in_r}{t_{ox}}$$

$t_{ox} \rightarrow$ oxide thickness = 1.7 nm

$\in_o \rightarrow 8.854 \times 10^{-12}$F/M

$\in_r \rightarrow$ Relative permittivity (3.9)

$V_{th} \rightarrow$ Threshold voltage

The Threshold voltage equation is

$$V_{th} = V_{to} + \sqrt{} \left(\sqrt{\varnothing - Vbs} - \sqrt{\varnothing} \right) \text{ - 2}$$

$V_{to} \rightarrow$ Threshold voltage at zero bias (0.22)

γ = Bulk threshold parameter (0.43)

$$\varnothing \rightarrow 0.4 + V_{tm} \ln \left[\frac{N_{dep}}{n_i} \right]$$

where $V_{tm} \rightarrow$ thermal voltage = 0.025

$N_{dep} \rightarrow$ channel doping concentration

$\rightarrow 2.6 \times 10^{18}$

$n_i \rightarrow$ Intrinsic carrier concentration

$\rightarrow 1.02 \times 10^{10}$ cm^{-3}

$\varnothing \rightarrow 0.8993$

In order to estimate the I_{ds}-V_{gs} characteristics for NMOS, the following steps are to be considered.

Step1 : For V_{AN} = 0.2v, V_{gs} is varied from 0 to 0.2v, the threshold voltage is calculated from equation (2) for the given parameters.

Step 2. The calculated threshold voltage value is substituted in current I_{ds} equation (1) and corresponding I_{ds} value is obtained.

Step 3. The I_{ds} - V_{gs} values are tabulated and compared with simulated values, in Table (2).

In this case, an attempt has been made to estimate I_{ds} - V_{gs} characteristics using the above equations with BSIM level - 54 MOS model parameters. The calculated values are given in Table 2(a).

Since these characteristics are calculated with only limited values of parameters, the characteristics have been simulated using all the default parameters (reference : as given in HSPICE manual).

The I_{ds} - V_{gs} curve for 0.2v is given in Table 2(a)(manual)and 2(b)(simulated). From these tables it may be seen that the estimated values are different from those values obtained through direct simulation. Therefore one may use expressions to obtain the trends, rather than to obtain actual values. Further investigations use only the simulated values.

Section 4

VTMOS Inverter

The VTMOS Inverter as shown in Fig (4) consists of a PMOS and NMOSFETS, connected in series. The substrate of PMOS is connected to gate through V_{AP}, which bias the gate negative with respect to substrate. The substrate of NMOS is connected, to the gate through V_{AN} which bias the gate positive with respect to substrate. This ensures that both transistors work in the low current region. The transistors for VTMOS are chosen from the 65 nm technology. The threshold voltage for these devices are 0.22v for NMOS and-0.22v for PMOS. The width of NMOS (W_N) and PMOS (W_P) is chosen as 200 nm and 400 nm respectively. The supply voltage is taken as 0.2v which is below the threshold of both the devices.

For different values of V_{AN} starting from O to 0.2v, and corresponding V_{AP} from 0 to - 0.2v, the performance of the inverter - logic levels, power dissipation, frequency response and propagation delay have been obtained, through simulation. When the bias voltage is increased beyond supply voltage, the logic levels are affected. Hence there is a limitation for bias voltage and it should be always below supply voltage.

In the first instance, the transfer characteristics of VTMOS with V_{AN} varying from 0 to 0.2v and V_{AP} varying from 0 to -0.2v have been obtained for V_{DS} = 0.2v. In order to compare these characteristics with CMOS , transfer characteristics of these cases are also obtained in Fig (5). The corresponding logic levels and noise margins are shown in Table (3) and Table(4).

The other important characteristics, of the inverter, i.e. power dissipation, frequency response, propagation delay, have been obtained and reported [9].

In this case the input is taken in the form of square wave varying from 0 to 0.2 v with a rise and fall time of 25 ns. The frequency of square wave is varied over a range of 1 Khz to 2 Mhz.

Section 5

Results and Analysis

This section is sub divided as follows: In section 5.1, the VTC characteristics and logic levels of all inverters are compared. The transient characteristics of inverters are discussed in section 5.2 and effect of frequency on the static and dynamic characteristics are discussed in section 5.3.

Section 5.1

Voltage transfer characteristics / DC Transfer characteristics

The voltage transfer characteristics plots the output voltage as a function of input voltage. For DC analysis the Voltage Transfer characteristics (VTC) of CMOS and VTMOS with various V_{AN}'s are compared in Fig (5). It may be seen that the VTC characteristics of all circuits are similar.

The logic levels in CMOS and VTMOS with various V_{AN}'s ranging from 0 to 0.2v are given in Table (3). It may be seen that, as the bias voltage V_{AN} is increased, the output logic low V_{OL} tends to go down with V_{AN} for a Vgs of 0.2v. The logic high output V_{OH} also go up marginally with V_{AN}. These variations are within tolerable limits for VTMOS and provide good logic swing.

Noise margin : A measure of sensitivity of a gate to noise is given by the noise margin's NM_L and NM_H, which indicate the range of 'O' and ' I' respectively.

To find the noise- margin , the input and output logic levels are required. Both V_{OH} and V_{OL} are obtained from characteristics, and is shown in Table(3).The input logic levels, both V_{IH} and V_{IL} are the points at which the VTC characteristics has slope of -1.To find these points ,the curve for the derivative of VTC is to be obtained, and the two points at which the value is -1 is to be found and that gives V_{IL} and V_{IH} logic levels.

$NM_L = V_{IL} - V_{OL}$

$NM_H = V_{OH} - V_{IH}$

A large noise margin is always desirable. The noise margin of CMOS and VTMOS with various V_{AN} are calculated and are given in Table (4).

The noise margin increases as one go from CMOS to VTMOS (0.2v).

Section 5.2

Transient (Dynamic Characteristics of Inverter)

The variation of Propagation delay, power dissipation and power delay product for different devices (CMOS and VTMOS with various VAN'S) are given in Table (5) for a frequency of 100KHZ and at V_{dd} = 0.2V. From Table (5) the following conclusion are made.

(1) **Propagation delay**. The propagation delay associated with the inverter has been calculated through the values of T_{PLH} and T_{PHL} obtained through simulation, for various values of V_{AN}, and given in table (5). It was been found that the propagation delay increases as one increase V_{AN}.

(2) **Power dissipation** : The power consumed by the inverter for a square wave of 0.2v amplitude with varying V_{AN} at a frequency of 100 Khz has been measured further and given in Table (5). It has been found that the power dissipation decreases considerably with increase in V_{AN}.

(3) **Power delay product** : From Table (5) it may be seen that, while the power dissipation decreases with increase in V_{AN}, the delay has been found to be increased. In order to get an idea of the merit of operating the inverter in sub threshold region, the power delay product has been computed and given in the same table (5). It may be seen that , the PDP decreases with increase in V_{AN} . Thus the VTMOS appear to have an edge over the other configuration from the point of power and delay.

Section 5.3

Effect of frequency on the static and dynamic characteristics.

The static and dynamic characteristics mentioned above have been measured for various types of Inverters at the frequency range of 1 Khz to 2 Mhz.

In order to get an idea of the effect of frequency on the dynamic characteristics, they are measured at different frequencies ranging from 1Khz to 2Mhz.

It has been found that the general nature of variation of power dissipation and propagation delays are maintained as those reported at 100 Khz. However, the power dissipation increases with frequency and the variation of power dissipation with frequency for CMOS and VTMOS(0 to 0.2v) is shown in Fig(7). Propagation delay and logic levels remain almost constant with frequency. The power dissipation in VTMOS increases faster than in the case of CMOS inverter and there is no visible advantage of operating the inverter in VTMOS mode beyond 2Mhz.

Section 5.4 :

Estimation of power consumption

The overall average power consumption in conventional CMOS devices can be expressed as the sum of 3 main components.

1. The dynamic (switching) power consumption.
2. The short - circuit power consumption.
3. The leakage power consumption or static power consumption.

The dynamic power is a result of power consumed in charging and discharging load capacitance in the circuit. Short circuit power arises when a conducting path between supply voltage and ground is formed. Static power is the power dissipated while the device is turned off.

The Table (6) shows the three components of power for CMOS and VTMOS with various V_{AN}. For a device with C_{load} =10fF and frequency = 100 Khz, static power dissipation is dominant power at 100 khz, when compared to dynamic and short circuit power. Both static and short-circuit power components are obtained through simulation and dynamic power is calculated by the equation $P_{dyn} = C_{load} V_{DD}^2 f_{clk}$.

Conclusions : From the observation made and analysis done, the following conclusions have been arrived at. With a view to reduce the power dissipation of CMOS and DTMOS circuits, the gate is biased positive with respect to substrate for NMOS and biased negative with respect to substrate for PMOS. Currents

flowing through the channel is further reduced compared to CMOS and DTMOS devices resulting in further reduction in power dissipation.

Further the leakage current which flows through out the operation is also reduced. In view of this, these circuits which we call as VTMOS have been visualized simulated and the performance has been measured. The measurement include transfer characteristics of VTMOS devices with drain voltage 0.2V less than the threshold voltage of FET for different values of V_{AN} for both P and N MOSFETS. Through this transfer characteristics, the leakage or static power is estimated. This is followed by simulation of the inverter with different V_{AN} values. The power consumed and the corresponding delay for different V_{AN}'s at different frequencies have been measured. The power delay product with V_{AN} at specific frequency has been estimated. It has been found that the power dissipation in general, decreases with increase in V_{AN} upto input frequency of 2Mhz and it is lower than the power consumed by CMOS and DTMOS Inverters. However the PDP improves only upto 500 khz. It may be possible to further increase the frequency response by appropriately designing the transistors to suit the requirements.

Figure captions:

Fig. 1 : Structures of CMOS DTMOS and VTMOS configuration.

Fig. 2 (a) : Ids-Vgs characteristics of VTMOS with V_{AN} varying from 0 to 0.2v.

Fig. 2 (b) : Ids - Vgs characteristics of VTMOS with V_{AN} varying from 0 to 0.2V (zoomed versions) to get I_{off} of VTMOS.

Fig. 3 : I_{ds} - V_{ds} characteristics of VTMOS with V_{AN} varying from 0 to 0.2V.

Fig. 4 : VTMOS inverter

Fig. 5 : Voltage transfer characteristics of CMOS and VTMOS Inverter with V_{AN} varying from 0 to 0.2v.

Fig. 6 : Frequency versus power dissipation for VTMOS Inverter with V_{AN} varying from 0 to 0.2v.

Figure 1a - CMOS Structure

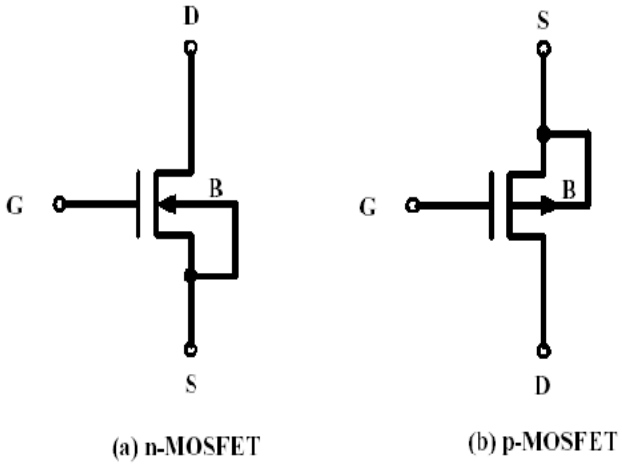


Figure 1b - DTMOS Structure

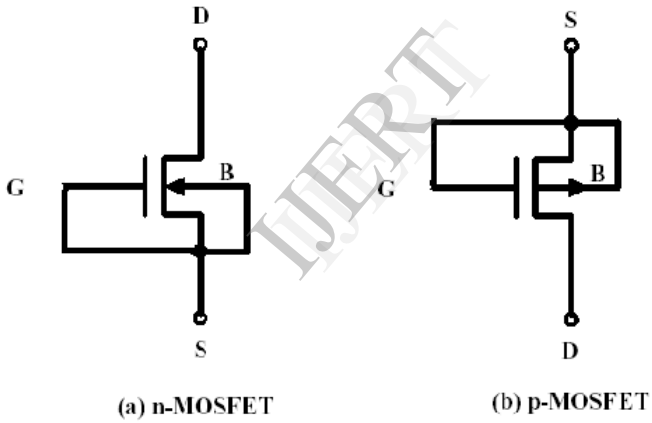


Figure 1c - VTMOS Structure

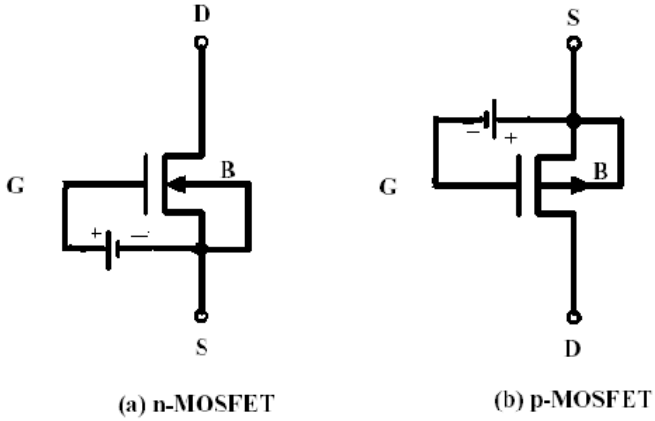


Figure 2a -I_{ds} - V_{gs} Characteristics of VTMOS V_{AN} Varying from 0(top) to 0.2V(Bottom)

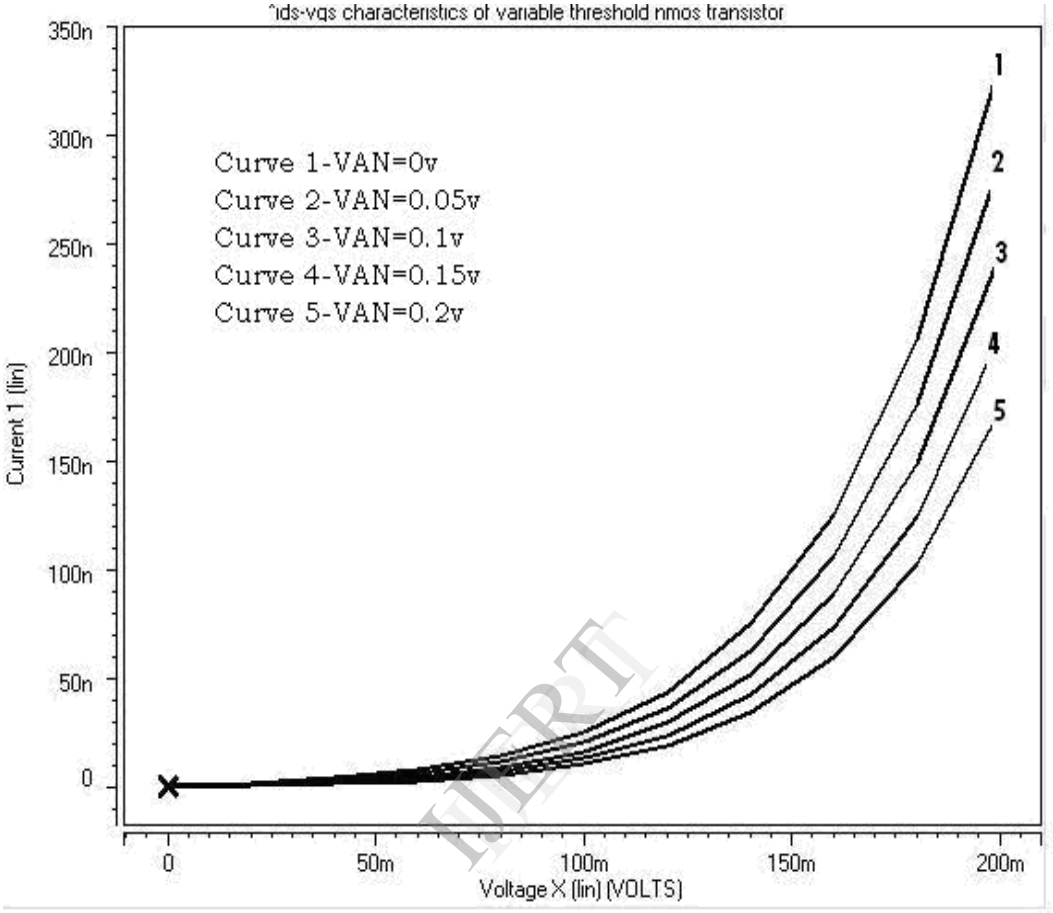


Figure (2b)- I_{ds}-V_{gs} Curves for VTNMOS-V_{AN} Varying From 0(Top) TO 0.2V(Bottom)

(Zomed Version)

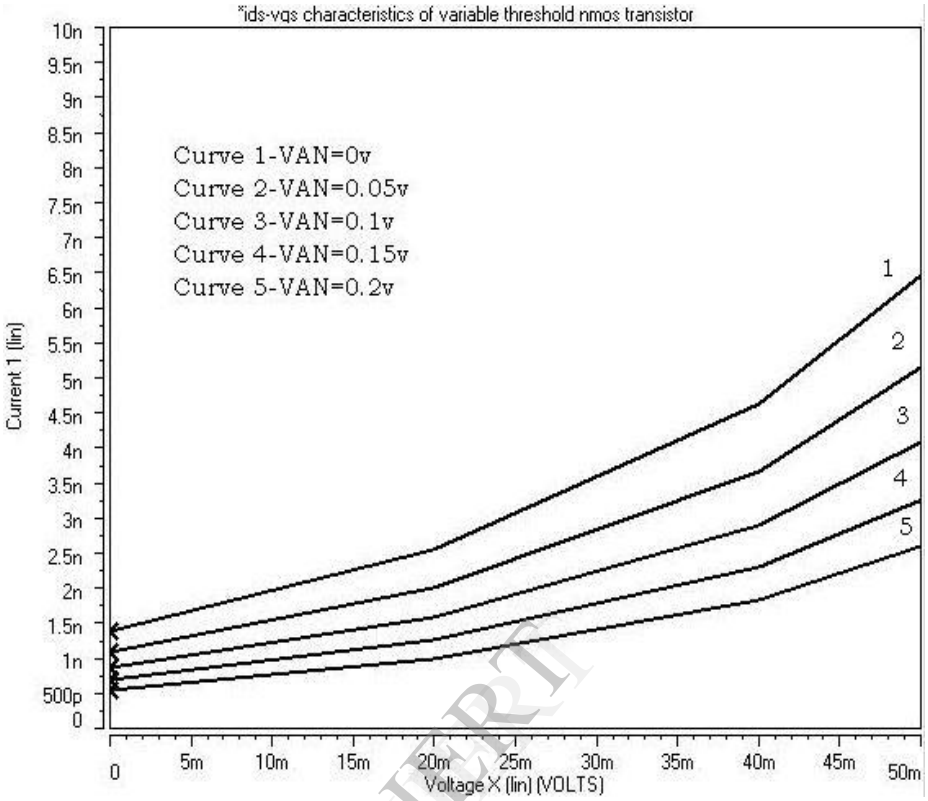


Fig 3- I_{ds}-V_{ds} Curves For VTNMOS-V_{AN} Varying From 0(Top) TO 0.2V(Bottom)

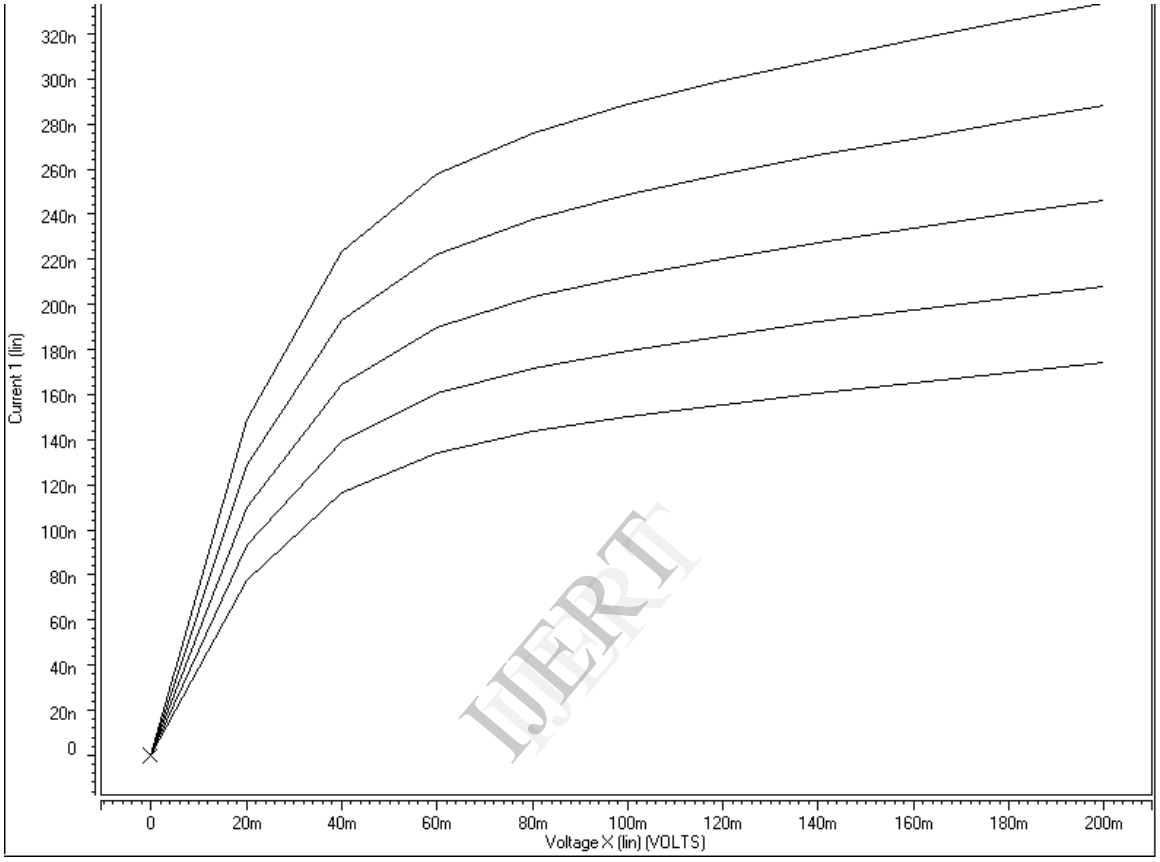


Figure 4 VTMOS Inverter

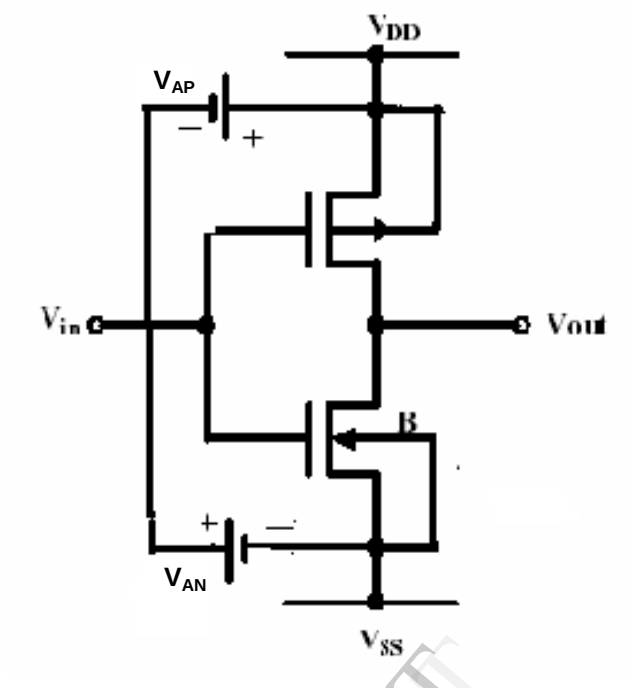
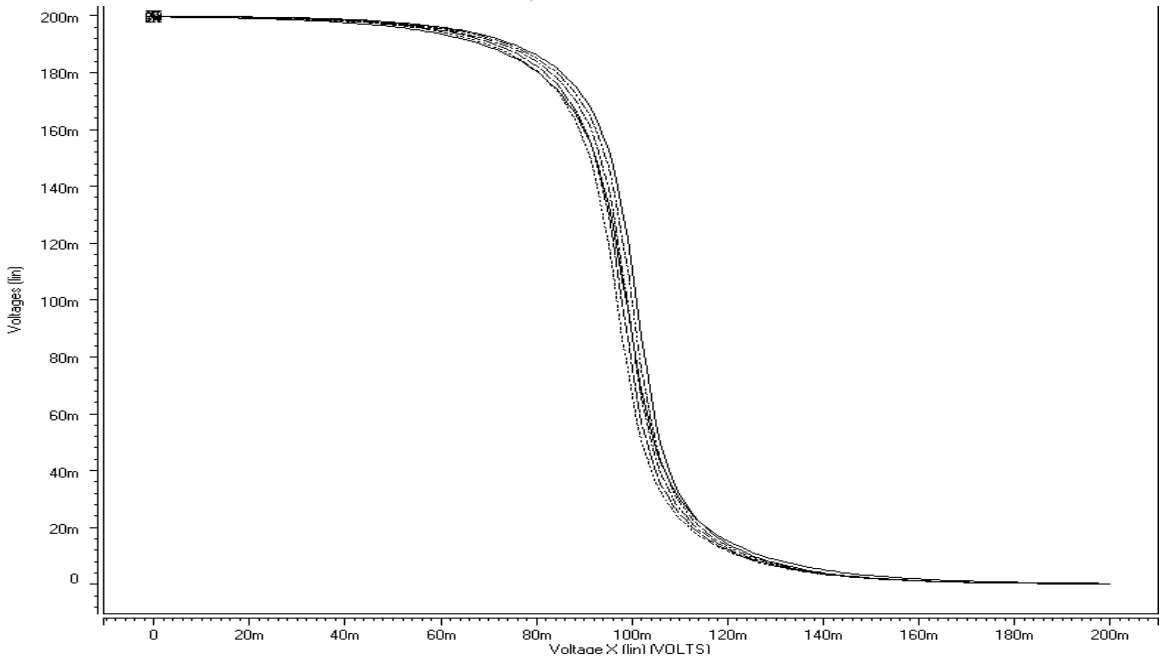


Figure 5 Voltage Transfer characteristics of CMOS and VTMOS (V_{AN} varying from 0 to 0.2 V)



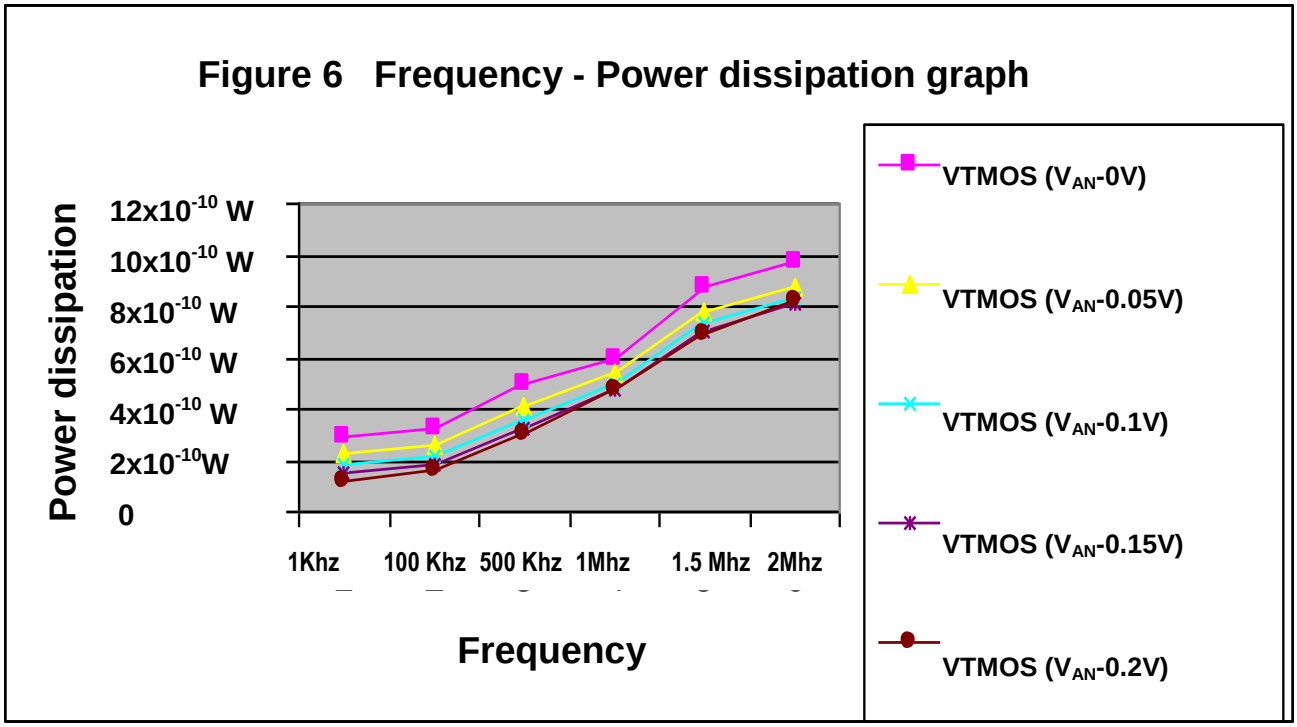


Figure 6 Frequency - Power dissipation graph
Power dissipation
12x10-10 W
10x10-10 W
8x10-10 W
6x10-10 W
4x10-10 W
2x10-10W
0
1Khz
100 Khz
500 Khz
1Mhz
1.5 Mhz
2Mhz
Frequency
VTMOS (VAN-0V)
VTMOS (VAN-0.05V)
VTMOS (VAN-0.1V)
VTMOS (VAN-0.15V)
VTMOS (VAN-0.2V)

Table Captions:

Table 1 V_{AN} versus I_{on} / I_{off} ratio.

Table 2 I_{ds} - V_{gs} curve for V_{AN} = 0.2V and V_{ds} = 0.2V

Table 3 Logic levels for CMOS and VTMOS with V_{AN} varying from 0 to 0.2 volts.

Table 4 Noise margins are compared for CMOS and VTMOS with V_{AN} varying from 0 to 0.2 volts.

Table 5 Variation of propagation delay, power dissipation and power delay product for CMOS and VTMOS with VAN varying from 0 to 0.2v.

Table 6 Components of Power and total estimated power is compared with average power dissipation for CMOS and VTMOS varying from 0 to 0.2v.

TABLES

Table:1

V_{AN} (v)	I_{on}/I_{off}
0	244
0.05	258
0.1	271
0.15	290
0.2	300

Table - 2 (a)
Manual

I_{ds}	V_{gs}(v)
58pA	0
668pA	0.05
8nA	0.1
84nA	0.15
969 nA	0.2

Table - 2 (b)
Simulation

I_{ds}	V_{gs} (v)
565 pA	0
1.5nA	0.05
25nA	0.1
50nA	015
170nA	0.2

Table-3

Device	V_{OH} (mv)	V_{OL} (mv)
CMOS	199.64	0.279
VTMOS (V_{AN}-0v)	199.77	0.149
VTMOS (V_{AN}-0.05v)	199.80	0.140
VTMOS (V_{AN}-0.1v)	199.83	0.136
VTMOS (V_{AN}-0.15v)	199.84	0.135
VTMOS (V_{AN}-0.2v)	199.86	0.134

Table - 4

Device	NM_H mv	NM_L mv
CMOS	83.64	81.32
VTMOS (V_{AN}-0v)	84.07	81.60
VTMOS (V_{AN}-0.05v)	84.20	81.64
VTMOS (V_{AN}-0.1v)	84.25	81.65
VTMOS (V_{AN}-0.15v)	84.34	81.66
VTMOS (V_{AN}-0.2v)	84.38	81.66

Table -5

C_{load} = 10ff freq = 100 khz PULSE (0 0.2 0 0.025u 0.025U 5U 10.05U)

Device	t_{phl}	t_{phl}	t_p (sec)	Power dissipation (watt)	Power Delay Product
CMOS	1.401×10^{-8}	1.414×10^{-8}	1.455×10^{-8}	3.139×10^{-10}	4.512×10^{-18}
VTMOS (V_{AN}-0v)	1.170×10^{-8}	1.029×10^{-8}	1.115×10^{-8}	3.235×10^{-10}	3.606×10^{-18}
VTMOS (V_{AN}-0.05v)	1.254×10^{-8}	1.124×10^{-8}	1.205×10^{-8}	2.638×10^{-10}	3.179×10^{-18}
VTMOS (V_{AN}-0.1v)	1.337×10^{-8}	1.247×10^{-8}	1.310×10^{-8}	2.178×10^{-10}	2.852×10^{-18}
VTMOS (V_{AN}-0.15v)	1.344×10^{-8}	1.379×10^{-8}	1.423×10^{-8}	1.836×10^{-10}	2.612×10^{-18}
VTMOS (V_{AN}-0.2v)	1.464×10^{-8}	1.507×10^{-8}	1.538×10^{-8}	1.227×10^{-10}	1.866×10^{-18}

Table 6 - Components of power dissipation

Device	Static Power dissipation (watts)	Dynamic Power dissipation (watts)	Short circuit power dissipation (watts)	Estimated total power dissipation (watts)	Simulated average power dissipation (watts)
CMOS	$2.79\ x10^{-10}$	$0.4\ x10^{-10}$	$0.075\ x10^{-10}$	$3.265\ x10^{-10}$	$3.140\ x10^{-10}$
VTMOS (V_{AN}-0v)	$2.84\ x10^{-10}$	$0.4\ x10^{-10}$	$0.186\ x10^{-10}$	$3.426\ x10^{-10}$	$3.235\ x10^{-10}$
VTMOS (V_{AN}-0.05V)	$2.20\ x10^{-10}$	$0.4\ x10^{-10}$	$0.179\ x10^{-10}$	$2.779\ x10^{-10}$	$2.638\ x10^{-10}$
VTMOS (V_{AN}-0.1v)	$1.73\ x10^{-10}$	$0.4\ x10^{-10}$	$0.171\ x10^{-10}$	$2.3005\ x10^{-10}$	$2.177\ x10^{-10}$
VTMOS (V_{AN}-0.15v)	$1.37\ x10^{-10}$	$0.4\ x10^{-10}$	$0.155\ x10^{-10}$	$1.925\ x10^{-10}$	$1.836\ x10^{-10}$
VTMOS (V_{AN}-0.2v)	$1.09\ x10^{-10}$	$0.4\ x10^{-10}$	$0.148\ x10^{-10}$	$1.638\ x10^{-10}$	$1.59\ x10^{-10}$

References:

1. H.Soeleman, K. Roy and B.C. Paul : 'Robust subthreshold loigc for ultra low power operation ; IEEE trans VLSI syst., Vol. 9, PP. 90-99, Feb 2001.

2. Jabulani : Nyathi and brent Bero; "Logic circuits operating in subthreshold voltages" ISLPED 06, October 4-6, 2006, Tegernsee, Germany.

3. C. Hyung - 11 kim, H.Soeleman and K.roy, "ultra-low power DLMS Adaptive Filter for hearing Aid Applications, IEEE transactions on very large scale integration (VLS1) system, vol. 11, No.6, Decemberr, 2003. PP 1058-1067.

4. Fariborz Assaderaghi ; stephen Parke, Dennis Simitsky, Jeffrey Bokor, Ping K. KO. chenming Hu 'A Dynamic threshold voltage MOSFET (DTMOS) for very low voltage opertaion'. IEEE Electron device letters, vol. 13, No.12, December 1994.

5. Tae-Hyoung kim, Hanyang Eom, John. Keane, and chris Kim Utilizing reverse short channel effect for optimal sub threshold circuit design," ISLPED 06, October 4-6, 2006. Tegern . see, Germany.

6. F. Assaderaghi et al., "Dynamic threshold - voltage Mosfet (DTMOS) for ultra - low voltage VLSI, "IEEE trans Electron Devices, Vol. 44, PP 414-422, Mar 1997.

7. T. Kobayashi and T.Sakurai "Self-adjusting threshold voltage scheme (SATS) for low-voltage high - speed operation ; in custom integrated circuits conf., May 1994, pp.271-274.

8. Wet Jin and Philip Ch. Chan: A comparative study of S01 inverter circuits for low voltage and low power applications" Proceedings 1997 IEEE International SOI conference, Oct. 1997.

9. Liquiong Wei, Kaushik Roy and Cheng - kok koh : "Power minimization by simultaneous Dual - Vth Assignment and Gate Sizing" "IEE 2000 custom integrated circuits conference.

10. N. Weste and K. Eshraghian, Principles of CMOS VLSI Design, A System perspective, Reading, M.A. Addison - Wesley, 1993.

11. Rabacy, J.M., Digital Integrated circuits: A design perspective 1st ed upper saddle river, new jersey: Prentice Hall, 1996.