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# VLSI Implementation of Adaptive FIR Filter using DA with Low Power and Low Area

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***Abstract-*** **Adaptive Filter are digital filters whose coefficients change with an objective to make the filter converge to optimal state. The conventional adaptive Fir filter the adder-based shift accumulation is replaced by compressor adder are used to reduce area and the critical path is large to obtain filter response so pipelined concept are introduced in the least mean square (LMS)algorithm. With these two concepts the power consumption of the adaptive filters will be reduced. This will be coded in Verilog HDL language and implemented on Artix 7 FPGA hardware. This will be suited for signal processing application design such as adaptive decision feedback equalizer for removing the signal noises, hearing aids and ECG signal analysis.**

***Keywords: Pipelined, LMS adaptive FIR filter, Distributed Arithmetic, Compressor adder, Artix 7 FPGA***

## I. INTRODUCTION

An adaptive filter is a digital filter that has self-adjusting characteristics. It is capable of adjusting its filter coefficients automatically to adapt the input signal via an adaptive algorithm. Adaptive filter play an important role in digital signal processing (DSP) products in area such as telephone echo cancellation, noise cancellation, equalization of communication channel, biomedical signal enhancement, active noise control (ANC), and adaptive control systems. Adaptive filter work generally for the adaptation of signal-changing environments, spectral overlap between noise and signal and unknown or time-varying noise.

Adaptive filter are widely used in several digital signal processing applications. The tapped-delay line finite impulse response (FIR) filter whose weights are updated by the Least mean square (LMS)algorithm is the mostly popularly used adaptive filter not only due to its simplicity but also due to its satisfactory convergence performance. The direct form-configuration on the forward path of the FIR filter results in a long critical path due to the inner-product computation to obtain a filter output. Therefore, when the input signal has sampling rate, it is necessary to reduce the critical path of the structure so that the critical path could not exceed the sampling period.

LMS is the frequently used algorithm in adaptive filtering. It is basically a gradient descent algorithm which means that is adjusts the adaptive filter coefficients by modifying them by an amount which is proportional to the gradient of the error surface. It can be represented in the following equation (1).

$$F(u(n), e(n), \mu) = \mu e(n)u^{*}(n) \quad \ldots\ldots\ldots\ldots (1)$$

In signal processing applications such as echo cancellation, digital communications an adaptive filter, is essential since only a limited amount of a priori knowledge of signal properties is available in. It consist of multiplier, delay elements and adders. When we observe the architecture multiplier will occupy more area and power consumption. The linear combiner form the filter output y, remains at the centre of the architecture. The adaptive filter will change the filter coefficient to bring them closer to their ideal values. The filter coefficient can be updated with a variety of adaptive techniques. FIR and IIR are two types of adaptive filters. Because of the natural stability and ease of computation adaptive FIR filter are more advantageous than IIR filters.

Least mean square adaptive design, Recursive adaptive design, Normalized adaptive filter are the three main algorithms presents. Because filter coefficients may be quickly adjusted, the least mean square adaptive method is better choice. Multiplier, shifter, and adder are commonly used in any filters. Multiplier will take up more space and energy. Multiplier architecture are replaced by multiplier-less architecture in adaptive FIR filter to save area and power consumption. To enhance the speed and reduce power, a number of multiplier-less adaptive FIR filter topologies are available. The distributed arithmetic model is well known multiplier-free design for more efficient adaptive filter implementation.

## II. PREVIOUS WORK

In 1996, pipeline FIR filter architecture and increasing performance of decision-feedback equalizer [13] in which using Booth-encoding based input decomposition scheme for FIR filter implementations. The high-order/high speed FIR filter architecture usually have unavoidable pipelining delays, and they add to the feedback loop delay of the decision feedback equalizers. The added delay degrades the performance of the equalizer for strong ISI signals. Finally, we present a new decision feedback equalizer architecture which function perfectly even though strong near-ISI signals exist in the channel.

In 2020, a generalized maximum correntropy criterion based robust sparse adaptive room equalization.[4] An adaptive room equalization scheme is usually employed to compensate for the distortion of sound produced by the room impulse response, thereby offering an improved listening experience. In a conventional adaptive room equalizer, an adaptive filter updated using a filtered-x least mean square

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(FxLMS) algorithm is used to achieve room equalization. FxLMS algorithm-based room equalizers are not robust to strong disturbances picked by the reference microphone. An adaptive room equalizer tries to compensate for the deterioration in audio quality caused by the acoustic path between loudspeaker and the listener. In its basic form, an adaptive room equalization system consists of an adaptive filter which is added between the sound sources and loudspeaker.

### FIR FILTER USING LMS ALGORITHM

Mostly the adaptive filter is used in noise cancellation applications. The desired signal is combination of source signal and noise signal which is uncorrelated to the signal. Filters takes a noise input and correlates with the noise in desired signal to obtain the actual signal. Input of a filter is a reference noise which is correlated with the noise in the desired signal. The error term e(n) obtained from the system is then used to cancel the noise in the original signal by using the LMS algorithm. Most widely use algorithm in adaptive filter is an LMS algorithm due to its simplicity. It doesn't needs an extra mathematical calculation like matrix inversion nor correlation function.

Mean square error (MSE) logic is used in LMS algorithm.[6] It uses an input signal, step-size parameter, the subtraction of desired signal and filter output signal for calculating the updated filter coefficients. The LMS algorithm uses a structure of an FIR filter. Filter as two main components those are L delay registers and weight updated blocks. The unit delay register are made of D flipflops. And each weight updated component consist of multiplier, adder, and a buffer to store the new updated weights of the filter coefficient. According to error signal is obtained from the difference of the filter output and desired signal. The error signal is then multiplied with input signal and step size μ, which produces next sets of filter coefficients.

### FIR FILTER WITH SEVERAL WINDOW FUNCTIONS

FIR low-pass filter is analysed and designed by window function method [3] The design of FIR filter with different window functions such as Hamming window and Hanning window, simulates on MATLAB platform, and compares and analyses the influence of different window functions on the design performance of FIR filter.

Hanning window is also called rising cosine window. The side lobe is greatly reduced and the main lobe width is doubled. Thus, high frequency interference and energy leakage can be eliminated. Compare with the spectrum of hanning window and rectangular window, the main lobe of hanning window is widened and reduced, and the side lobe is significantly reduced. Hanning window is better than rectangular window. However, the disadvantage of hanning window is that it widens the main lobe, which is equivalent to widening the analysis bandwidth and reducing the frequency resolution.

Hamming window is also a kind of cosine window, also known as improved raised cosine window. It and Hanning window are cosine windows, but the weight coefficient is different. The weighting of Hamming window will make the side lobe smaller. Its spectrum is also composed of three rectangular windows, and the attenuation speed is slower than that of Hanning window. Hamming window and Hanning window are window functions often in signal processing.

## III. CURRENT WORK

Adaptive filters have coefficients that are allowed to vary over time. They are used when the filter response that best accomplishes a particular task is not known a priori, or when the nature of the operating environment is expected to change over time. A typical system goal would be for a filter to suppress undesired noise to the greatest extent possible while leaving the target signal intact to the extent possible.

$$yk = \sum_{l=0}^{L-1} xlk\ wlk$$

.....(1)

Where the $\{wlk\}$represent the variable weights of the adaptive filter and the signals $\{xlk\}$ are the inputs to those weights. While this equation can be applied directly to any system for which the output is obtained by computing the linear combination of the outputs of an array of sensors, the most common implementation for the adaptive processor is that of an FIR filter with variable coefficients. The block diagram of adaptive FIR filter as shown in Fig.1.

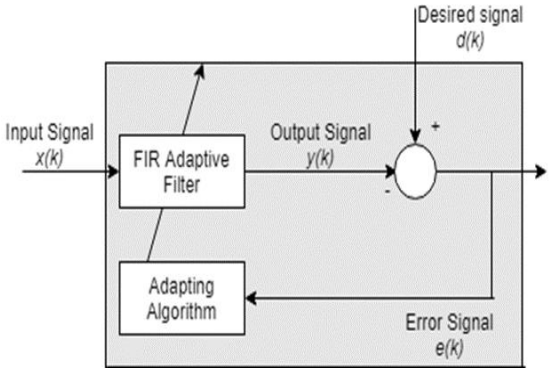


Fig.1 Block diagram of adaptive FIR filter

### ADAPTIVE FIR FILTER USING DA WITH LOW POWER AND LOW AREA

A low-complexity pipelined adaptive FIR filter is designed using Distributed Arithmetic (DA) architecture for signal processing applications. Generally adaptive filter will occupy more area and power consumption because of using memories in the filters for partial product (PP) generation. To get rid of this, the pipeline concept to reduce the registers in the filter and also reduce the area further compressor adders are used in the adaptive filter architectures instead of using normal adders. With these two concepts the area and power consumption of the adaptive filter will be reduced.

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And is well suited for signal processing application designs such as adaptive decision feedback equalizers for removing the signal noises and inter symbol interference, hearing aids and ECG signal analysis.

It consist of multipliers, delay elements and adders. The adaptive filters will change the filter coefficient to bring them closer to their ideal values. The filter coefficient can be updated with a variety of adaptive techniques. FIR and IIR are two types of adaptive filters. Because of their natural stability and ease of computation, adaptive FIR filters are more advantageous than IIR filters. Adaptive filters come in a variety of shapes and sizes. Least mean square adaptive design, Recursive adaptive design, Normalized adaptive filter are the three main algorithms present. Because filter coefficients may be quickly adjusted, the least mean square adaptive method is a better choice.

Fig.2 shows the 4-point inner product block. It contains a DA table, 16:1 multiplexer, and conditional carry save accumulator. The DA table, which is made up of a 15 registers array, stores the partial inner products y. The register's contents are selected using the 16:1 multiplexer (MUX). The weight vector A=h31h21h11h01 is used to regulate the MUX, and the MUX output is sent to the conditional carry save accumulator (CSA) after every L bit cycles. The CSA is used to shift and aggregate all partial inner products acquired from the MUX, as well as produce a total and a carry for each with a bit length of (L+2). To generate filter output, the sum words ROM the carry save accumulator are shifted and then added with the carry words and an input carry "1" is employed. The error signal e is obtained by subtracting the filter's result from the target signal w(n).

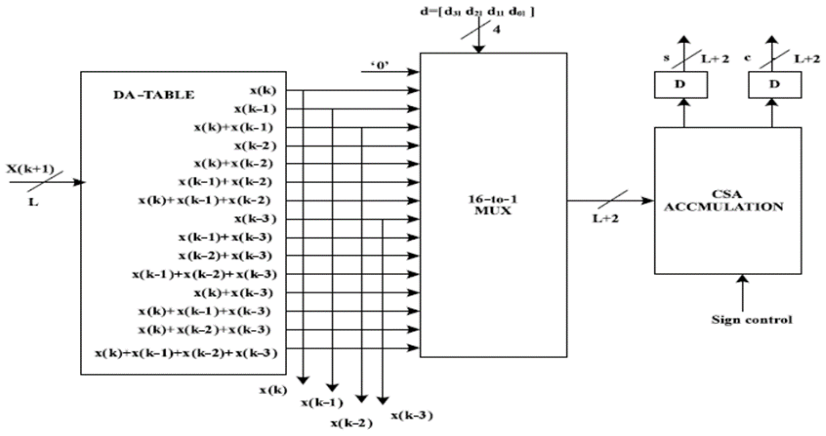


Fig.2 Inner product block

Except for the most significant bit, all of the bits of the error signal are evaluated, and the error signal is multiplied by a right shift. The no. of sites to be moved will be determined by the magnitude of the error, which is dependent on the number of leading zeros present. Execute the control word 't' present in the barrel shifter by leveraging that error. In error calculations, the convergence factor is commonly given as O(1/N). In the current DA design, we have assumed it is =1/N. In contrast,2-i/N is used when 'i' is a tiny integer value. To reduce hardware complexity, 'i' places increase the amount of shifts in the t and 'I' places increases the input to the barrel shifters.

## DISTRIBUTED ARITHMETIC (DA)

It is widely used technique for implementing sum-of-products computations without the use of multipliers. Designers frequently use DA to build efficient Multiply-Accumulate Circuitry (MAC) for filters and other DSP applications. The main advantages of DA is its high computational efficiency. DA distributes multiply and accumulate operations across shifters, lookup tables (LUTs), and adders in such a way that conventional multiplier are not required. It is extensively used in computing the sum of products.

Fig.3 illustrate the partial product DA table for N=4. It has seven parallel adders, each of which calculates seven new clock values in advance. It will assist in reducing the no. of clock cycles needed to compute the sums of input samples. It only has 15 registers to aggregate the pre-computed sums of partial products of the input words. It takes only four clock cycles to compute all 15 products for input bits data length of 8 bits.

Rather than providing x(k+1) input samples to the adders and register every time, the pipelined DA table architecture uses prior register samples recovered from the registers and returned as inputs to the adder to accomplish the same DA table features. There are 15 registers and 7 adders in total, requiring hardware.

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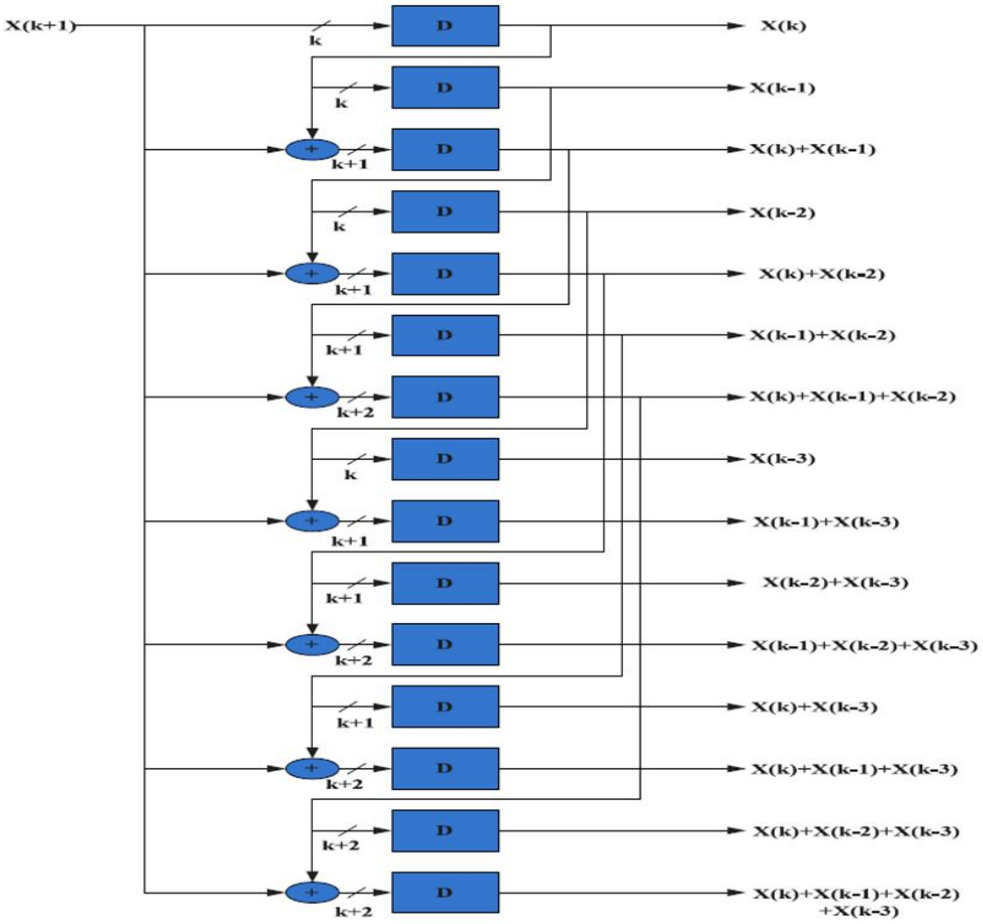


Fig.3. Partial product outputs of DA tables

To construct X(k-1) +x(k+1), the inputs x(k) and x(k+1) are added and transferred via the register x(k). As a result, the register and adders will produces outputs like x(k-2) +x(k), x(k), x(k-2) +x(k-1) ….., which will delivered in to a 16:1 multiplexer with filter coefficient as selected lines.

## ADAPTIVE FILTER ALGORITHM

For every clock cycle the filter coefficient can be updated in adaptive filter to find filter output and error value. The error value achieved is used for filter coefficient updating process.

Input data $X(k)$ ,

$X(k) = [x(k),\ldots\ldots x(k-K+1)]^T$ ……(1)

'T' = Transposed form.

Output signal $Y(k)$ ,

$Y(k) = h(k)X^T(k)$ ……(2)

h(k) = filter coefficient vector

Weight updating of the LMS algorithm is :

$h(k+1) = \mu e(k)X(k) + h(k)$ …….(3)

Eq. (3) is the increment of filter coefficient

Where $\mu$ = Step size , e(k) = error signal

$e(k) = (D(k) - Y(k))$ …….. (4)

$D(k)$ = desired signal

## COMPRESSOR ADDER

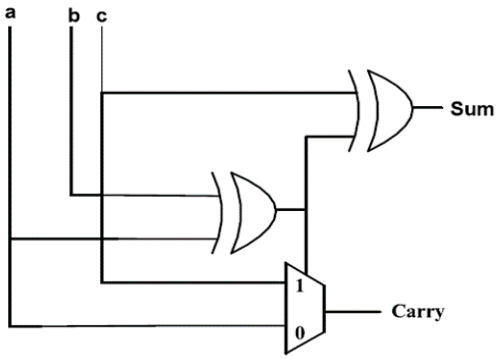


Fig.4. Compressor adder

The size of DA-based adaptive filters may be lowered by adopting the design, and to reduce the adders, a 3:2 compressor adder with two XOR gates and a 2:1 multiplexer. a, b, c are the inputs with sum and carry as outputs. The signal a, b are passed to first XOR gate, the output of first XOR gate will passed as one input to the second XOR gate and c is the second input to the second XOR gate. Both the signals are passed and get final sum. Whereas for getting carry a, c are passed as inputs to the 2:1

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MUX to get carry as output. By using this method the number of gates are going to reduced in adder gates which are shown in Fig.4. As a result, the number of adders required decreases as the area decreases.

## IV. SYSTEM DESIGN REQUIREMENTS

### MATALB

MATLAB is a software package for high performance mathematical computation, visualization, and programming environment. It provides an interactive environment with hundreds of built-in functions for technical computing, graphics and animations. MATLAB stands for Matrix Laboratory. MATLAB is a modern programming language environment, and it has refined data structure, includes built-in editing and debugging tools, and support object oriented programming. MATLAB is Multi-paradigm. So it can work with multiple types of programming approaches, such as functional, object-oriented and visual.

Filter design using MATLAB with different windows are taken for the verification of signal with noise filtering. The different windows frequency spectrum, signal-to-noise ratio and magnitude response are taken from the MATLAB. The kaiser window, equiripple method, hamming window and hanning window are used for the filter design. The input sine wave with high frequency noise are filtered into original signal using MATLAB. The sampling frequency 1000Hz, passband frequency 500Hz and stopband frequency 600Hz are provided to design the low pass filter. The filter coefficients are taken from the MATLAB and it is converted into hexadecimal for assigned in Xilinx Vivado for Verilog implementation.

### XILINX VIVADO

Vivado design suite is a software suite produced by Xilinx for synthesis and analysis of hardware description language (HDL) designs, superseding Xilinx ISE with additional features for system on a chip development and high-level synthesis. Vivado includes the in-built logic simulator. Vivado also introduces high-level synthesis, with a toolchain that converts C code into programmable logic.

The framework was executed in Xilinx vivado using Verilog programming along the test bench and results. The filter design is taken in Xilinx vivado using distributed arithmetic with the behavioral simulation of waveform shows the filtering of input sine wave with noise will extract the original signal. The vivado platform is used to implement in the hardware Artix 7 FPGA. The Signal-to-noise ratio, power consumption, area are identified by the vivado platform.

### ARTIX 7 FPGA

Artix 7 FPGA provides high performance-per-watt fabric, DSP processing and analog mixed signal integration in a cost optimized FPGA. The Xilinx Artix-7 FPGA board is flexible enough for different application reprogramming. Artix 7 FPGA have about 50% lesser total power consumption than earlier generation. The Xilinx Artix-7 FPGA board features 32 MB of SDRAM memory. The Xilinx Artix-7 FPGA has redefined cost-sensitive solutions by cutting power consumption in half from the previous generation while providing best-in class transceivers and signal processing capabilities for high bandwidth applications. Built on the 28nm HPL process, together with the MicroBlaze (TM) soft processor, Artix-7 FPGAs are ideal for products like portable medical equipment, military radios, and compact wireless infrastructure. Artix-7 FPGA meet the need of size, weight, power, and cost sensitive markets.

## V. RESULTS AND DISCUSSION

Low-pass filters are often used to clean up signals, remove noise, create a smoothing effect, perform data averaging, and design decimators and interpolators. Low-pass filters produce slow changes in output values to make it easier to see trends and boost the overall signal-to-noise ratio with minimal signal degradation.

FIR filters are very attractive because they are inherently stable. They can be designed to have linear phase that introduces a delay in the filtered signal while maintaining the waveform shape. Nonetheless, these filters can have long transient response and might prove computationally expensive in certain applications. FIR filters are useful in audio, biomedical, radar, and other applications where the waveform shape provides useful information. Common design methods for low-pass FIR-based filters include Kaiser window, Least squares, and equiripple.

The filter coefficient from MATLAB are the numerical value is converted into hexadecimal for assign in Verilog. The normal sine wave with high frequency noise added are filtered to extract original and spectrum as shown in Fig.5, 6 and 7. The 300Hz sine wave, 1000 HZ sine Fig.8. The different window such as equiripple, Kaiser window, hanning window and hamming window are designed in MATLAB for verifying the Original signal with its spectrums are shown in Fig.9, 10,11and 12. The adaptive FIR filter using DA are designed in Verilog implementation using vivado and its behavioral simulation as shown in Fig 13and is implemented in Artix 7 FPGA. The power consumption, area , signal-to-noise ratio and mean square error are calculated in vivado.

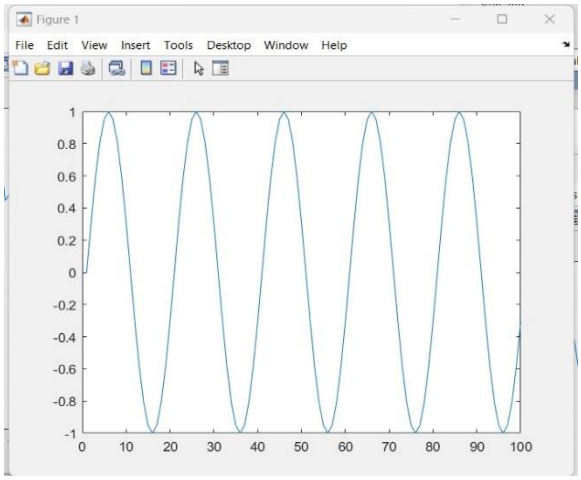


Fig.5. Basic sine wave developed in MATLAB

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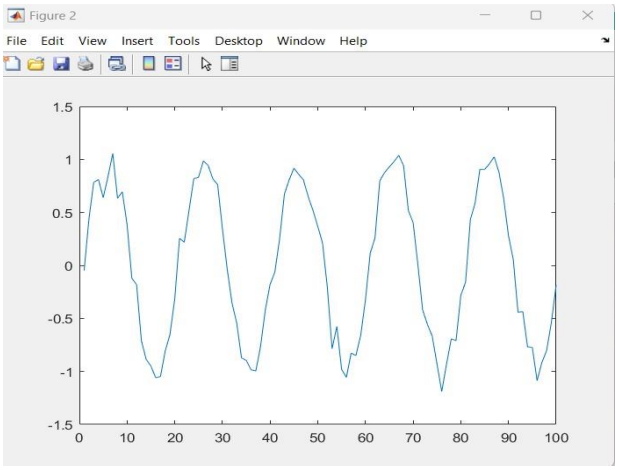


Fig.6.Sine wave added with high frequency noise

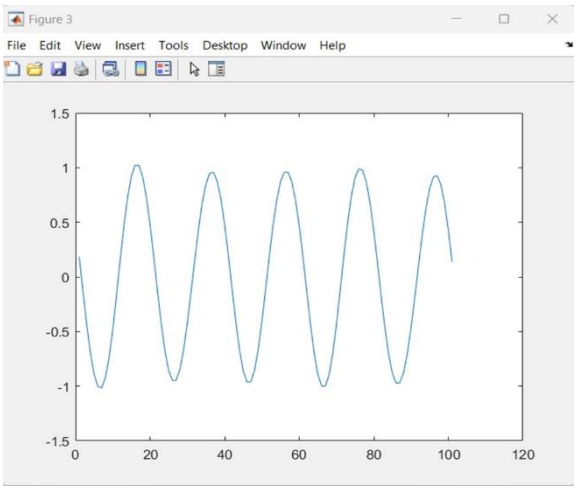


Fig.7. Extracted original signal using low pass filter

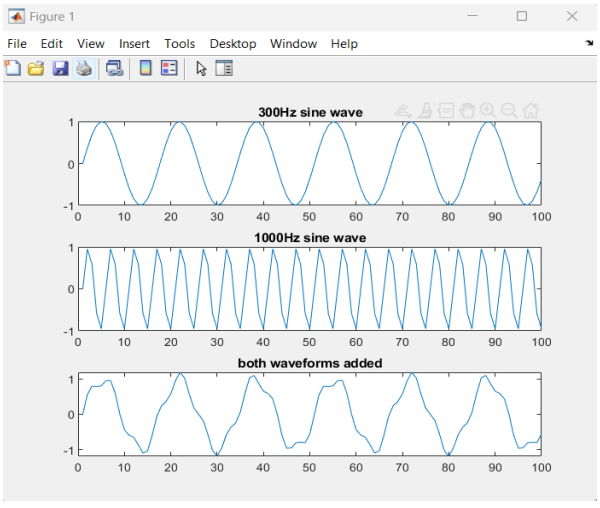


Fig.8. 300Hz and 1000Hz waveforms and these are added to form the distorted waveform

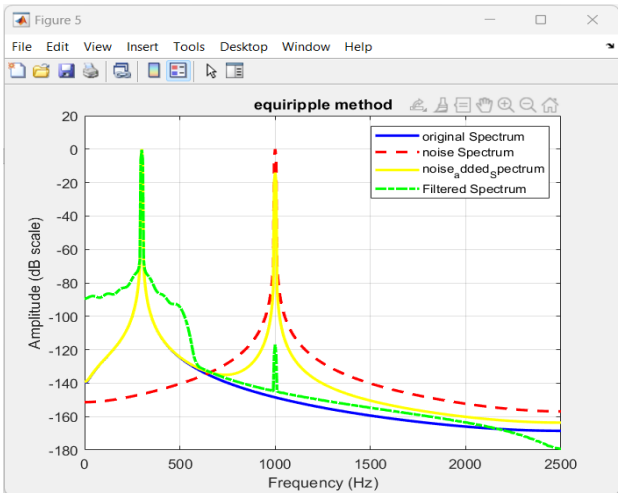


Fig.9 Spectrum of input and output signals FIR filter designed in equiripple method

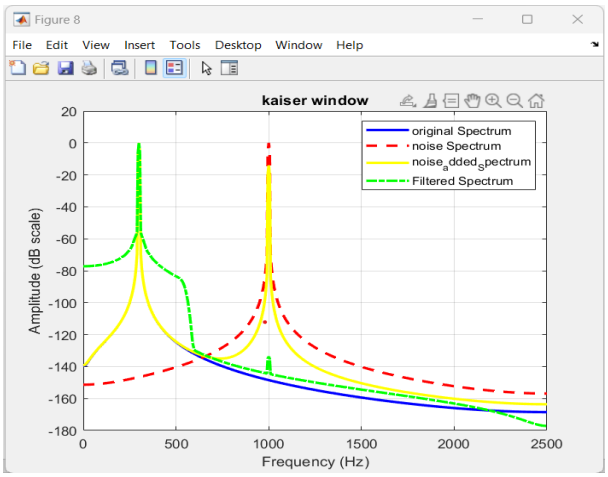


Fig .10 Spectrum of input and output signals of FIR filter designed using kaiser window

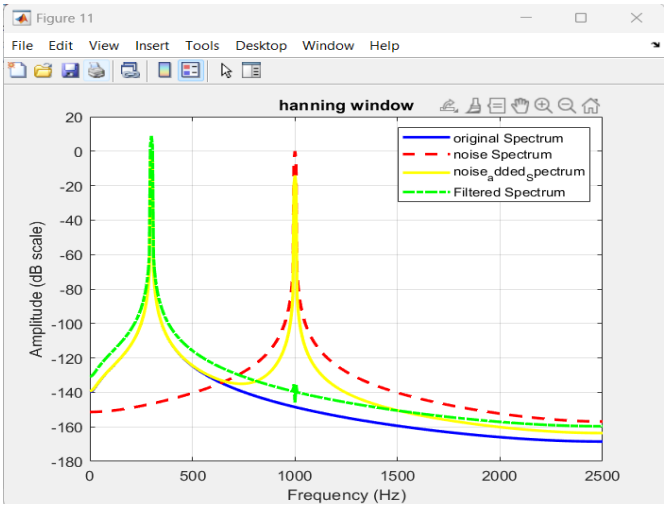


Fig.11 Spectrum of input signals of FIR filter designed using hanning window

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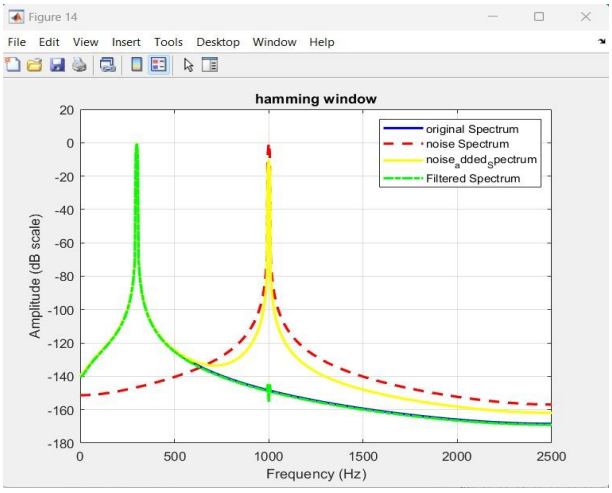


Fig.12 Spectrum of input and output signals of FIR filter designed using hamming window

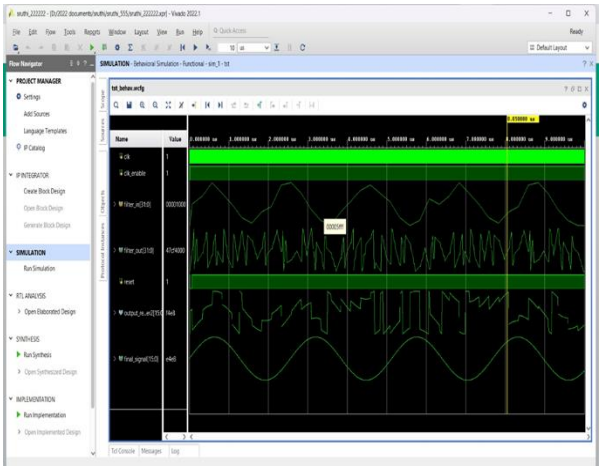

Fig .13. Verilog implementation of DA based FIR filter

I. Table .Comparison of Existing method and proposed method with power

| Design | Filter length | Power(W) |
|---|---|---|
| Allred [12] | 16 | 24.39 |
| R.Guo [10] | 16 | 21.36 |
| Meher [11] | 16 | 12.08 |
| Sang Yoon [8] | 16 | 9.41 |
| proposed | 16 | 7.965 |

## VI. CONCLUSION

In this paper a basic design of adaptive FIR filter to remove the noise with low power and low area. The conventional adaptive FIR filter the adder-based shift accumulation is replaced by compressor adder are used to reduce area and the critical path is large to obtain filter response so pipelined concept are introduced in the Least Mean Square algorithm (LMS). It was analysed the value of outputs are changing when the clock is changing. The designed are executed using Verilog coding along with the test bench. This framework was executed in Xilinx Vivado using Verilog coding and test bench for the design also introduced in order to test the design, to make the things more clears and illustrative the simulations waveforms and finally implemented on the board Xilinx Artix 7 FPGA. Then analysed the power consumption, area and Signal-to-noise ratio. And is suitable for all signal processing applications such as audio, biomedical, radar etc.

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