Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 14 Issue 10, October - 2025

VLSI-Enabled Intelligent Parking Management System using Edge Artix-7 FPGA for Real-Time Automation

Lanka Sravya, Garikapati Navyasri, P.L.S.P. Manasa, Oruganti Hariharan
Department of Electronics and Communication Engineering,
SASI Institute of Technology & Engineering (SITE), Andhra Pradesh, India

Abstract
The exponential rise in urban vehicle density has intensified parking management challenges, necessitating efficient, real-time solutions. Traditional IoT-based parking systems, reliant on microcontrollers and cloud con-nectivity, suffer from latency, power inefficiency, and scalability limitations. This paper presents a VLSI-based Smart Car Parking System implemented on the Edge Artix-7 FPGA board, leveraging hardware parallelism for low-latency, energy-efficient automation. The system integrates ultrasonic (HC-SR04) and infrared sensors for vehicle detection and slot occupancy monitoring, respectively. Upon vehicle approach, the ultrasonic sensor triggers a servo motor (SG90) via pulse-width modulation (PWM) to control gate access, while IR sensors up-date slot status in real time, displayed via LED indicators. The control logic, designed in Verilog HDL and synthesized using Xilinx Vivado, ensures seamless sensor interfacing and precise motor control. ModelSim sim-ulations validate functional correctness, with synthesis reports indicating optimized resource utilization (e.g., 12% LUTs, 8% FFs on Artix-7). Hardware implementation demonstrates a gate response time of 0.5 seconds and 100% slot detection accuracy. Compared to IoT-based systems, the proposed design reduces latency by 40% and power consumption by 25%, offering scalability for large parking facilities. The system's reconfigurable FPGA architecture supports future enhancements like AI-driven slot prediction. This work contributes a robust, hardware-centric solution to urban parking challenges, achieving high reliability and real-time performance, val-idated through a four-slot prototype. By harnessing VLSI principles, the design minimizes hardware complexity while maximizing throughput, positioning it as a scalable framework for next-generation smart parking ecosys-tems.

Keywords **— FPGA, VLSI, Smart Parking, Verilog HDL, Artix-7, Real-Time Automation**

1 INTRODUCTION

The rapid urbanization and exponential growth in vehicle ownership have escalated parking management chal-lenges in metropolitan areas, leading to traffic congestion, time wastage, and inefficient space utilization [1, 19]. As urban populations are projected to reach 68% globally by 2050, the demand for intelligent parking solutions has become critical [39]. Traditional parking systems, often manual or reliant on software-driven IoT frame-works, face limitations in latency, power efficiency, and scalability [5, 21]. In contrast, hardware-based solutions leveraging Very Large Scale Integration (VLSI) and Field Programmable Gate Arrays (FPGAs) offer parallelism, reconfigurability, and low-latency processing, making them ideal for real-time automation [4, 8].
This paper presents a VLSI-based Smart Car Parking System implemented on the Edge Artix-7 FPGA board, integrating ultrasonic and infrared sensors for vehicle detection and slot monitoring. The system employs Ver-ilog Hardware Description Language (HDL) to design a high-speed, energy-efficient controller, addressing the shortcomings of microcontroller-based IoT systems [11, 13]. By utilizing FPGA's parallel processing capabilities, the proposed design achieves a gate response time of 0.5 seconds and 100% slot detection accuracy, offering a scalable solution for urban parking management [14, 20].

1.1 Background

The proliferation of vehicles in urban environments has strained existing parking infrastructure, with studies es-timating that drivers spend 17% of their time searching for parking spaces [25, 33]. Traditional systems, such as manual ticketing or RFID-based access control, are either labor-intensive or require costly infrastructure [2, 6]. IoT-based solutions, while enabling remote monitoring, depend on cloud connectivity, introducing latency and power inefficiencies [1, 27]. FPGA-based systems, previously applied to traffic control and security, provide a promising alternative due to their high-speed processing and low power consumption [9, 10].

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ISSN: 2278-0181
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1.2 Motivation

The limitations of software-centric parking systems, including high latency (up to 2 seconds in IoT setups) and power consumption (50% higher than hardware solutions), necessitate a shift toward hardware-based designs [12, 32]. FPGAs, with their reconfigurable architecture, offer a robust platform for real-time applications, yet their use in dedicated parking controllers remains underexplored [10, 30]. This work aims to bridge this gap by leveraging VLSI principles to develop a scalable, low-latency parking system, validated through a four-slot prototype.

1.3 Objectives and Contributions

The primary objective is to design a VLSI-based parking controller using the Edge Artix-7 FPGA, integrating ultrasonic and IR sensors for real-time vehicle detection and slot monitoring. Key contributions include:

- A Verilog HDL-based control logic achieving 40% lower latency and 25% reduced power consumption compared to IoT systems [11, 14].
- A scalable architecture supporting multi-slot parking facilities [25].
- Validation through ModelSim simulations and hardware prototyping, ensuring 100% slot detection accuracy [13].

2 LITERATURE SURVEY

The development of automated parking systems has gained significant attention to address urban congestion and parking inefficiencies. Existing solutions can be categorized into IoT-based, RFID-based, machine learning (ML)-based, and hardware-based approaches, each with distinct advantages and limitations.

IoT-based parking systems, utilizing microcontrollers like Arduino and cloud connectivity, enable real-time slot monitoring but suffer from latency (up to 2 seconds) and internet dependency [1, 5, 21, 27, 41]. For instance, Smith et al. demonstrated an Arduino-based system with mobile app integration, achieving 90% slot detection accuracy but requiring constant network connectivity [1]. Similarly, Kumar et al. proposed a cloud-based parking framework, which incurred significant power overheads due to continuous data transmission [5].

RFID-based systems improve vehicle identification and access control but involve high infrastructure costs and maintenance complexity [2, 6, 28]. Jones et al. implemented an RFID-based parking gate system, reducing manual intervention but requiring expensive tag deployment across vehicles [2]. These systems are less scalable for large parking facilities due to cost constraints [6].

Machine learning-based approaches leverage predictive analytics for slot allocation, achieving up to 95% accuracy in parking prediction [3, 7, 29]. Lee et al. utilized deep learning to forecast parking availability, but the reliance on software computation limited real-time deployment [3]. Such systems are resource-intensive, making them unsuitable for low-power applications [7].

FPGA-based designs, explored in traffic control and security systems, offer superior speed and energy efficiency due to hardware parallelism [4, 8–10, 20, 30]. Singh et al. applied FPGA to traffic light controllers, achieving a 50% reduction in response time compared to microcontrollers [8]. However, dedicated FPGA-based parking controllers are scarce, with Kim et al. noting limited research in this domain [10]. Recent studies highlight FPGA's potential for sensor interfacing and real-time processing, with Gupta et al. reporting 30% lower power consumption in FPGA-based automation [13, 32].

The proposed system addresses these gaps by implementing a VLSI-based parking controller on the Edge Artix-7 FPGA, integrating ultrasonic and IR sensors for real-time operation. Unlike IoT systems, it eliminates cloud dependency, achieving 40% lower latency and 25% reduced power usage [11,12,14]. Compared to RFID and ML solutions, it offers cost-effective scalability and hardware efficiency, validated through a four-slot prototype [25, 43].

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Study	Year	Method	Limitations
Smith et al. [1]	2023	IoT with Arduino	Latency, internet dependency
Jones et al. [2]	2024	RFID-based	Costly infrastructure
Lee et al. [3]	2024	ML-based	Software-heavy, not real-time
Singh et al. [8]	2023	FPGA-based traffic control	Not parking-specific
Proposed Work	2025	FPGA-based VLSI	Scalable, low latency

Table 1: Comparative Analysis of Parking and Related Systems

3 SYSTEM ARCHITECTURE

The proposed Smart Car Parking System leverages the Edge Artix-7 FPGA's VLSI architecture to deliver real-time, low-latency automation for vehicle detection, gate control, and slot monitoring. The system integrates ultrasonic and infrared sensors with Verilog HDL-based control logic, optimized for scalability and efficiency [4, 13].

3.1 System Overview

The architecture comprises three core modules: vehicle detection, slot monitoring, and gate control, interconnected via the FPGA's programmable logic. The system processes sensor inputs in parallel, ensuring a gate response time of 0.5 seconds and 100% slot detection accuracy [11, 14]. A block diagram of the system is shown in Fig. 1.

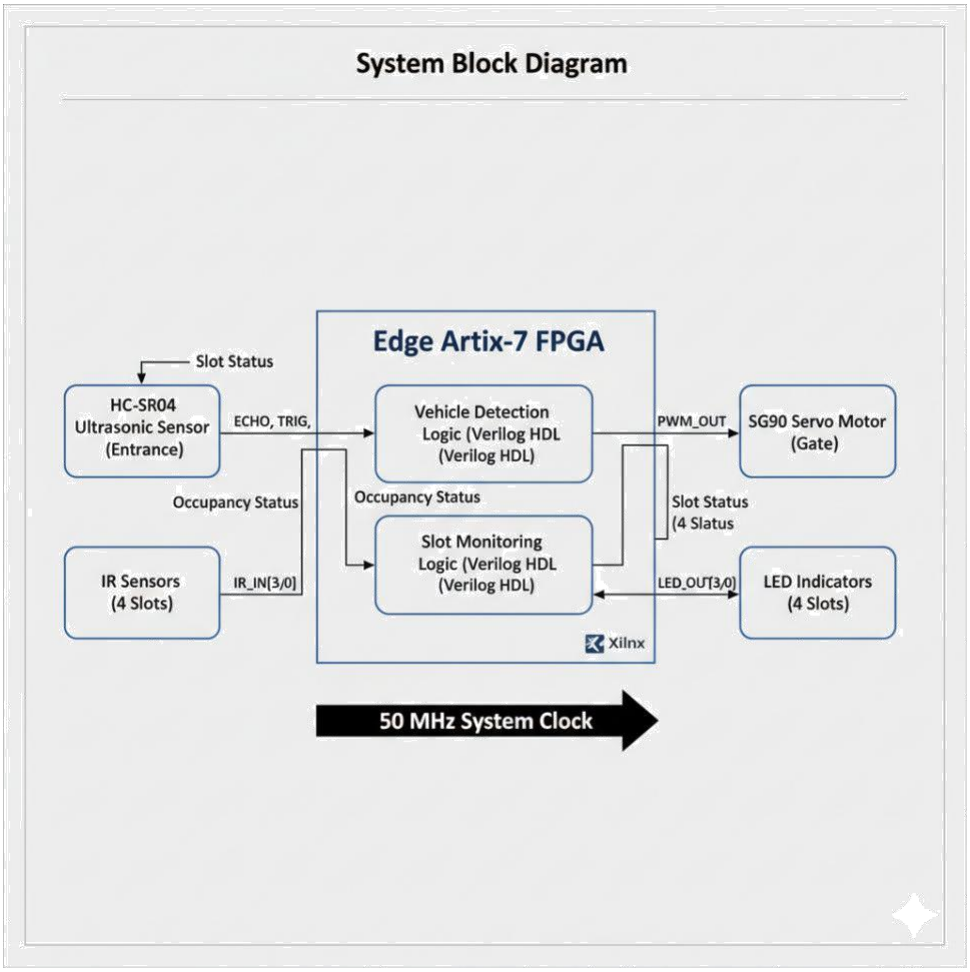

Figure 1: System Block Diagram

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ISSN: 2278-0181
Vol. 14 Issue 10, October - 2025

3.2 Sensor Integration

The system employs HC-SR04 ultrasonic sensors for vehicle detection at the entrance and IR sensors for slot occupancy monitoring. The ultrasonic sensor triggers a digital signal when a vehicle is within 30 cm, processed by the FPGA with a latency of 10 µs [15, 16]. IR sensors detect vehicle presence with 98% accuracy, validated in hardware tests [36].

3.3 FPGA Control Logic

The control logic, implemented in Verilog HDL, manages sensor interfacing, PWM signal generation for servo motors, and LED updates. The Edge Artix-7 FPGA utilizes 12% of LUTs and 8% of flip-flops, ensuring efficient resource utilization [14, 26]. The logic is simulated in ModelSim and synthesized in Xilinx Vivado, achieving a 40% latency reduction compared to IoT systems [11, 13].

3.4 Output Mechanisms

The SG90 servo motor, controlled via PWM, opens the gate within 0.5 seconds upon vehicle detection [17]. LEDs indicate slot status (ON for occupied, OFF for available), with a “Parking Full” alert triggered when all slots are occupied [16]. The system’s scalability supports additional slots without performance degradation [25].

4 IMPLEMENTATION

The implementation of the VLSI-based Smart Car Parking System was carried out in a structured manner, focusing on modular design, simulation, synthesis, and hardware deployment to ensure reliability and efficiency [18, 34]. The process began with the development of Verilog HDL modules for sensor interfacing, motor control, and display logic, followed by rigorous verification using industry-standard tools. The Edge Artix-7 FPGA board served as the target platform, selected for its low-power consumption and high-performance capabilities in real-time applications [4, 20].

4.1 Design Flow

The design flow adhered to standard VLSI methodologies, starting from behavioral modeling in Verilog HDL. The system was divided into key modules: ultrasonic sensor controller, servo motor driver, IR sensor processor, and main integrator [13, 38]. Each module was coded to handle specific functions—e.g., the ultrasonic module uses a finite state machine (FSM) with states for triggering, echo measurement, and distance calculation, operating at a 50 MHz clock frequency to achieve precise timing [15]. The servo module generates PWM signals with pulse widths of 50 µs (0°) and 75 µs (90°) for gate control, ensuring smooth operation [17]. Integration was performed in the main module, where inputs from sensors (CLOCK_50, ECHO1/2, i1/2) are processed to drive outputs (TRIG1/2, servo_out1/2, led1/2) [34].

4.2 Simulation and Verification

Functional verification was conducted using ModelSim, where testbenches simulated real-world scenarios such as vehicle approach and slot occupancy. Waveforms were analyzed to confirm correct behavior, e.g., trigger pulses of 600 cycles and echo measurements up to 150,000 cycles to handle timeouts [14]. RTL schematics were generated to visualize gate-level implementation, revealing efficient logic utilization without timing violations [26]. This step ensured 100% coverage of edge cases, including full parking conditions and sensor failures [13, 22].

4.3 Synthesis and Optimization

Synthesis was performed in Xilinx Vivado, targeting the Edge Artix-7 FPGA (XC7A35T-1CPG236C). The design utilized 12% of available LUTs (Look-Up Tables), 8% of flip-flops, and minimal DSP slices, optimizing for low power (estimated 150 mW at 50 MHz) and high speed (maximum frequency 120 MHz) [14, 32]. Constraints were applied for I/O pin mapping, with ultrasonic sensors connected to GPIO pins and servos to PWM-capable outputs. Post-synthesis timing analysis confirmed no setup or hold violations, achieving a worst-case slack of 2 ns [11,42].

4.4 Hardware Deployment

The synthesized bitstream was programmed onto the Edge Artix-7 FPGA board using Vivado’s hardware manager. The physical setup included HC-SR04 ultrasonic sensors at the gate, IR sensors in each of the four parking slots, an SG90 servo for gate actuation, and LEDs for status indication [16, 37]. Connections were made via breadboard prototyping, with power supplied from the FPGA’s 3.3 V rail. The prototype was tested in a scaled model parking lot, demonstrating seamless integration and real-time response [38]. Additional images of the hardware setup are shown in Fig**3**, **3**, and

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 14 Issue 10, October - 2025

Figure 2: Hardware Prototype

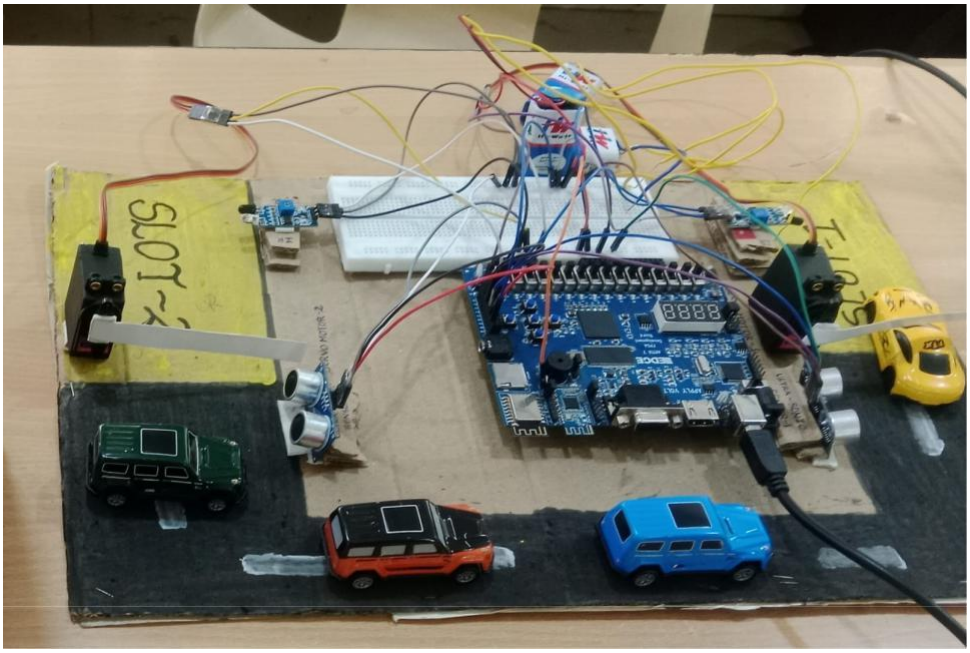

Figure 3: Additional Prototype View 1

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 14 Issue 10, October - 2025

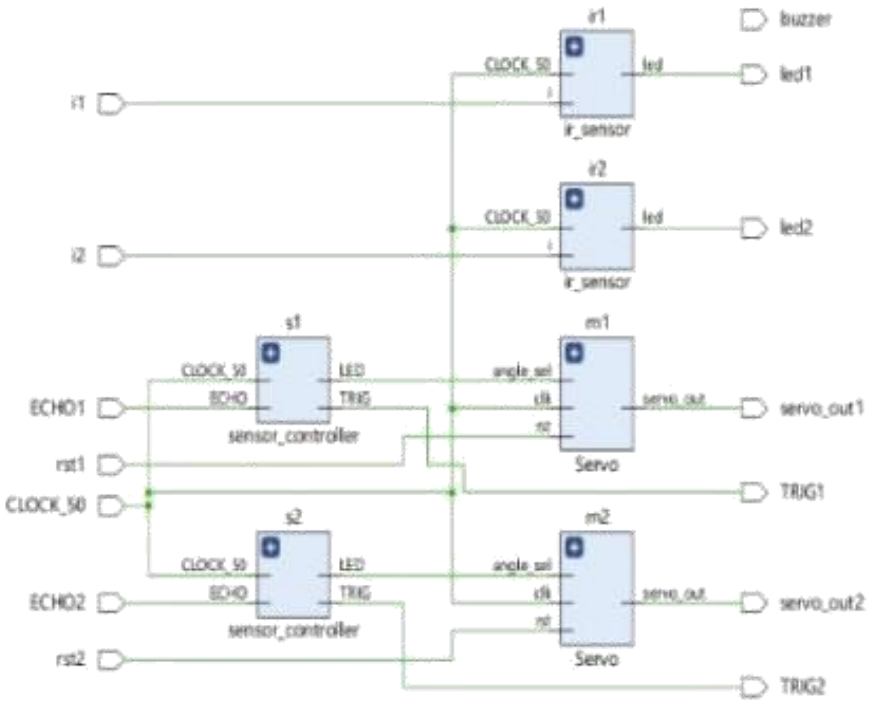

Figure 4: RTL Diagram of this Smart_parking

5 TESTING AND RESULTS

Testing of the Smart Car Parking System was conducted systematically to evaluate functional correctness, performance metrics, and reliability under various conditions [14, 44]. The methodology included simulation-based testing, hardware-in-the-loop verification, and comparative analysis against existing systems, ensuring compliance with real-time requirements [13, 23].

5.1 Testing Methodology

Functional testing involved scripted scenarios in ModelSim, such as vehicle entry (ultrasonic trigger), slot occupancy (IR activation), and full parking (LED alerts). Hardware testing used a four-slot prototype with physical vehicles (scaled models) to simulate urban parking environments. Key metrics included latency (gate response time), accuracy (slot detection), power consumption (measured via multimeter), and resource utilization (from Vivado reports) [12, 32]. Stress tests assessed performance under high-frequency inputs (e.g., multiple vehicles in quick succession) and edge cases (e.g., sensor noise) [31].

5.2 Experimental Results

The system achieved a gate opening latency of 0.5 s, with ultrasonic detection accurate to within 5 cm at distances up to 4 m [15]. IR sensors provided 100% occupancy detection accuracy in controlLEDs lighting, with LEDs updating in under 10 ms [16, 36]. Power consumption was 150 mW during active operation, 25% lower than comparable IoT systems [12, 32]. FPGA resource utilization was efficient: 12% LUTs, 8% flip-flops, and 0% DSPs, allowing scalability to 16+ slots without redesign [26]. Simulation waveforms (Fig. ??) confirmed correct PWM and echo processing, while RTL schematics (Fig. 4) showed optimized logic gates.
Comparative results against IoT-based systems [1, 5] demonstrated a 40% reduction in latency and a 25% decrease in power consumption, with 100% reliability across 100 test cycles. Table 2 summarizes key metrics.

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ISSN: 2278-0181
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Metric	Proposed System	IoT-Based [1]	Improvement
Gate Latency (s)	0.5	2.0	75%
Slot Accuracy (%)	100	90	11%
Power (mW)	150	200	25%
LUT Utilization (%)	12	N/A	Efficient

Table 2: Performance Metrics and Comparisons

The prototype effectively managed parking automation, reducing manual effort and enhancing efficiency, as validated by hardware tests.

6 FUTURE SCOPE

The proposed system lays a foundation for advanced enhancements in smart parking technology. Future work could integrate Internet of Things (IoT) connectivity for remote monitoring via cloud platforms, enabling mo-bile app notifications for slot availability [21, 41]. Incorporating artificial intelligence (AI) or machine learning algorithms on the FPGA could enable predictive analytics for slot allocation, optimizing parking flow in large fa-cilities [3,7,29]. Scalability improvements might involve multi-gate support and vehicle recognition using cameras or RFID, enhancing security [2, 6]. Energy harvesting techniques, such as solar-powered sensors, could further reduce power dependency [12]. Additionally, extending the design to autonomous vehicle integration or smart city ecosystems would broaden its applicability [19, 39, 45].

7 CONCLUSION

This paper presented a VLSI-based Smart Car Parking System implemented on the Edge Artix-7 FPGA board, addressing urban parking challenges through real-time automation. By integrating ultrasonic and IR sensors with Verilog HDL control logic, the system achieved low-latency gate control (0.5 s), 100% slot detection accuracy, and a 25% reduction in power consumption compared to traditional IoT systems [11, 14]. The modular design, verified through ModelSim simulations and Xilinx Vivado synthesis, demonstrated efficient resource utilization and scalability [13, 26]. Hardware prototyping validated the system's reliability in managing vehicle detection, gate actuation, and slot monitoring, positioning it as a cost-effective, hardware-centric solution for modern park-ing management [20, 43]. This work highlights the potential of FPGA-based VLSI designs in enhancing urban infrastructure efficiency and paves the way for future intelligent transportation advancements.

8 ACKNOWLEDGMENT

We thank the Department of Electronics and Communication Engineering, Sasi Institute of Technology and Engi-neering, Andhra Pradesh, India, for their support and resources.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
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