VLSI Architectures for the 2-D Daubechies-4 and Daubechies-6 Wavelet Filters using Algebraic Integers

Nagarjuna K
M.Tech VLSI design and embedded system
T john institute of technology
Bangalore

Mohan H M
Asst. Professor E & C.
T john institute of technology
Bangalore

***Abstract*— The project proposes a novel algebraic integer (AI) based multi encoding of Daubechies-4 and Daubechies-6 2D wavelet filters having error free integer based computation. Digital VLSI architectures employing and working parallel channels are being proposed. The multi encoded AI framework allows a multiplication free and computationally accurate architecture. It provides a noise free computation throughput and the multi-level, multi rate 2D filtering operation. A single final reconstruction step furnishes filtered and down sampled image outputs in fixed-point, resulting in low levels of image noise. It Compares between Daubechies-4 and Daubechies-6 designs in terms of SNR, PSNR, and hardware structure, and power consumptions, for different word lengths. Further, FRS designs based on canonical signed digit representation and on expansion factors are proposed with dynamic power consumption which will be verified on FPGA chip using an ML605 platform.**

Keywords—Algebraic integer encoding, daubechies wavelets, error-free algorithm, fixed-point scheme, sub-band coding, VLSI.

I. INTRODUCTION

The field of discrete wavelet transforms (DWT) has been great interest in wavelets is not only partly due to their ability to efficiently represent functions with localized features, but also due to the wavelet analysis being capable of decomposing a signal into a particular set of basis functions. They have a good spectral properties to the fact that it was discovered that some wavelets might be implemented in an extremely computationally efficient manner. Just as fast Fourier transform (*FFT*) algorithms made the Fourier transform a practical tool for spectral analysis, the multi-resolution analysis has made the discrete wavelet transform (*DWT*) a viable tool for computational time-scale analysis. DWT based multi-resolution analysis leads to both time and frequency localization.

A Daubechies wavelets are well-suited and commonly used in image compression applications. Herein we refer to the Daubechies wavelets generated from 4- and 6-tap filter banks as Daub-4 and -6 wavelets, respectively. Whereas the Daub-4 wavelets are often employed in applications where the signals are smooth and slowly varying, the Daub-6 wavelets are used for signals bearing abrupt changes and having high undesired noise levels. Daub-4 wavelets can be highly localized to smooth and Daub-6 wavelets have found applications in medical imaging.

we propose a new multi-encoding technique in this project. That achieves exact computation of multi-level 2-D Daubechies wavelet transforms using algebraic integer encoding. Compared to existing AI designs in literature, the proposed design can compute wavelet image approximations entirely over integer fields and with a single FRS in a purely AI based 2-D architecture. The design avoids the need of intermediate reconstruction steps.

Moreover, the proposed architecture is sought to be multiplier free. Such design facilitate speed, relatively smaller area on chip as well as cost of design. The new design is multi-encoded and multi-rate, operating over AI with no intermediate reconstruction steps. In this implementation, a error-free computations can be performed until the final FRS. Our architecture emphasizes on quality of output image and speed and power consumption for accuracy.

II. LITERATURE SURVEY

Algebraic integer based low power high speed Daubechies wavelet filter using VLSI architecture. Here it explains the error-free integer-based computation using AI based multi-encoding of 2-D Daubechies wavelet filters and it explains multiplication-free and computationally accurate architecture. This paper mainly guarantied noise-free computation throughput using 2-D filtering operation. SNR & PSNR improvements are approximately 41% only [1].

Digital image processing by S Jayaraman, image processing plays an important role in daily life application. Such as computer graphics, computer tomography, satellite television tec. So the study of image process Is very important for digital world. Basically image is a numerical representation of the object[2].

VLSI architecture design for Bi-orthogonal wavelet filter using algebraic integer encoding, here flexible architecture were introduced for algebraic integer based Bi-orthgonal wavelet filter. The Bi-orthogonal wavelet filter are very useful in medical field, it quantized before implementations performance uses less shifts & additions, it provides improvement in fixed point representation because of this architecture shows better performance in reducing chip area[3].

FPGA implementation of efficient for fixed point 1-D discrete wavelet transform using lifting scheme, explains high speed pipeline & design of area efficient based on VLSI

architecture of 1-D DWT, this paper scheme is to reduce the clock cycle area of efficient on hardware resource it needs a fixed point representation[4].

FPGA implementation of FIR filter using distributed arithmetic architecture for DWT. This paper explains fast 1-D DWT on parallel FIR filter & presents hardware architecture reduction using 2-D DWT using lifting scheme results are combined to reduce the registers for these it needs 2 input and 2 output parallel scanning architecture. This needs parallel FIR filter structure & also this paper explains brief about DWT implemented in VHDL. It uses FPGA technology for various threshold technique[5].

III. CONTRIBUTIONS

A. The Problem of Fixed-Point Errors

Filter banks associated to Daubechies wavelets have irrational coefficients whose representation in fixed-point requires truncation. Such approximations introduce representation errors which propagate through a given filter bank. The required filter bank is, the computational error may become. This effects a lower obtained signal-to-noise of the resulting data.

B. Prior Art on AI-Based DWT

A algebraic integers encoding can address the computational noise injection in DWT analysis.AI quantization has been employed in many signal processing schemes, including wavelet and DCT analysis. A significant advantage of the AI encoding is having capability of mapping the required irrational wavelet coefficients into a vectors of integers. Thus, the irrational coefficients of the Daubechies filters can be represented into arrays or integers.

AI encoding schemes require a reconstruction step to convert the resulting AI encoded quantities back into fixed-precision binary. The design of digital architectures for the one Dimension Daub-4 and -6 filters were in the recent past. Whereas in the 2-D architectures require intermediate reconstruction steps that map the AI encoded transform coefficients back into fixed-point format. These are one Dimension DWT architectures that compute the 2-D DWT by repeated use of a one Dimension AI-encoded architecture. This IRS is located after the first application of the transform before submitting the resulting data to the next stage. When multi-level decompositions are attempted. Errors incurred in the intermediate reconstructions mitigate the benefits of using AI encoding for 2-D multi-level DWTs. This is an outstanding problem in the current literature which we identify and correct in the present contribution.

C. According to the base paper

Filter Filter banks associated to Daubechies wavelets have irrational coefficients whose representation in fixed-point requires truncation or rounding off. Such approximations introduce representation errors which propagate through a given filter bank. the longer the required filter bank is, the greater the computational error may become. This process effects a lower obtained signal-to-noise of the resulting data. Minimum operating frequency, signal-to-noise ratio (SNR) and peak-signal-to noise ratio (PSNR) figures are sought using the proposed designs operating in fixed-point. The overall system power consummation is more and performance is less. In my project I will try to find out the solutions for the above mentioned problems.

VI. REVIEW OF SUB-BAND CODING

The wavelet decomposition of input image data can be accomplished by sub-band coding. A 2-D FIR filter bank processes the input image data resulting in an approximation and detail sub-images.

1. Single application of the 2-D wavelet filter bank

After each iteration a coarser approximation can be achieved. Let the original image to be analyzed be denoted by An-1. Computes the approximation data. Detail information data Dvn,Dhn and Ddn are normally discarded or thresholded in data compression applications.

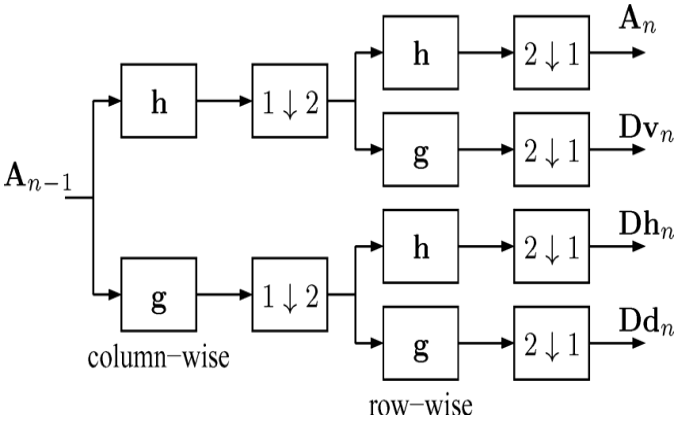

Fig.1. Diagram of a single application of the 2-D wavelet filter bank.

2. Recursive application of the 2-D wavelet filter bank

The recursive diagram of the multi-level wavelet analysis. After each set of filter banks & a coarser approximation, is furnished. Each level also produces the detail information.

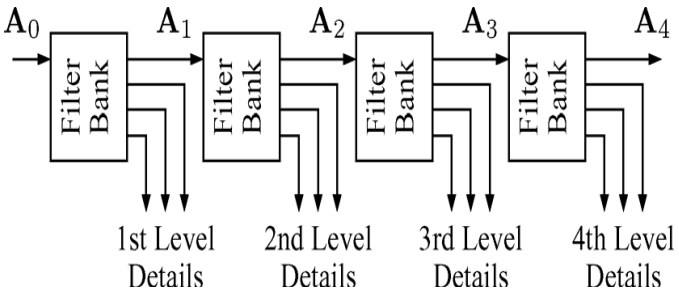

Fig.2. Recursive application of the 2-D wavelet filter bank.

3. Single AI filter bank decomposition

In this single AI filter bank decomposition. Let the original image data to be analyzed be denoted by An-1. Computes the approximation data.

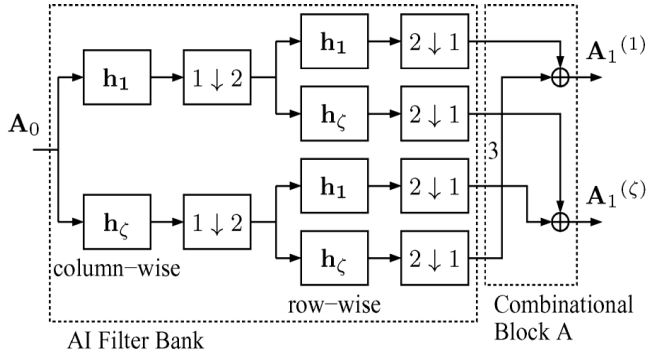

Fig. 3 Single AI filter bank decomposition.

4. Multi-level AI filter bank with final reconstruction step

In this Multi AI filter bank operates entirely over the AI representation up to a single and final reconstruction block without any intermediate reconstruction steps. The FRS is the only possible source of computational errors.

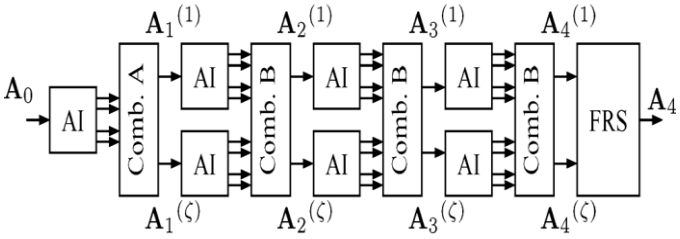

Fig.4. multi-level AI filter bank with final reconstruction step.

VI. FINAL RECONSTRUCTION STEP

The proposed AI-based daubechies wavelet analyses based Daub-4 and -6 filter banks are entirely over extended integer fields. The AI encoded approximations must be converted back to again a standard fixed- point representation.

We proposed two approaches for the Final Reconstruction Step design. They are (i) Canonical signed digit(CSD) representation and (ii) Expansion Factor Method.

TABLE I

COMPARISON OF DAUB-4 AND DAUB-6 PERFORMANCE

Aspect	Daub-4	Daub-6	Proposed
FPGA	Xilinx Virtex-6	Xilinx Virtex-6	Xilinx Virtex-6
Target Device	Vcx240t-1ff1156	Vcx240t-1ff1156	Vcx240t-1ff1156
Max Freq	442.47	274.72	327.600MHz
CPD	2.26	3.64	2.040ns
# Adders	32	61	23
Registers	258	765	421

TABLE II

RESOURCE CONSUMPTION FOR PROPOSED DAUB-6 ARCHITECTURE

Resources	Daub-4	Daub-6
Slices	3669	1161
LUTs		1149
CPD	5.44	2.040ns
Ma. Frequency(MHz)	183.80	327.600

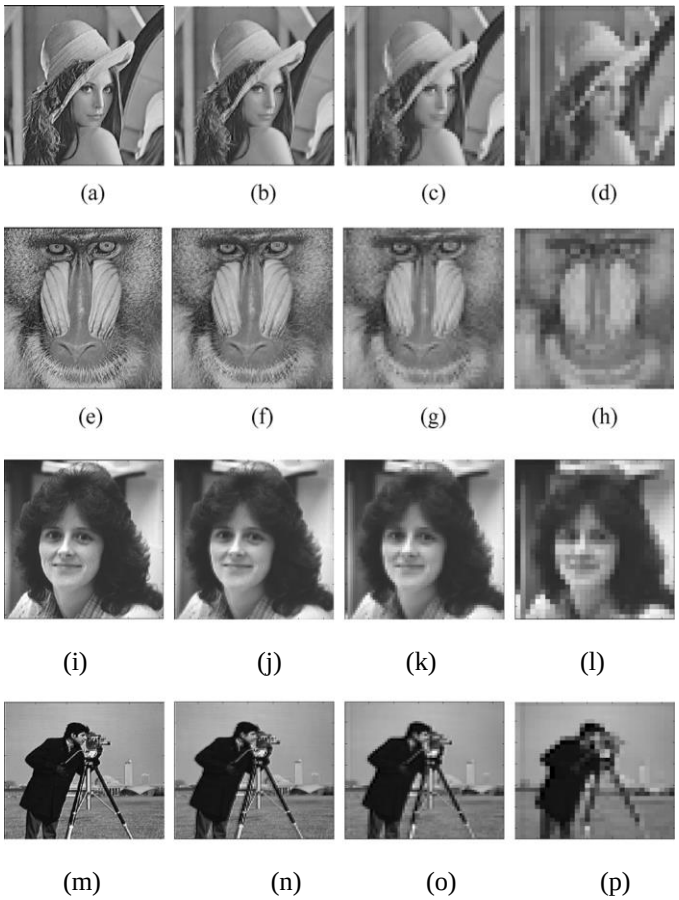

Fig. 5. Approximation sub-images A_1,A_2,A_3,and obtained from on-chip physical verification on a Virtex-6 vcx240t-1ff1156.(a)A_1,(b)A_2,(c)A_3,(d)A_4,(e)A_1,(f)A_2,(g)A_3,(h)A_4,(i)A_1, (j)A_2,(k)A_3,(l)A_4,(m)A_1,(n)A_2,(o)A_3,(p)A_4.

VI. FPGA IMPLEMENTATION AND RESULTS

The architectures for Daub-4 and -6 filter banks were implemented on Xilinx Virtex xc6vcx240t-1ff1156 device using the ML605 evaluation board. The designs were tested with three different standard images obtained from . Gray 64 × 64 images Woman and Cameraman to the Daub-4 filter banks whereas Mandrill were sub- mitted to the Daub-6 filter banks. Hardware results were verified with MATLAB. Fig. 6 displays hardware results from the Xilinx FPGA for

TABLE.III
COMPARISON OF PROPOSED ARCHITECTURE WITH EXISTING 2-D DWT ARCHITECTURE

`	Tze-Yun	Marino	Po-Chih	Bing-Fei	Hongyu	Kishore	Zhang	This paper	Proposed
wavelet	Daub-4	N/A	9/7	5/3,9/7	9/7	5/3,9/7	9/7	Daub-4/6	Daub-4/6
Multiplexers	Yes	No	No	No	No	No	No	Yes	Yes
DWT/IDWT	DWT/IDWT	DWT	DWT	DWT	DWT	DWT	DWT	DWT	DWT
Technology	Xilinx XC2V4000	N/A	N/A	CMOS 0.25um	Virtex-II XC2V250	CMOS 0.18um	Xilinx xc2v500	Xilinx xc6vcx240t	Xilinx xc6vcx240t

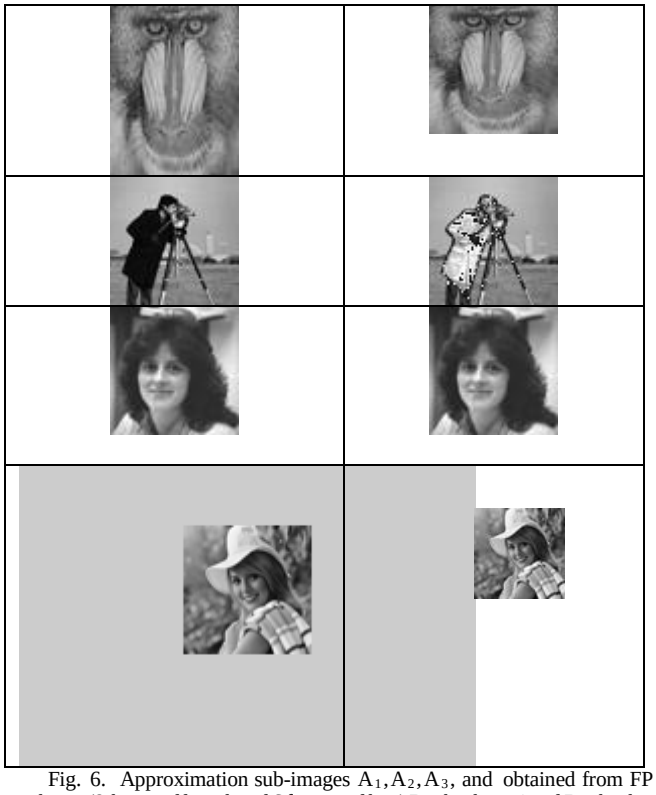

Fig. 6. Approximation sub-images A_1, A_2, A_3, and obtained from FP scheme (8-bit word length and 6 fractional bits) Daubechies -4 and Daubechies -6 wavelet filters.

the Daub-4 and -6 filter banks. Table VI shows a performance comparison among proposed Daub-4 and -6 architectures for single level decomposition of 8-bit Lena image.

For comparison, we devised a version of the proposed system that operates over fixed-point arithmetic instead of AI-based arithmetic. For such, we employed 8 bits for word size with 6 fractional bits. In this case, the required filter banks were implemented by quantizing the exact filter coefficients into the fixed-point representation. Notice that the fixed-point scheme incurs coupled quantization noise, whereas the AI-based architecture is immune to this source of contamination. Fig. 6 shows the results for the fixed-point design.

A. *Resource Consumption and Figures of Merit*

The AT product is a standard performance metric in digital hardware designs. It refers to chip-area and maximum frequency (speed) of the design. Lower Area – time product values indicate a higher speed of operation. In an PGA, the area (A) is provided by the number of slice LUTFs used for logic given by the FPGA de- sign tool called XFLOW and the time is simply the critical path delay. Quantity AT2 is useful, when clock speed is the driving factor of design optimization, for high-throughput realizations. Table III shows the estimated power. consumption for the Daub-4 and -6 filter banks. The SNR and peak PSNR were adopted as figures of merit.

B. *Comparison With Existing Methods*

A significant amount of work is published on 1-D and 2-D DWT VLSI architectures. The proposed designs address the Daub-4 and -6 wavelet analysis. Also detailed data is re- ported in [3], [6] allowing us to derive meaningful comparison

Considering 8-bit input word length, the obtained SNR and PSNR values for proposed architectures higher than the 1-D and 2-D DWT architectures.

Among the FRS approaches we have mentioned, Moreover, we compared the proposed architectures with several prominent VLSI 2-D DWT designs archived in literature. In particular, we separated the following works:

To compare with other architectures, PSNR values presented for proposed Daub-4 and -6 architectures, were obtained by employing reconstructions between column and row transforms, whereas the PSNR values in Table V are entirely 2-D based with single final reconstruction step.

TABLE IV
DAUB-4 AND DAUB-6 ISE XPOWER RESULTS

Device		On-Chip	Power (W)	Used	Available	Utilization (%)
Family	Virtex6	Clocks	0.000	1	--	--
Part	xc6vlx240t	Logic	0.000	522	150720	0
Package	ff1156	Signals	0.000	867	--	--
Temp Grade	Commercial	IOs	0.000	44	600	7
Process	Typical	Leakage	3.409			
Speed Grade	-2	Total	3.409			

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.000	1.670	0.000	1.670
Vccaux	2.500	0.135	0.000	0.135
Vcco25	2.500	0.002	0.000	0.002
MGTAVcc	1.000	0.758	0.000	0.758
MGTAVtt	1.200	0.532	0.000	0.532

TABLE V
SNR AND PSNR FOR DAUB-4 AND DAUB-6 FILTER BANKS BASED ON FIXED-POINT AND AI ENCODING

Original Image(512x512)	**Resized Image(64x64) PSNR**	**Proposed PSNR**
Woman	39.84 dB	96.28 dB
Cameraman	34.69dB	67.70 dB
Mandril	35.27 dB	78.35 dB
Original Image(512x512)	**Resized Image(64x64) SNR**	**Proposed SNR**
Woman	38.84 dB	61.28 dB
Cameraman	31.72dB	60.97 dB
Mandril	33.20 dB	77.02 dB

VII. CONCLUSION

We proposed a multi-encoded AI-based 2-D wavelet filter Bank architecture capable of arbitrarily numerical accuracy. By employing AI encoding, resulting wavelet decomposed images had SNR and PSNR are improved. A single FRS is the only source of computational error. Noise Injection from intermediate fixed-point errors is non-existent.

We proposed several designs for the FRS based on CSD representation and expansion factor scaling. The SNR and PSNR values for the AI-based Daub-6 architecture were approximately 6–10% higher than the Daub-4 architecture. Due to its inherent simplicity of coefficients and smaller number of AI numbers, the Daub-4 AI- based architecture had consumed approximately half of the Daub-6 systems.Daub-4 and Daub-6 single level decomposition architectures were also FPGA prototyped with the Xilinx Virtex-6 device at 442.47 and 274.72MHz, respectively. In the presence of higher resolution and increased frame rate, there is no option but to increase the throughput of the digital filtering architectures. Finally AI based scheme can be applied to any type of DWT as long as the scaling and wavelet coefficients of the corresponding filters could be given and exact representation.

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