VLSI Architecture for Multilevel Inverters

Athira T. N
PG Scholar
Applied Electronics & Instrumentation
Younus College of Engineering & Technology
Kollam, India

Sarath Gopal
Assistant Professor
Electronics & Communication
Younus College of Engineering & Technology
Kollam, India

***Abstract*—The DC/AC power inverters constitute the major unit of the power generation systems implemented in renewable energy sources, AC motor drives, and UPS applications. The digital implementation of SPWM generator is executed through FPGA which makes it capable to operate at high switching frequencies with lower power consumption. The Total Harmonic Distortion reduction as well as better performance can be obtained through multilevel inverters. The complexity of multilevel circuit topologies will be high. This paper presents the simulation of a transistor clamped H-bridge multilevel inverter with reduced number of switches using phase disposition pulse width modulation technique. Simulation is verified through MATLAB Simulink and implemented using FPGA in XILINX ISE Design Suite 14.5. Phase Disposition pulse width modulation (PDPWM) technique is employed for generating pulses for multilevel inverters.**

Keywords—Sinusoidal Pulse Width Modulation (SPWM); Field Programmable Gate Array (FPGA); Multilevel inverter; THD; Phase Disposition Modulation Technique; Transistor Clamped H-Bridge MLI

I. INTRODUCTION

An inverter is basically a device that converts electrical energy of DC form into that of AC, which are widely used in renewable energy production, motor drive, and uninterruptible power supply applications [1] – [4]. A simplified block diagram of a single-phase, full bridge dc/ac power converter is depicted in Fig.1. The Sinusoidal Pulse Width Modulation (SPWM) technique is widely employed in order to adjust the dc/ac inverter output voltage amplitude and frequency to the desired value. In this case, the power converter switches are set to the ON or OFF state according to the result of the comparison between a high-frequency, constant-amplitude triangular wave (carrier) with two low-frequency reference sine waves of adjustable amplitude and/or frequency [5], [6]. In the unipolar SPWM technique which is illustrated in Fig. 2, the generated pulses are either positive or negative during each half period of the SPWM wave. The high-frequency harmonics of the generated SPWM signal, *V*spwm in Fig. 2, posses are then filtered using a low-pass *LC*-, *LCL*- or *LLCL* type filter [5], [7] thus producing the high-power and low-frequency sinusoidal waveform *Vo* at the output terminals of the dc/ac inverter.

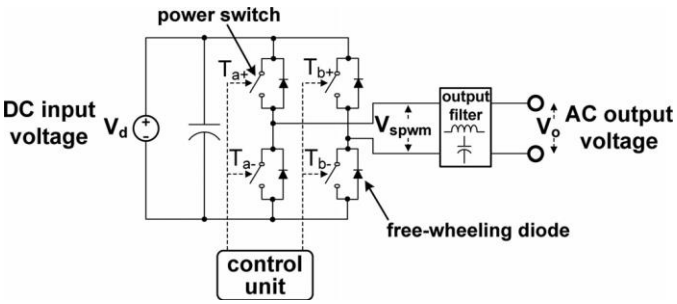

Fig. 1. Block diagram of a single-phase, full-bridge dc/ac power converter.

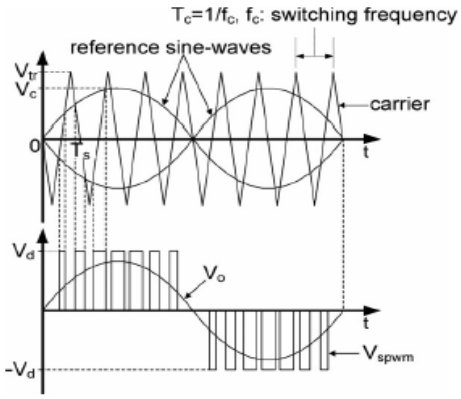

Fig. 2. Unipolar SPWM technique.

The AC output available from an inverter should have less distortion in order to obtain a good power quality [8],[9].To obtain low distortion on the output voltage waveforms, the conventional inverters are switched at very high frequency [8]. However, high switching frequency causes high dv/dt of output voltages, higher switching losses, voltage doubling effects and electro-magnetic interferences [8].One of the alternatives for the above mentioned problem is made by the development of multilevel inverters. Multilevel inverters generate an AC voltage using small voltage steps obtained with the help of DC supplies or capacitor banks [10]. Output voltages obtained from multilevel inverters are superior in quality and need less filter requirements thereby reducing the overall system size [11]. The output voltage of the multilevel inverter can be improved by increasing its number of levels. The total harmonic distortion (THD) also reduces thereby improving the power quality of the overall system.

There are mainly three most common multilevel inverters which include the neutral point clamped inverter, flying capacitor inverter and cascaded H-bridge inverter [8]-

[12], [13]-[14]. The diode clamped multilevel inverter topology requires more number of clamping diodes thereby making the circuit complex, bulky and expensive [15], [16]. In a capacitor clamped topology, floating capacitors are used to hold the voltage levels [17]. Compared to the other two topologies, cascaded H-bridge multilevel inverter is more reliable as it has a modular structure [17]-[18], [13], and [19]. But it require separate DC source for each H-Bridge unit, causing an increase in the cost [20].

For getting a better output voltage with minimum harmonic distortion, multilevel inverters employ different modulation techniques. Some of the commonly used modulation techniques include Sinusoidal Pulse Width Modulation, Selective Harmonic Elimination, Space Vector Modulation etc [21], [9]-[10], [18], [13], [22], and [23]. Various topologies of multilevel inverters have been introduced with several modulation techniques. Nowadays, researchers focus on topologies and modulation techniques that can produce a higher output voltage level with reduced number of switches. A 5-level transistor clamped multilevel inverter with reduced number of switches is introduced in this paper. The output voltage, output current and voltage stress across the switches of the transistor clamped H-bridge multilevel inverter is obtained by employing pulse disposition pulse width carrier modulation technique.

This paper is organized as follows: Section II discusses in brief the existing system. Section III describes the proposed transistor clamped H-bridge multilevel inverter with reduced number of switches. Section IV shows the simulation results and Section V concludes the work.

II. EXISTING SYSTEM

There are different types of methodologies found in existing system to obtain high switching frequency. Here the system is implemented using FPGA. SPWM generator is used to adjust the dc/ac inverter output voltage and frequency. The architecture of existing SPWM generation unit is presented in Fig. 3. The system inputs are the modulation index of the output SPWM wave *M*, as well as the "clock" and "reset" signals. The architecture of the proposed system consists of five subsystems, like Clock Generator Subsystem, Modulation Index Subsystem, Sine-carrier Subsystem, Adjustable Amplitude Sine Subsystem and Comparison Subsystem, which implement the SPWM generation algorithm. The values of a sinusoidal wave, mathematically being in the range [−1, 1], have been adapted in the proposed architecture to the equivalent range of [0, 255] with the zero point corresponding to the discrete value of "128."

A. Clock Generator Subsystem

The FPGA input clock will be the input of the "Clock generator" subsystem and in turn produces a new clock signal used by the digital circuits of the proposed SPWM generator. Thereby the desired SPWM switching frequency fc specified by the designer/user is generated. The input clock frequency f clk is set to f clk/2 using two state finite state machine (FSM).

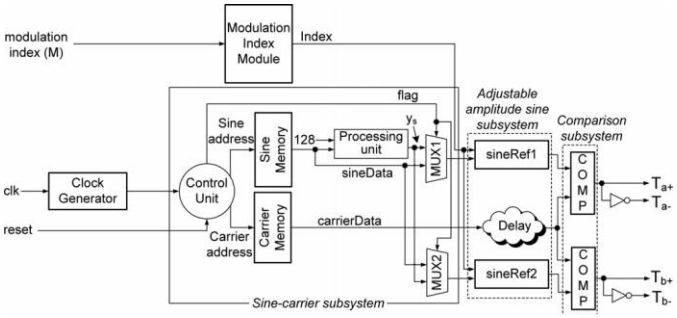

Fig. 3. Architecture of the proposed SPWM generation unit.

A Digital Clock Manager module adapts this frequency to the desired value. DCM module uses the Very high speed integrated circuit Hardware Description Language (VHDL) code. The operational parameters "CLKFX_MULTIPLY" and "CLKFX_DIVIDE" of the DCM module are changed according to the switching frequency requirements of the SPWM output waveform, while the FSM is kept constant. Therefore, the proposed SPWM generator is flexible to be adapted to the generation of any operating switching frequency specified by the system designer.

B. Modulation Index Subsystem

The "Modulation index" subsystem will convert the floating-point modulation index *M*, which is input in the proposed SPWM generation system ($M \in [0, 1]$) to the corresponding value in fixed-point arithmetic.

C. Sine-Carrier Subsystem

The "Sine-Carrier" subsystem consists of the control unit, two BRAMs, which contain samples of the sinusoidal and triangular (i.e., carrier) waves and two multiplexers that produce the two constant-amplitude reference sine waves used for the production of the SPWM output signals. The BRAMs of the sine wave and carrier operate as LUTs. Both the sinusoidal and triangular waves are simulated through MATLAB simulink and through FPGA using VHDL. The value of the sine waves are obtained from the MATLAB and is used in FPGA to produce a sine wave and the produced wave is then inverted to obtain sine wave of opposite phase.

D. Adjustable Amplitude Sine Subsystem

The constant-amplitude reference sinusoidal value produced by the "Sine-Carrier" subsystem is the input of the "Adjustable amplitude sine". It generates a sinusoidal digital signal *ya* with adjustable amplitude according to the value of the modulation index *M* which is an input in the SPWM generation system. The value of *ya* is in the range 0– 255 and it is then calculated. The value of the constant amplitude reference sine wave and *Index* is the output of the "Modulation Index" subsystem.

E. Comparison Subsystem

The comparison between the high-frequency constant amplitude triangular waves (carrier) with the two low frequency reference sine waves, using two comparators ("COMP") is implemented by the "Comparison" subsystem. The control signals *Ta+, Ta−, Tb+*, and *Tb−* are generated from the outputs of the corresponding comparators of this subsystem. They form the SPWM wave (*V*spwm) at the dc/ac inverter output terminals. The outputs of the comparators in

the Comparison" subsystem (i.e., control signals *Ta+* and *Tb+*) are equal to one when the corresponding output of the "Adjustable amplitude sine" subsystem is equal to or greater than the current digital value of the carrier signal. The DC/AC inverter control signals *Ta−* and *Tb−* are produced by inverting *Ta+* and *Tb+*, respectively.

An FPGA-based SPWM generator has been implemented and simulated as depicted in fig. 4, which is capable to operate at high switching frequencies.

III. PROPOSED 5- LEVEL TRANSISTOR CLAMPED H-BRIDGE MULTILEVEL INVERTER

Fig.5. Shows a 5-level transistor clamped Multilevel Inverter. It has a normal H-Bridge inverter and an auxiliary circuit which consisting of a single IGBT switch is combined. The power circuit of TCHB multilevel inverter is such that it can produce more output levels with reduced number of power switches [24], [23] thereby reducing the complexity.

Fig. 6. Shows the multicarrier level shifted sinusoidal pulse width modulation technique. In this method, four triangular carrier waves of equal amplitude arranged one over the other is compared with a sinusoidal wave was introduced to generate

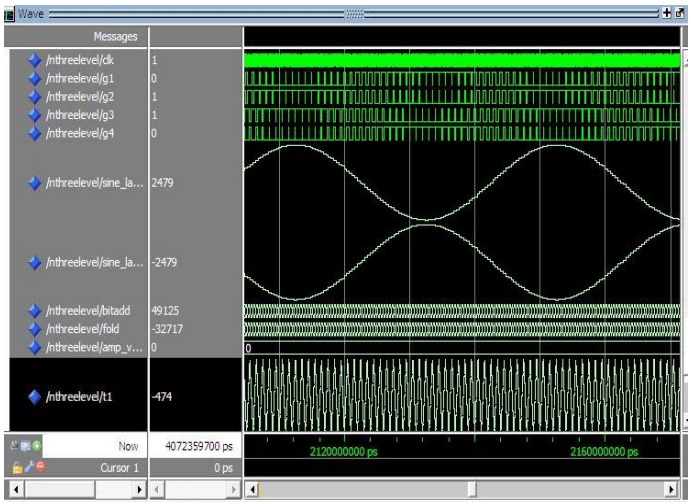

Fig. 4. Output waveform of Comparison of Sine wave with reference carrier waveform.

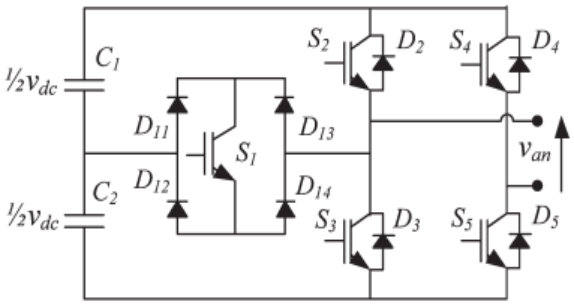

Fig. 5. Transistor clamped CHB multilevel inverter

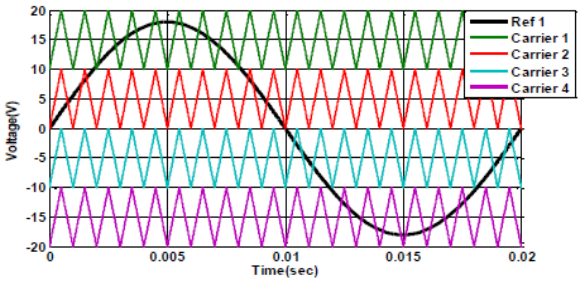

Fig. 6. Multicarrier level shifted modulation techniques

the PWM switching signals in the proposed system. In this method all the carriers above and below zero reference line are in same phase. If all the carriers are selected with the same phase, the method is known as Phase Disposition (PD) method [25]. Carrier and reference wave arrangements are as shown in Fig. 6. The PDPWM is the widely used strategy for Modular Multilevel converters and conventional multilevel inverters because it provides load voltage and current with lower harmonic distortion [26].

The converter is switched to + Vdc / 2 when the sine wave is greater than both carriers, the converter switches to +Vdc / 4 when the sine wave is lower than the uppermost carrier waveform and greater than all other carriers, the converter is switched to zero when sine wave is lower than upper carrier but higher than the lower carrier, the converter switches to - Vdc / 4 when the sine wave is higher than the lowermost carrier waveform and lesser than all other carriers and the converter is switched to - Vdc / 2 when the sine wave is less than both carrier waveforms.

In this topology five level output voltage is obtained by reduced number of switches compared to that of conventional cascaded H-Bridge multilevel inverter. The pulse pattern for a TCHB MLI is shown in Fig 7.

IV. SIMULATION RESULTS

The TCHB multilevel inverter with reduced number of switches is simulated using MATLAB-Simulink. The simulation is carried out for modulation index of 1.25. Fig. 8 and Fig. 9 shows expected waveforms of output current and output voltage. It is seen that the total harmonic distortion is reduced. The simulation of the multilevel inverter is then implemented using FPGA in XILINX ISE Design Suite14.5.

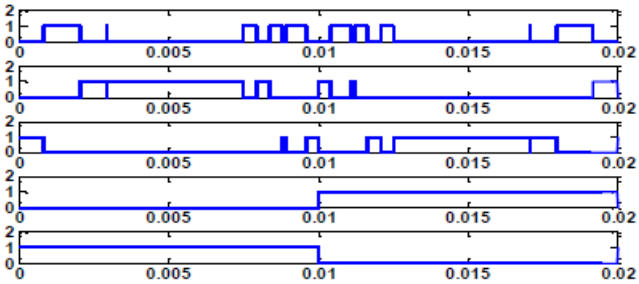

Fig. 7. Gate pulses for the switches from s1-s5

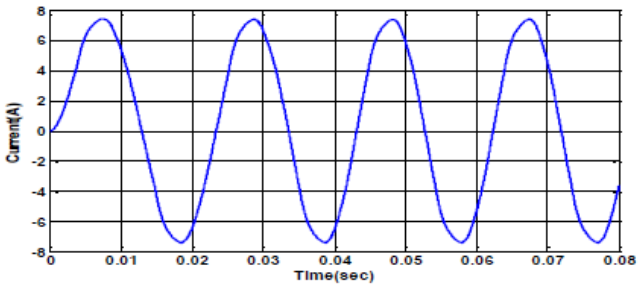

Fig. 8. Output current of TCHB MLI for m=1.25

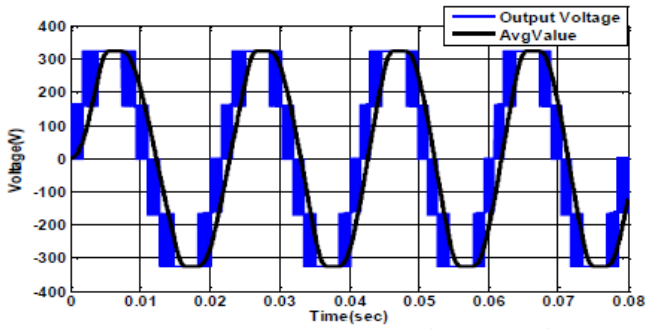

Fig. 9. Output voltage of TCHB MLI for m=1.25

TABLE I. DESIGN PARAMETERS FOR A TRANSISTOR CLAMPED H-BRIDGE MLI

DC Voltage	325 V
Modulation Index	0.85<mi<1.25
Switching Frequency	20 kHz
Rated output voltage	1000 W
Power factor	.89
Capacitance C1-C2	1100µF

Table I shows the various design parameters used for the simulation of a single-phase five level transistor clamped H-Bridge inverter.

V. CONCLUSION

For controlling multilevel inverter different modulation scheme are used. Of these different modulation schemes SPWM method has gained more interest in industrial application. The same can be implemented using hardware. Mainly DSP or microcontroller based controller are preferred over analog controller for implementing SPWM scheme for multilevel inverter. But DSP based scheme such as symmetrical sampling, asymmetrical sampling or regular sampling method either produce phase delay in generated output waveform or required dedicated processor for continuous sampling. In this paper, phase disposition pulse width modulation technique is employed for a transistor clamped H-bridge multilevel inverter. The simulation is done through MATLAB simulink and implemented using FPGA. It is found that the transistor clamped H-Bridge multilevel inverter requires only reduced number of switches and exhibits a better performance with reduced Total Harmonic Distortion.

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