International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 2 Issue 5, May - 2013

VLSI Architecture For DCT Based On Distributed Arithmetic

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Abstract

Discrete cosine transform (DCT) is widely used in multimedia communications such as image and video which require high volume of data transmission. An 8x8 2-D discrete cosine transform is used in image and video compression standards. DCT is a computation intensive operation. It requires a large number of adders and multipliers for direct implementation. Multipliers consume more power and hence distributed arithmetic (DA) is used to implement multiplication without multiplier so, DA acts as an multiplier . In the proposed method, VLSI architecture of 1-D DCT based distributed arithmetic (DA) is for low hardware circuit cost as well as low power consumption. The proposed 1-D DCT architecture is implemented in Xilinx ISE Simulator.

With proposed 1-D DCT architecture, 2-D DCT will implement using row column decomposition technique. Results of proposed architecture with existed architecture are compared and delay and power is reduced to 50% . Further, this project can be extendable by using any other type of faster adder/multiplier in terms of area, speed and power.

Keywords: Discrete cosine transform (DCT), Distributed arithmetic (DA).

1. Introduction

A discrete cosine transform (DCT) expresses a sequence of finitely many data points in terms of a sum of cosine functions oscillating at different frequencies. DCTs are important to numerous applications in science and engineering, from lossy compression of audio and images (where small high-frequency components can be discarded), to spectral methods for the numerical solution of partial differential equations. The use of cosine rather than sine functions is critical in applications such as compression. The cosine functions are much more efficient where as for differential equations the cosines express a particular choice of boundary conditions.

As like Fourier-related transform, DFT, discrete cosine transforms (DCTs) express a function or a signal in terms of a sum of sinusoids with different frequencies and amplitudes. And which operates on a function at a finite number of discrete data points. However, this visible difference is merely a consequence of a deeper distinction. A DCT implies different boundary conditions than the DFT or other related transforms.

Frequency analysis of discrete time signals is most convenient in DCT. Discrete cosine transform is the most popular transform technique for image compression and is adopted on various standardized coding schemes. Some applications require real-time manipulation of digital images. Because this, fast algorithms and specific circuits for DCT have been developed. Among the methods for two-dimensional DCT, the indirect method based on row-column decomposition is the best method for hardware implementation.

The energy compaction property of the DCT is well suited for image compression since, as in most images, the energy is concentrated in the low to middle frequencies, and the human eye is more sensitive to the middle frequencies.

A large majority of useful image contents change relatively slowly across images, i.e., it is unusual for intensity values to alter up and down several times in a small area, for example, within an 8 x 8 image block. Translate this into the spatial frequency domain, it says that, generally, lower spatial frequency components contain more information than

the high frequency components which often correspond to less useful details and noises.

The Discrete Cosine Transform, transforms data into a format that can be easily compressed. The characteristics of the DCT make it ideally suited for image compression algorithms. These algorithms let you minimize the amount of data needed to recreate a digitized image. Reducing digitized images into the least amount of data possible has some advantages such as Less memory required to store images, Less time may be needed to analyze images, Channel bandwidth efficiency increased when transmiting images.

Performing the DCT on a digitized image creates a data array that can be compressed by data compaction algorithms. Then, data can be stored or transmitted in its compacted form. The image quality depends on the amount of quantization used in the compaction algorithm. To reproduce the original image, the data is retrieved from memory, uncompacted, and an inverse DCT is performed.

Some of today's most popular image data compression applications include, Teleconferencing using motion-compensated video codecs, ISDN multimedia communications including voice, video, text, and images, Video channel transmission using commercial geosynchronous tele communications satellites, Digital facsimile transmission using dedicated equipment and personal computers.

Several image data compression algorithms use the DCT to remove spatial data redundancies in two-dimensional (2D) data. Images are subdivided into smaller, two-dimensional blocks. These blocks are then processed independently of the neighboring blocks. In general, the two dimensional, discrete cosine transform (2D DCT) transforms an (n x n) data array into an (n x n) result array. First the DCT transforms the columns, then it transforms the rows.

2. Existing Method (DCT in pipelined fashion)

For a 2-D data X(i, j), $0 \le i \le 7$ and $0 \le j \le 7$, 8x8 2-D DCT is given by

$$F(u,v)=\frac{2}{8}C(u)C(v)\sum_{i=0}^{7}\sum_{j=0}^{7}X(i,j) \times\cos\left(\frac{(2i+1)u\pi}{16}\right)\cos\left(\frac{(2j+1)v\pi}{16}\right) \quad (1)$$

Where $0<u<7$ and $0<v<7$ and C(u),C(v)=1/2 for u,v=0,C(u),C(v)=1

Implementation computation is reduced by decomposing 2-D DCT in two 8x1 !-D DCT & it is given by

$$F(u)=\frac{1}{2}C(u)\sum_{i=0}^{7}X(i)\cos\left(\frac{(2i+1)u\pi}{16}\right) \quad (2)$$

Considering the periodicity and the symmetry of trigonometry function, the following 8 equations can be inferred from equation (2). Then the 1-D DCT is simplied as by applying i=0 to 7 from eqn (2)

F(0) =[X(0) + X(1) + X(2) + X(3) + X(4) + X(5) + X(6) + X(7)]P
F(1)=[X(0)-X(7)]A+[X(1)-X(6)]B+[X(2)-X(5)]C + [X(3)-X(4)]D
F(2) =[X(0)- X(3)- X(4)+ X(7)]M+[X(1)-X(2)-X(5)+ X(6)]N
F(3)=[X(0)-X(7)]B+[X(1)-X(6)](-D)+[X(2)-X(5)](-A)+[X(3) -X(4)](-C)
F(4) =[X(0) - X(1) -X(2) + X(3) + X(4) - X(5) - X(6) + X(7)]P
F(5) =[X(0)- X(7)]C+[X(1)- X(6)](-A)+[X(2)-X(5)] D +[X(3)- X(4)]B
F(6) =[X(0)- X(3)- X(4)+ X(7)]N+[X(1)- X(2)- X(5) + X(6)](-M)
F(7) =[X(0) -X(7)]D+[X(1)-X(6)](-C)+[X(2)-X(5)] B +[X(3)-X(4)](-A)

Where,
M=1/2 cos(π/8), N=1/2cos(3π/8), P=1/2cos(π/4),
A=1/2cos(π/16), B=1/2cos(3π/16), C=1/2cos(5π/16),
C=1/2cos(7π/16);

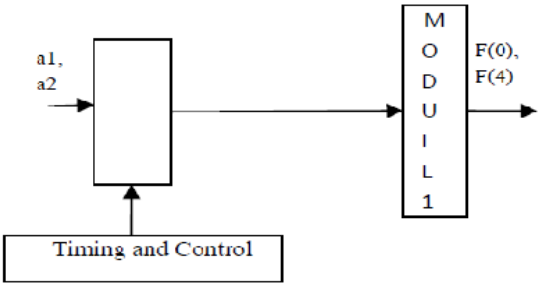
Let us assume the equations as

a1=X(0)+X(1)+X(2)+X(3)+X(4)+X(5)+X(6)+X(7),
a2=X(0)-X(1)-X(2)+X(3)+X(4)-X(5)-X(6)+X(7),
b1=X(0)-X(7),
b2=X(1)-X(6),
b3=X(2)-X(5),
b4=X(3)-X(4),
c1=X(0)-X(3)-X(4)+X(7) and
c2-X(1)-X(2)-X(5)+X(6).

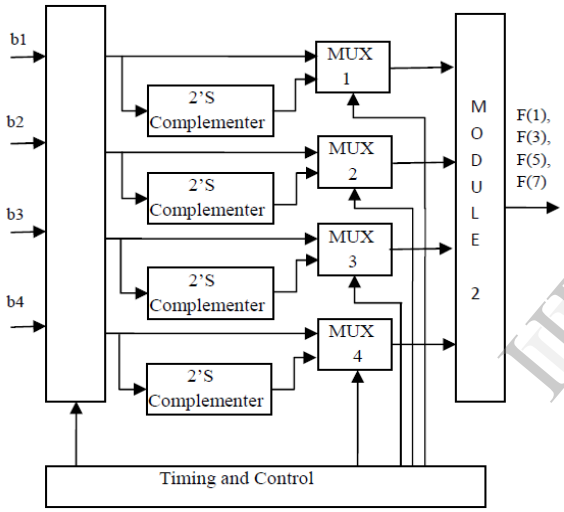
By implementing above equqtions in 1-D DCT equations, it becomes

F(0)=a1xP, F(4)=a2xP.
F(1)=b1xA+b2xB+b3xC+b4xD.
F(3)=b1xB-b2xD-b3xA-b4xB.
F(5)=b1xC-b2xA+b3xd+b4xB.

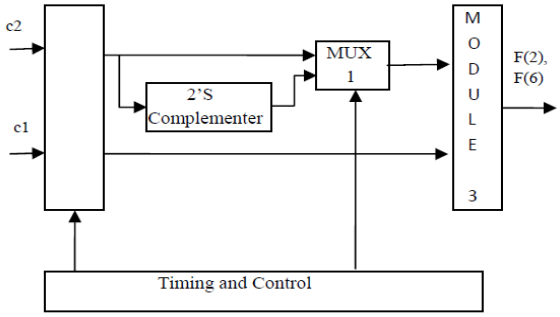
F(7)=b1xD-b2xC+b3xB-b4xA.
F(2)=c1xM+c2xN, and F(6)=c1xN-c2xM.



"Figure 1. VLSI architecture for computing of 8 point DCT in pipeline manner for computation of F(0) and F(4)"



"Figure 2. VLSI architecture for computing of 8 point DCT in pipeline manner for computation of F(1), F (3), F(5)"



"Figure.3. VLSI architecture for computing of 8 point DCT in pipeline manner for computation of F(2) and F(6)"

In the fig 2,3,4 the 1D-DCT architecture is implemented in pipeline fashion ,it requires more no.of multipliers and adders so it consumes more power,area and delay wiil be more.

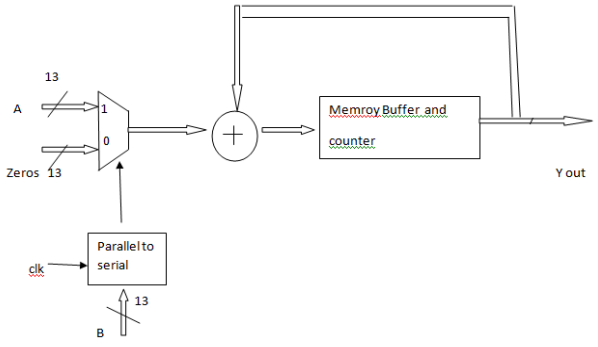
3. Proposed Method

(DCT using Distributed Arithmetic)

Distributed arithmetic is a bit level rearrangement of a multiply accumulate to hide the multiplications. It is a powerful technique for reducing the size of a parallel hardware multiply-accumulate that is well suited to FPGA designs. It can also be extended to other sum functions such as complex multiplies, fourier transforms. Distributed arithmetic(DA) is an effective method for computing inner products. It uses Look Up Tables(LUT) and accumulators instead of a multipliers.

Distributed arithmetic (DA) provides application in Very Large Scale Integration(VLSI) implementations of Digital Signal Processing(DSP) algorithms. Most of these applications, for example Discrete Cosine Transform(DCT) calculation, are arithmetic intensive with multiply/accumulate (MAC) being the predominant operation.

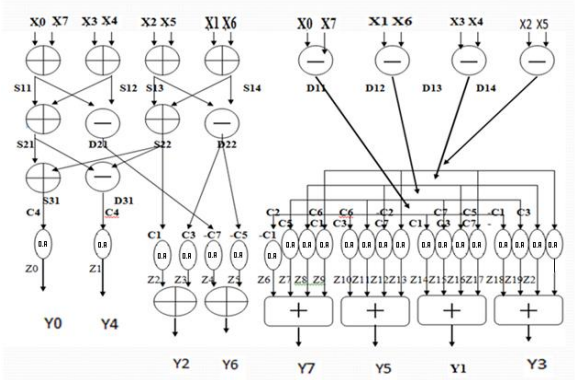
The advantage of DA approach is that it alerts the basic assumption of using multipliers and adders for computing the DCT.



"Figure 4. Distributed Arithmetic"

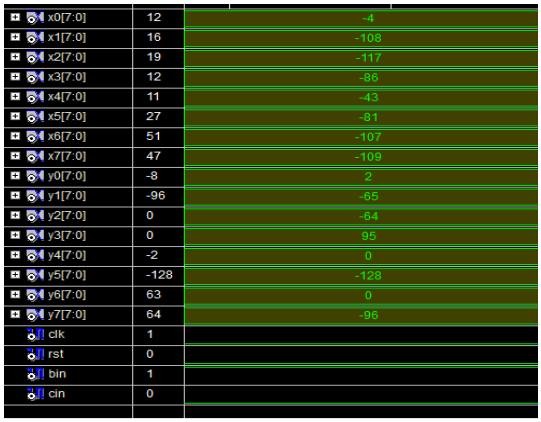
DCT is a computational intensive operation.It requires large number of adders and multipliers for direct implementation .Multipliers consume more power and hence distributed arithmetic (DA) is used to implement multiplication without multiplier.

The above 8 equations F(0) to F(7) are analysed and instead of multiplier Distributed Arithemetic (DA) is used for the arhitecture of 1D-DCT

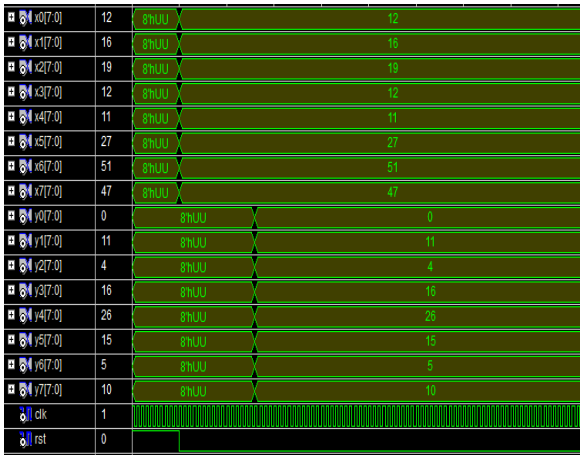


"Figure 5. Overall architecture for DA base DCT"

4. Simulation Results



"Figure.6. Simulation of 1-D DCT Architecture"



"Figure 7. Simulation of 1-D DCT using DA architecture"

In this work VHDL code is written for the1D-DCT architecture using Distributed Arithmetic and implemented in Xilinx ISE simulator.

"Table 1. Device Utilization"

Device	Existing method	Proposed method
No.of 4 i/p LUT's	692	372
No.of slices	370	303
No.of slice flip flops	97	97
No.of IOB flip flops	0	18
Min period(ns)	16.29(Freq:61.38 MHz)	9.156(Freq:109.213 MHz)

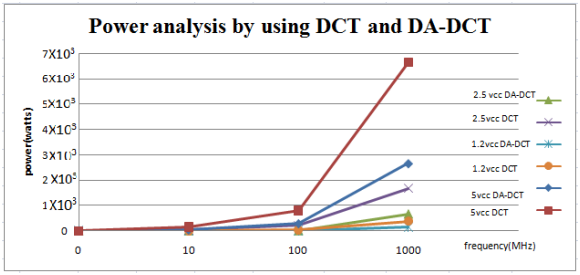
Table1 shows the device utilization for both existed method and proposed method . It is observed that the delay is reduced and frequency is increased in the proposed method

"Table 2. Power Calculation"

Vcc/Frequency	DCT			DA-DCT		
	10MHz	100MHz	1000MHz	10MHz	100MHz	1000MHz
1.2	8.95	46.35	383.05	2.34	16.00	152.94
2.5	38.87	201.7	1662.53	10.16	16.39	663.82
5.0	155.47	804.66	6650.11	40.43	284.46	2655.27

Table 2 shows the power calculation for normal DCT and DA-DCT

5. Graphical Analysis for Power



"Figure 8. Graphical representation for power"

In fig.7 x-axis represents frequency, y-axis represents power. Power is analysed for both the methods at 10,100,1000MHz and it is reduced up to 50% for DA-DCT when compared to normal DCT.

6. Conclusion

The proposed 1-D DCT Architecture using distributed arithmetic is designed and simulated using Xilinx ISE simulator. Power is calculated and it is reduced to 50% when compared to normal DCT. Here the device utilization is compared and delay has been reduced to large extent.

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