

VHDL Implementation of Reversible Full Adder using PERES Gate

Md. Riyaj¹, Anshul Gangwar², Gagan Goyal³
 M-tech Scholar Suresh Gyan Vihar University, Jaipur, India¹,
 M-tech Scholar Suresh Gyan Vihar University, Jaipur, India²,
 M-tech Scholar Jaipur National University, Jaipur, India³

Abstract— In low power vlsi design and power optimization reversible logic method is being used more frequently. It is also the fundamental need for the emerging field of the quantum computing ,Digital signal processing and communications. The use of reversible logic in vlsi design has many advantages because it reduces number of gates and garbage outputs. When we use a logically irreversible gate we dissipate energy into the environment. The loss of energy equals to the information loss. One bit information lost dissipates $KT \ln 2$ of energy. By reversible logic we can reduce power dissipation. In reversible logic number of input equals to the number of outputs. i.e $k*k$. All the outputs are not used as input to other gate is called garbage output. This paper presents quantum implementation and combinational circuit of all basic reversible gates and its VHDL code. All reversible logic gates are verified and simulated by Xilinx8.2i.

Keywords— Reversible logic, NOT gate, FEYNMAN gate, PERES gate, VHDL CODE, TR gate

I. INTRODUCTION

To increase the speed the clock frequency must be increased. In VLSI systems increase in number of transistors makes the system complex which[1] further increase the power consumed by the system. Moreover any Boolean function can be implemented by using logic of reversible logic gates as it has already been proved.

When an input is applied to the reversible gate, a logical operation is performed and also there is loss of some information which is dissipated as heat. So we can conclude that power dissipation is the main concern for both producers and consumers. A reversible logic gate gives a unique output pattern for each input pattern. It has k -inputs and k -outputs, hence denoted by $k*k$. In reversible logic gates we have one more aspect to focus on than that of number of gates ,is the number of garbage outputs. Garbage

outputs are those outputs from a reversible circuit that are not used as an output.

In low power VLSI design another problem is the solution of Landauer's principle. It states that logical [2] computation of

irreversible gates generate $KT*\log 2$ Joules of heat energy on loss of every bit of information. K is the Boltzmann constant

and T is the absolute temperature at which the operation is performed.

To reduce the power dissipation and to prevent the loss of information reversible logic is used it has application[3] in different field like as in field of low power computing quantum computing optical computing and other encoding computing technologies.

In a reversible circuit the input vector can be reconstructed from the output vector. Not only outputs can be calculated from the input but also the inputs can be reconstructed the number of input and output are equal. It finds application in low power CMOS design, optical computing , DNA computing quantum computing, nano technology, bioinformatics and thermodynamic technology . in quantum circuits reversible logic gates are used. Fanout and feedback is not permitted in reversible logic gates.

NOT gate is the simplest $1*1$ reversible gate . An example of a $2*2$ reversible gate is controlled gate(CNOT). Examples for $3*3$ reversible gates are F,TG,PG and TR gate.

The performance of the reversible gate is calculated by calculating the quantum cost by counting the number of V , V^+ and CNOT gates. Some properties of V and V^+ quantum gates are given below:

$$V*V=NOT$$

$$V*V^+=V^+*V=-1$$

$$V^+*V=NOT$$

II. BASIC REVERSIBLE GATE

A. NOT Gate

The reversible $1*1$ gate[4] is NOT gate with zero quantum cost is as shown below.

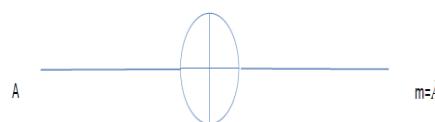


Fig 1 Quantum implementation of NOT gate

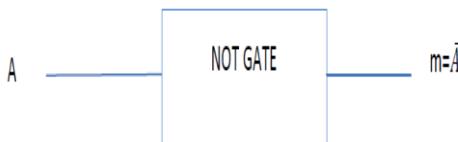


Fig 2 1*1 NOT GATE

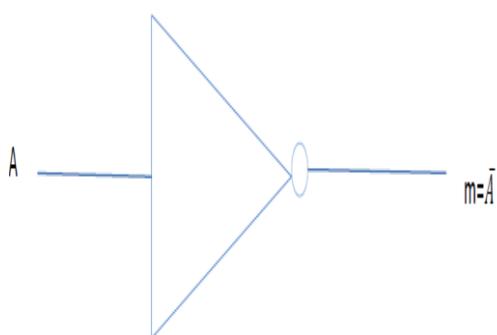


Fig 3 Combinational circuit of NOT gate

VHDL CODE

```
library ieee;
use ieee std_logic_1164.all;
entity not is
port(A : in std_logic;
      m : out std_logic);
end not;
```

B. FEYNMAN/CNOT GATE

The reversible 2×2 gate with quantum cost of one having mapping [5]input (P,Q) to output(X,Y) is as shown in figure.

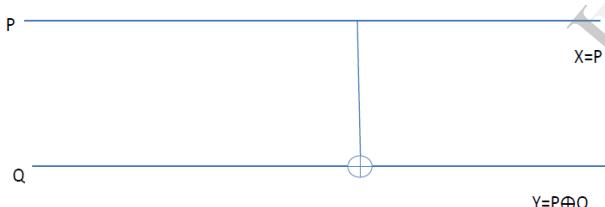


Fig 4 Quantum implementation of FEYNMAN gate

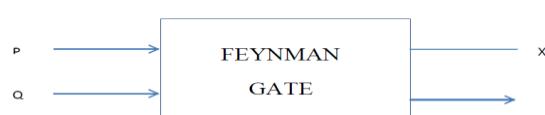


Fig 5 2*2 FEYNMAN gate

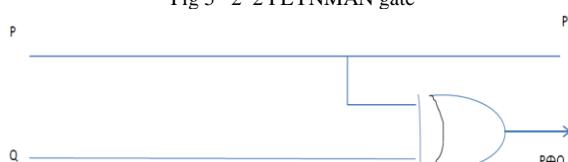


Fig 6 Combinational circuit of FEYNMAN gate

VHDL CODE

```
library ieee;
use ieee std_logic_1164.all;
entity feynman is
port(P,Q : in std_logic;
      X,Y : out std_logic);
end feynman;
```

architecture ckt of feynman is
begin
X <= P;
Y <= P xor Q;
end ckt;

C. PERES GATE

The reversible 3×3 gate with quantum cost of four having mapping input (P,Q,R) to output(X,Y,Z) is as shown in figure.

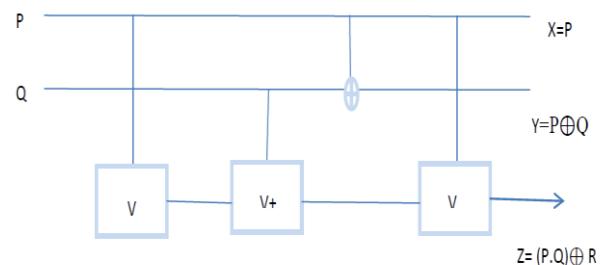


Fig 7 Quantum implementation of PERES gate

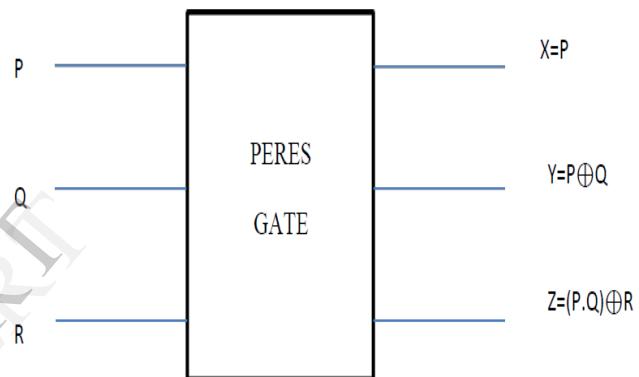


Fig 8 3*3 PERES gate

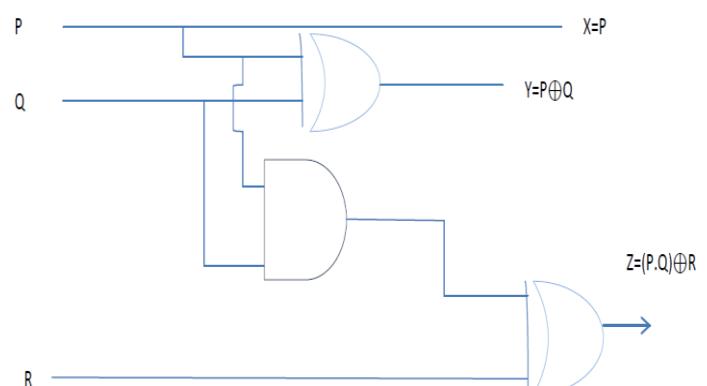


Fig 9 Combinational circuit of PERES GATE

VHDL CODE

```
library ieee;
use ieee std_logic_1164.all;
entity peres is
port(P,Q,R : in std_logic;
      X,Y,Z : out std_logic);
end peres;
architecture prs of peres is
signal S1: std_logic
```

```

begin
X <= P;
S1 <= P and Q;
Y <= P xor Q;
Z <= S1 xor R;
end prs;

```

2.4 TR GATE

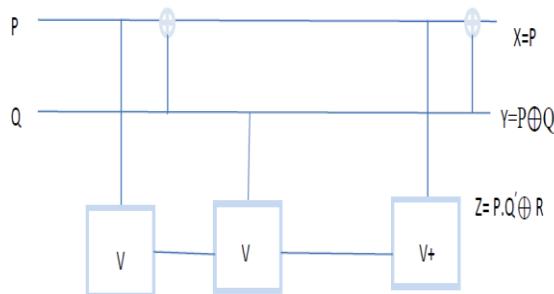


Fig 10 Quantum implementation of TR gate

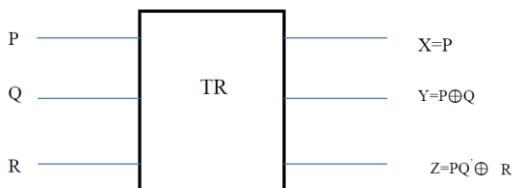


Fig 11 3*3 TR gate

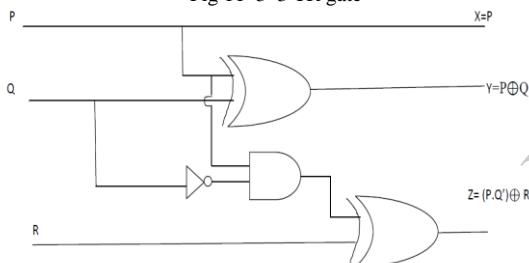


Fig 12 Combinational circuit of TR gate

VHDL CODE

```

library ieee;
use ieee std_logic_1164.all;
entity trgate is
aport(P,Q,R : in std_logic;
      X,Y,Z :out std_logic);
end trgate;
architecture tr of trgate is
signal Bbar,S1: std_logic;
begin
X <= P;
S1 <= P and Qbar;
Y <= P xor Q;
Z <= S1 xor R;
end tr;

```

III. PURPOSED PERES FULL ADDER

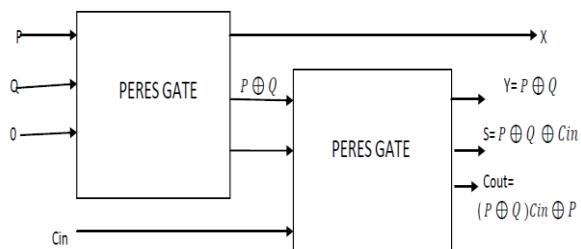


Fig 13 PERES full adder

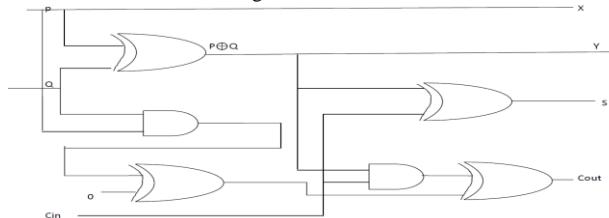


Fig 14 Combinational circuit of PERES full adder .

VHDL CODE

```

Library ieee;
USE ieee std_logic_1164.all;
USE ieee numeric_std.all;
Entity FA is
Port (P: in std_logic;
      Q: in std_logic;
      Cin: in std_logic;
      Zero: in std_logic;
      X: out std_logic;
      Y: out std_logic;
      S: out std_logic;
      Cout: out std_logic);
End FA ;
Architecture behavioral of FA is
Signal T1 :std_logic;
Signal T2 :std_logic;
Begin
T1 <= P xor Q
T2 <= (P xor Q) xor zero;
X <= P;
Y <= T1;
S <= T1 xor Cin;
Cout <= (T1 and Cin) xor T2;
End FA

```

IV. RESULT

The purposed PERES full adder as shown in figure 13&14 are implemented and resulted by using VHDL and simulated in Xilinx 8.2 i. The RTL schematic diagram and simulated results shown in figure 15 and figure 16 respectively.

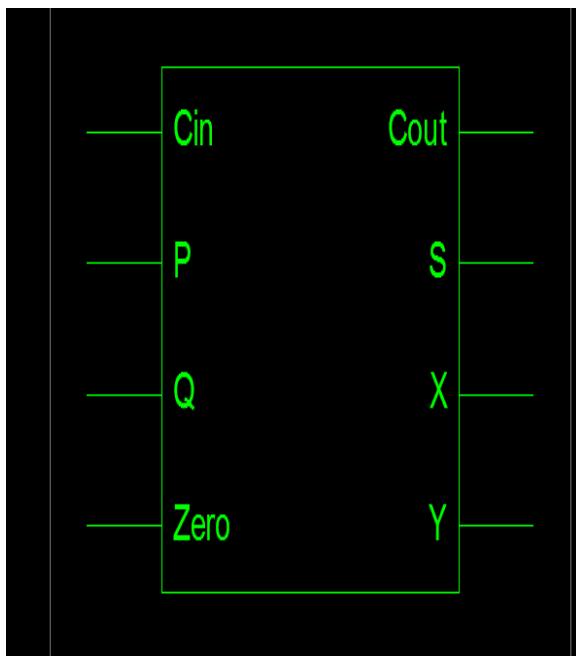


Fig 15(A) RTL schematic diagram for PERES full adder

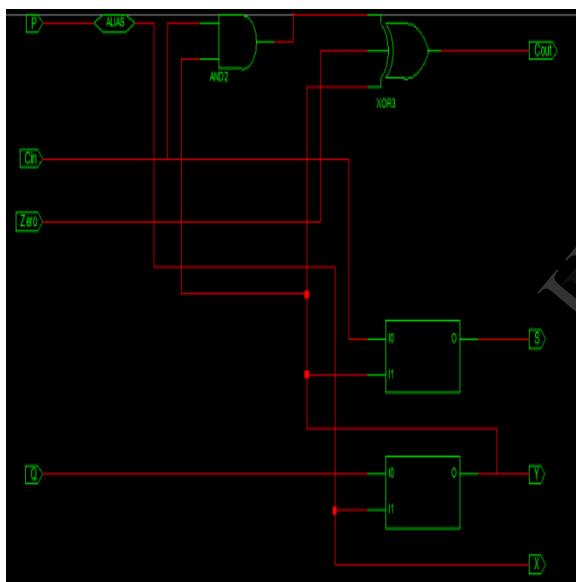


Fig 15(B) RTL schematic diagram for PERES full adder

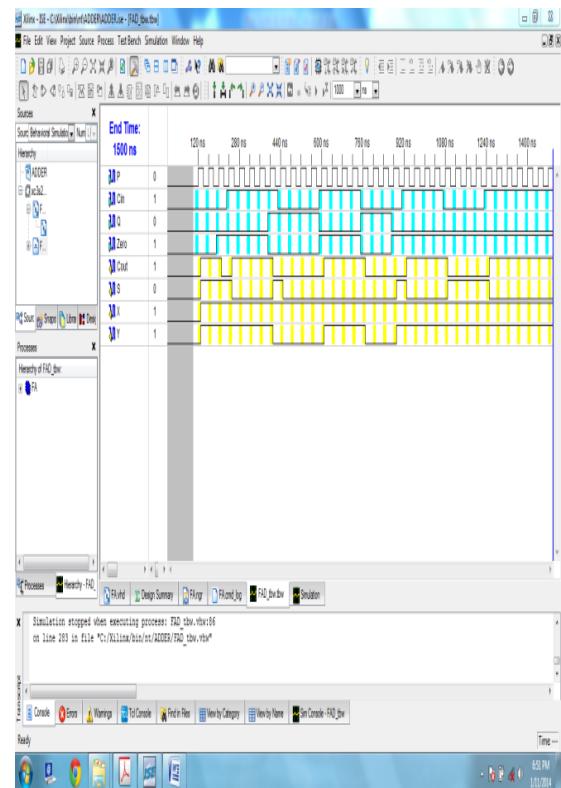


Fig 16(A) Test Bench Waveform & simulation with results

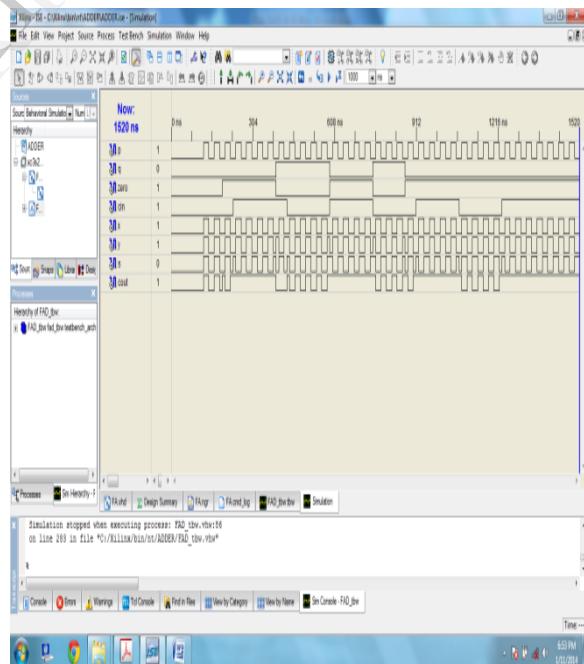


Fig 16(B) Test Bench Waveform & simulation with results

V. CONCLUSION

Reversible gate are used to implement arithmetic circuit using full adder. The main focus of this paper is the proposal of new reversible 4*4 PERES gate. The purposed PERES gate is used to design full adder. It is proved that the purposed PERES full adder is better than the existing counterparts in literature in terms of garbage outputs. By using purposed PERES full adder we can design large reversible systems. Here we can

calculate the power consumption and compare it with the irreversible full adder.

ACKNOWLEDGEMENT

I wish to express my thanks to Mr. Rashid Hussain H.O.D electronics and communication Suresh Gyan Vihar university jaipur and my colleague.

REFERENCES

1. T. Nagababu "A low power adder using reversible logic gates" IJERT Volume 1 issue 3 Nov 2012
2. Homework report "reversible adder implementation in VHDL"
3. Mr Devendra goyal "VHDL implementation of reversible logic gates."
4. Rangaraju H.G. "LOW POWER REVERSIBLE PARALLEL BINARY ADDER"
5. V. Kanalakannan "Design of adder /subtractor circuits based on based on reversible logic gate IJAREEIE vol 2 issue8 august 2013
6. Prashanth N.G. "design and synthesis of fault tolerant full adder/subtractor using reversible logic gates" IJERA vol 3 issue 4 july – aug 2013.
7. A. Kamraj "design of 8-bit arithmetic processor unit based on reversible logic" Global journals volume 13 issue 10 2013
8. Lakshmi viswanath "Design and analysis of 16 bit reversible ALU" IOSRJCE volume 1 Issue 1 june 2012
9. Md. Sajjad hussain "design of control unit for low power ALU with a barrel shifter using reversible logic" IJEBEA @2013
10. Ravish Aradhya "design of control unit for low power ALU with a barrel shifter using reversible logic" IJSER volume 2 issue 9 september 2011.

IJERT