VHDL Implementation of Multiplier using Reversible Logic

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***Abstract*-Conventional Multiplier used in digital circuits dissipates significant amount of energy as bits are erased during logic operations. Multiplier using reversible gates can significantly reduce the power consumed. In this paper, a reversible multiplier (4bit, 8bit and 16bit) is implemented using reversible gates such as MHNG gate and Peres gate. The results shows that proposed reversible multiplier is optimized in terms of number of garbage outputs, number of constant inputs and also has lesser power and delay as compared to conventional multipliers. This paper provides the initial step in building of more complex systems which can execute more complex operations using reversible logic.**

Keywords — Constant inputs ,Garbage outputs, Peres gate, Power delay, Multiplier, Reversible Logic, MHNG gate.

I. INTRODUCTION

Multiplier is basic arithmetic cell in computer arithmetic units. It also plays a vital role in many DSP (Digital Signal Processing) and multimedia applications. However, power dissipation is one of the important parameters in the design of multiplier. Design of multiplier using reversible logic gates is one of the promising solutions to reduce power dissipation to a greater extent and to improve system performance.

According to R.Landauer in the early 1960,any computing system which is not reversible, always dissipate some amout of power because of information loss. [1].It is proved that the loss of one bit of information dissipates at least KTln2 joules of energy (heat), where K=Boltzmann's constant and T=absolute temperature at which operation is performed [1]. If we assume that every transistor out of the 60 million transistors in processor (e.g. Pentium) dissipates energy at a rate equal to its processor frequency (e.g. 2GHz). Then its power consumption will be approximately 2x1016xKT ln2=0.06watts.(Assuming that the processor operates at 300K). This rate at which heat is generated is still small. However, according to Moore's law, the speed, the complexity and hence, the heat dissipation due to the information loss will increase exponentially. If this current trend continues, there will be an intolerable amount of heat generated by computer systems. In 1973, Bennet proved that to avoid KTln2 joules of heat dissipation in a irreversible circuit, such circuit must be built using reversible logic gates [2].

Multiplication is extensively used algorithm in many computational units. It is necessary for any system to have low power multiplier units. This work illustrates the multiplier using reversible gates such as MHNG gate and Peres gate.

II. CONCEPT OF REVERSIBLE LOGIC

Theoretically, internal power dissipation of any reversible logic circuit is zero because information loss is zero. A circuit is called as reversible if it is possible to uniquely determine the input vectors from its output vectors and there is one to one relation between input and output vectors. i.e. not only the output vectors can be uniquely derived from its inputs but also the inputs can be uniquely obtained from the outputs [4-6].Thus, the number of inputs vectors and number of output vectors in reversible logic gates are equal[3-5]. Reversible circuits are also called loss less circuits, as there is neither energy loss nor information loss. These circuits are very attractive for applications where extremely low power consumption. or heat dissipation is desirable in areas ranging from communications , low power VLSI(Very Large Scale Integration) technology, optical computing to nano-technology.

Any reversible logic circuit should have the following features [5]:

- Minimum number of reversible gates
- Minimum number of garbage outputs.
- Minimum constant inputs.

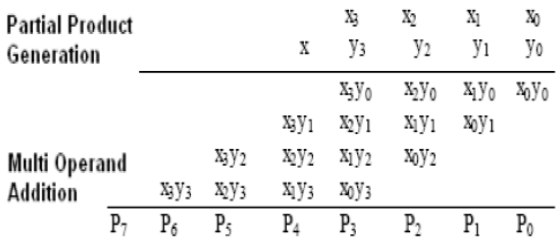
Garbage Output: The output that is not used for further calculation is called as garbage output [6].

Constant Input: The input that is added to an n x k irreversible function to make it reversible (n x n function) is called as constant input [7].

III. PROPOSED REVERSIBLE MULTIPLIER

General multiplier is basically based on two steps:

a) Generation of partial products
b) Addition of partial products.



Peres gate is a 3 inputs 3 outputs (3*3) reversible gate.
It can be represented as:
Iv = (A, B, C)
Ov = (P = A, Q = A XOR B, R = AB XOR C)
Where Iv and Ov are input and output vectors respectively. The peres gate is shown in Fig1.Peres gate can be used as a conventional AND gate and reversible half adder (taking input C as '0') as shown in Fig1.

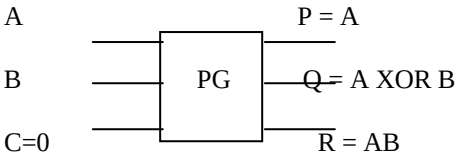


Fig. 1 Peres Gate as a AND gate and reversible half adder.

MHNG gate is 4*4 reversible logic gate.
It can be represented as:
Iv = (A, B, C, D)
Ov = (P = A, Q = D, R = A XOR B XOR C,
S = (A XOR B).C XOR AB XOR D)
Where Iv and Ov are input and output vectors respectively.
One of the prominent functionalities of MHNG gate is that it can singly work as a full adder unit. Implementation of MHNG gate as a full adder is shown in Fig.2.It requires only one constant input and produces only two garbage outputs.

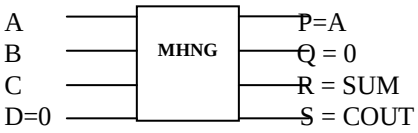


Fig. 2 MHNG Gate as a reversible full adder.

The operation of partial product generation can be achieved using 16 Peres gate in parallel as shown in Fig 3.

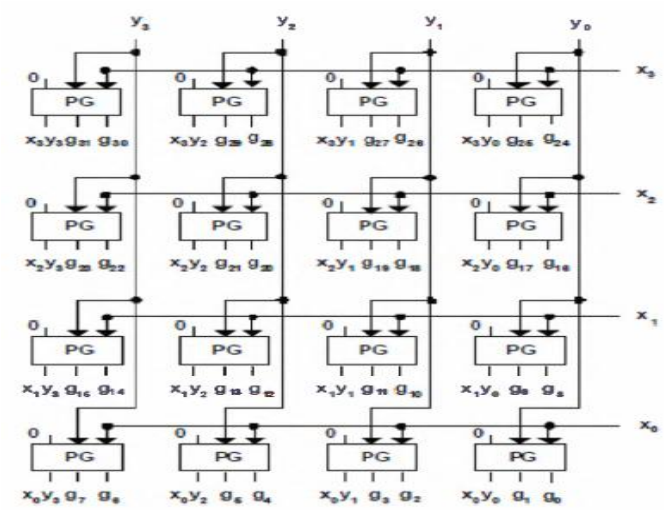


Fig.3 Partial Products Generation (PPG) using Peres gate [9]

Addition of partial products requires 8 full adders and 4 half adders. Reversible MHNG gate and Peres gate can be used as a full adder and half adder respectively. As shown in Fig 4.

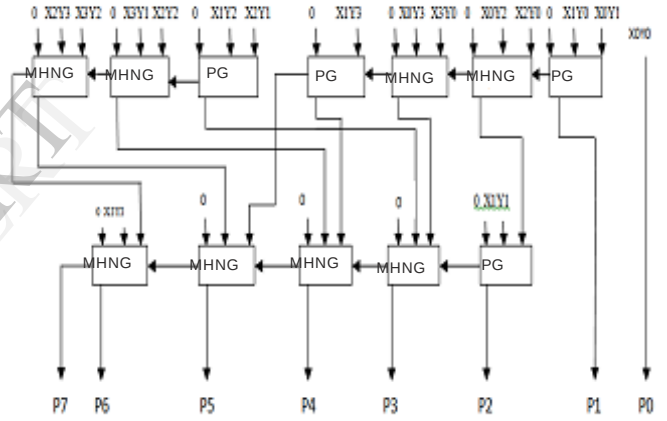


Fig.4 Reversible multiplier architecture (4bit) where outputs of PPG are input of MHNG (full adder) and Peres gate (half adder)

Proposed 4 bit reversible multiplier can be generalized for 8 bit and higher order multiplication using following algorithm.

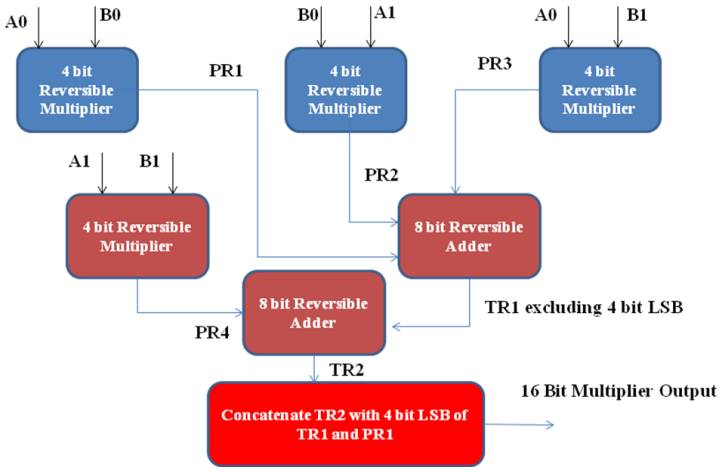


Fig.5 8 bit multiplier using 4 bit multiplier

IV. RESULTS.

Complete code of reversible multiplier (4bit, 8bit and 16bit) is written using VHDL, simulated using Xilinx ISE 13.1 simulator and synthesized using Xilinx synthesis tool (XST) 13.1.Power analysis performed using Xilinx X Power analyzer. Target FPGA used belongs to SPARTAN 3 families, XC3S50 device, VQ100 package, speed grade -5.
Fig. A, B, C shows the simulation results, device utilization summary and power analysis respectively.

Fig A) Simulation waveform.

rev_16bit_mult_using_4bit Project Status			
Project File:	rev_8bit_mult_using_4bit.xise	Parser Errors:	No Errors
Module Name:	rev_16bit_mult_using_4bit	Implementation State:	Programming File Generated
Target Device:	xc3s50-5vq100	• Errors:	No Errors
Product Version:	ISE 13.1	• Warnings:	13 Warnings (13 new)
Design Goal:	Balanced	• Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	0 (Timing Report)

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of 4 input LUTs	165	1,536	10%	
Number of occupied Slices	92	768	11%	
Number of Slices containing only related logic	92	92	100%	
Number of Slices containing unrelated logic	0	92	0%	
Total Number of 4 input LUTs	165	1,536	10%	
Number of bonded IOBs	32	63	50%	
Average Fanout of Non-Clock Nets	3.02			

Fig. B) Device Utilization Summary:

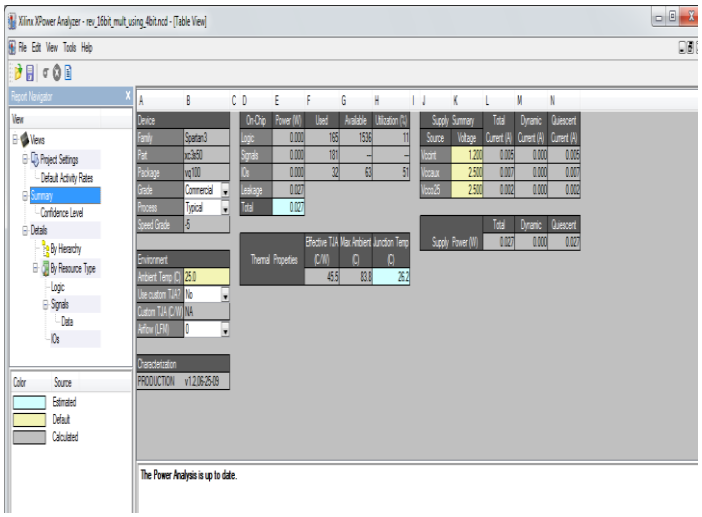


Fig C) Power Analysis:

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Table 1: Results of 4bit, 8bit and 16bit reversible multipliers.

Parameter	Delay	Power	Slices Used	4 Input LUT	Bonded IOBs
4 Bit	15.95ns	18mw	18	29	16
8 Bit	34.53ns	27mw	95	165	32
16 Bit	47.25ns	35.20mw	127	254	46.25

Table 2: Comparison of Reversible and Conventional Multipliers.

Parameter	Delay	Power	Slices Used	4 Input LUT	Bonded IOBs
4 Bit Rev. Multiplier	15.95ns	18mw	18	29	16
4 Bit Conv. Multiplier	16.32ns	27mw	18	32	16

Table 3: Comparison of different 4bit reversible multipliers

Paper No.	No. of Gates	Garbage Outputs	Constant Inputs	No. of Logical Calculations
Proposed Work	28	22	28	80a +36b
[15]	28	32	28	71a + 35b
[14]	28	28	28	71a + 36b
[13]	28	52	28	80a + 36b
[12]	28	56	32	92a + 52b + 36c
[11]	29	58	34	110a + 103b + 71c
[10]	40	56	31	80a + 100b + 68c

We define:
a=A two input XOR calculation.
b=A two input AND gate calculation.
c=A NOT gate calculation.
As shown in table3, our proposed design requires only 28 reversible gates and is also optimized in terms of number of garbage outputs, number of constant inputs and hardware complexity.

V. CONCLUSION.

Table 2 shows that proposed multiplier using reversible gates is better in terms of area power and delay as compared with conventional multiplier. Also it is efficient in terms of number of garbage outputs and constant inputs as compared with other reversible multipliers (Table 3).

However, we need synthesizing methods to minimize number of garbage outputs and constant inputs. We are short of simulation, synthesis, testing and verifying tools for designing reversible logic. But researchers around the world have been doing exciting research and making progress in this direction. Soon, reversible computing will become promising technology in near future.

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