VHDL Implementation Of 16 Bit ALU

Prof. Ravindra Joshi[1], Nagesh Naik[2], Nilesh Kashid[3], Sneha Waykar[4], Chirag Rangrass[5]

Department of Electronics and Telecommunication
KCCEMSR, Thane, India
nageshnaik@ymail.com

***Abstract*— In this paper VHDL implementation of 16 Bit ALU is proposed to be implemented. With help of 5 select lines, it has the ability to give the output for 32 different functions. Right from the basics of logical operations such as AND , OR , XOR to arithmetics like Addition and Subtraction; to higher operations such as binary to gray and concept of Floating Point operations. Floating point operations of addition, subtraction and multiplication will be performed along with use of new Floating point Format**

Keywords—VHDL, ALU, 16 Bit, Floating Point, new format)

I. INTRODUCTION

ALU is the heart of computing technologies and needs to improvise in all forms for additional functioning and flexibility of usage. Our proposed ALU has a facility for floating point number, thus allowing a large range of values to be operated on.

We have proposed to introduce a new floating point concept in form of a 16 bit floating point format. This format is to proposed to have a sign bit, a 5 bit exponent and a 10 bit mantissa

.

II. SOFTWARE

VHDL code is to be implemented with the use of VHDL synthesis tool Xilinx ISE. The program simulation is to be targeted for Spartan device

III. MAIN FEATURES

The main features will be:

- 16 bit data bus
- 16 bit processing
- 5 bit select lines for 32 functions
- 16 bit accumulator, 2 temporary registers and 2 working registers
- Ability to process floating point

IV. ARCHITECTURE

The figure alongside shows the architecture of the proposed 16 bit ALU. It shows the components as described in the previous point. Data bus is of 16 bit for both inputs and there are two temporary registers named as t1 and t2. Working registers are to be named as w1 and w2.

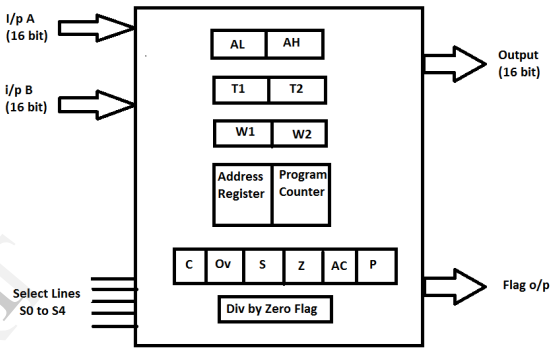

Fig 1. Block Diagram of the ALU.

Now let us have a look what is going to be the functioning of the proposed ALU. .

A. *Accumulator unit:*

The accumulator unit is proposed to consist of two 16 bit registers

i. AL: Lower 16 bit accumulator. To be used for general calculations and will be useful in the case of 16 bit multiplication where the output is more than 16 bits. In this case the lower 16 bits will be included in the AL register. When the output will be in the 16 bit format this register will be used.

ii. AH: Higher 16 bit accumulator. To be used only when result exceeds 16 bit . The excess bits are put in this register.

B. *Temporary Unit:*

- The temporary unit is to be used for operations which need temporary values to be stored.

i. The temporary registers are named as T1 and T2

ii. Both are 16 bit registers and have the ability to hold data when temporary data is to be held for particular operations

•

C. Working Register

It consists of 2 registers used for general calculations

i. These registers take data from the input lines or accumulator and then perform operations on it
ii. The result is then sent to the Accumulator section
iii. These are 16 bit registers

D. Flag Register:

The Proposed Flag Register has only status flags

i. Carry Flag: Shows the presence of carry being generated in a particular operation. Is useful for operations such as addition , subtraction and hence also for comparison
ii. Overflow Flag: Shows the overflow being generated. Useful especially in case of addition where higher bit may be lost
iii. Sign Flag: Indicates the sign of the given input value according to the general convention
iv. Zero Flag: Indicates the presence of Zero in Input or output
v. Auxiliary Carry flag: indicates the presence of carry between the number itself
vi. Parity Flag: Used to check parity of a given number
vii. Divide By Zero Flag: Special and important addition in the ALU. It indicates if the divisor of a division process is zero.

V. CONCEPT OF FLOATING POINT

The most important Feature of the proposed ALU is the ability to process Floating point values. We are glad that we have thought of a new floating point format for the same

IEEE single format floating point numbers use a 32-bit word. The first bit in the word is the sign bit, the next 8 bits are the exponent field, and the last 23 bits are the fraction field (for the fractional part of the significant).

+/-	00000000	00000000000000000000000

A. The proposed format:

The proposed Floating point format is has a sign bit, a 5 bit exponent and 10 bit mantissa.

This format is thus proposed to use a 16 bit word.

The proposed word format can be shown as follows

+ / -	0 0 0 0 0	0 0 0 0 0 0 0 0 0 0

The bias value for the format is 31. The max value attained by this format is 2147483648 in decimal number system. With the help of negative values is a total of 4.29 x 10^9 values can be operated on

This format will have special use in industrial applications which make use of smaller values for their operations

B. Functioning Of select lines:

We have proposed to make provision for 32 functions in this ALU. This will be made possible with the help of 5 select lines

TABLE I. FUNCTIONS

SELECT LINE	FUNCTION
00000	AND
00001	OR
00010	NOR
00011	XOR
00100	XNOR
00101	NAND
00110	NOT
00111	ADD
01000	SUB
01001	INCR
01010	DECR
01011	O/P=2^{ND} OPERAND
01100	ADD WITH CARRY
01101	SUB WITH BORROW
01110	1'S COMPLIMENT
01111	2'S COMPLIMENT
10000	SHIFT RIGHT
10001	SHIFT LEFT
10010	ROTATE RIGHT
10011	ROTATE LEFT
10100	COMPARATOR

10101	PARITY GENERATOR
10110	SHIFT RIGHT WITH CARRY
10111	SHIFT LEFT WITH CARRY
11000	ROTATE RIGHT WITH CARRY
11001	ROTATE LEFT WITH CARRY
11010	DECIMAL TO BINARY
11011	SIMPLE MULTIPLICATION
11100	SIMPLE DIVISION
11101	FLOATING ADDITION
11110	FLOATING SUBTRACTION
11111	FLOATING DIVISION

VI. CONCLUSION

Thus, we have proposed a 16 Bit ALU that has added functionality and ability to process floating point numbers. The added bias value makes sure of the accuracy of output.

REFERENCES

[1] IIANSIWEE Std. 754- 1985, IEEE Standard for Binary Flooring Point Arithmetic , IEEE NEwYork, 1985

[2] Suchita Kamble,Prof .N. N. Mhala,"VHDL Implementation of 8-Bit ALU" in IOSR Journal of Electronics and Communication Engineering (IOSRJECE) ISSN : 2278-2834 Volume 1, Issue 1 (May-June 2012), PP 07-11

[3] Lekshmi Viswanath, Ponni.M,"Design and Analysis of 16 Bit Reversible ALU" in IOSR Journal of Computer Engineering (IOSRJCE) ISSN : 2278-0661 Volume 1, Issue 1 (May-June 2012), PP 46-53.

[4] D. L. Perry, " VHDL", Tata Mcgraw Hill Edition, 4th Edition, 2002..

[5] J. Bhaskar, " VHDL Synthesis Primer", Pearson Education, 1st Edition,2002

[6] Computer Representation of Floating point numbers, Michael L. Overton

[7] J. Bhaskar, " VHDL Primer", Pearson Education, 3rd Edition, 2000