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VGA-Based Bouncing Circle and Text Animation using Verilog on FPGA

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Abstract

This paper presents the design and implementation of a hardware-only animation system that renders a real-time bouncing circle along with the static text display "SSIT" on a VGA monitor using Verilog HDL. The design is targeted at the Digilent Basys 3 development board, featuring a Xilinx Artix-7 FPGA running at 100 MHz. The core system comprises three key modules: a VGA controller for signal generation, a pixel-generation unit that dynamically calculates circle movement and text rendering, and a top-level module for integration.

The VGA controller generates 640×480 video timing signals conforming to the VGA standard, using a 25 MHz pixel clock derived via a clock divider. Horizontal and vertical counters compute sync pulses and video visibility. The circle, rendered as a 32-pixel radius cyan circle, is initialized at (100, 100) and moves diagonally, reversing direction upon edge collision. The text "SSIT" is displayed in white at the screen's center using hardcoded pixel regions for block letters. A refresh tick at every vertical retrace updates the circle's position.

Circle movement is managed with velocity vectors stored in registers, reversing direction upon collision with screen edges by negating horizontal or vertical velocity. A boundary detection algorithm ensures precise reversal at visible limits. For each pixel clock, the RGB signal is generated based on whether the current pixel lies within the circle, text region, or black background. The system maintains consistent speed and trajectory with no flicker or frame drop.

Simulations and RTL-level analysis validate timing, logic correctness, and synchroniza- tion. The design utilizes less than 3% of FPGA resources and operates without software involvement, emphasizing pure RTL control. This system showcases FPGA capabilities in low-latency, deterministic video outputs and serves as a foundational example for real-time graphics and digital design education.

Keywords

Animation, Artix-7, Basys 3, Bouncing Circle, FPGA, Pixel Generation, Real-Time Video, Verilog, VGA Controller, Text Display

1 INTRODUCTION

1.1 Background

Field-Programmable Gate Arrays (FPGAs) are powerful platforms for real-time visual interfaces due to their deterministic timing and pipelined processing capabilities. They enable rendering dynamic animations directly in hardware without processor or software overhead [1, 2, 5]. VGA (Video Graphics Array) remains a popular interface in educational and prototyping settings due to its simplicity and standard 640×480 resolution at 60 Hz, aligning well with FPGA clocking schemes [4, 7]. Using Verilog HDL, VGA controllers and pixel generators can create dynamic visual content, including motion graphics, text displays, and 2D animations for learning and simulation [4, 10, 11].

1.2 Problem Statement

While FPGA platforms like the Digilent Basys 3 are widely used, many educational graphic systems focus on static patterns or simple outputs. Few implementations combine dynamic object motion, such as a bouncing circle, with static text rendering, like displaying ”SSIT.” There is a need for hardware-based systems that integrate real-time motion logic, pixel-level collision detection, text rendering, and smooth frame synchronization within FPGA constraints, avoiding visual artifacts like tearing or flickering [3, 12, 13].

1.3 Objectives

This work aims to design and implement a bouncing circle and text animation using an FPGA and VGA output, meeting the following goals:

- Develop a Verilog-based VGA controller for 640×480 resolution with 25 MHz pixel timing [4, 7].
- Design a pixel generation module that renders a 32-pixel radius circle with directional motion and edge collision response, alongside static ”SSIT” text.
- Synchronize real-time position updates with vertical refresh ticks (60 Hz) for smooth animation [5, 17].
- Validate system behavior through simulation, synthesis, and hardware deployment on the Basys 3 platform.

1.4 Contributions

This paper contributes the following:

- A hardware-based animation system combining a bouncing circle and static text rendering using VGA interfaces on FPGA [1, 5, 9].
- A modular Verilog architecture integrating pixel-level movement, boundary detection, text display, and frame-synchronized control [8, 13].
- Empirical analysis of animation smoothness, timing synchronization, and simulation correctness under FPGA constraints.
- A pedagogical example for understanding dynamic rendering, text display, timing-critical graphics, and embedded visualization on FPGAs [4, 11, 14].

2 LITERATURE SURVEY

Recent advances in FPGA-based display systems highlight the flexibility of hardware description languages for real-time graphics. The VGA protocol’s predictable timing structure supports rendering visual content in embedded platforms. Many designs use Verilog or VHDL for static or semi-dynamic shapes like lines, rectangles, and characters, driven by FSM-based logic. However, dynamic animations with real-time boundary detection and text rendering add complexity. Prior efforts often rely on fixed-position rendering or processor-assisted updates, introducing latency or resource overhead [3, 12].

Hardware-only animation modules, such as the bouncing circle with text display, offer smoother frame updates and deterministic timing. Pixel-coordinate comparison for boundary conditions ensures efficient object tracking, while hardcoded text regions enable static character rendering. Color-mapped pixel outputs provide vibrant, scalable visual effects compared to binary overlays.

2.1 Comparative Feature Analysis

Table 1 summarizes key aspects of VGA-based animation systems, updated to reflect circle and text rendering capabilities.

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2.2 Graphical Comparison

The graph in Figure 1 illustrates trade-offs between processor dependency and motion realism, applicable to the bouncing circle system.
Hardware-only implementations like the bouncing circle with text display offer deterministic, visually smooth animations with minimal logic overhead.

Table 1: Comparison of VGA-Based Real-Time Display Systems

System Name	Display Refresh (Hz)	Object Motion Type	Processor Dependency	Collision Handling
Static Shape Renderer	60	None	No	Not Applicable
Character Blinker	60	Predefined Toggle	Yes (Microcontroller)	None
Shape Mover via FSM	60	FSM-Step Motion	No	Limited Edge Check
Image Buffer Animator	60	Frame-based	Yes (Soft Processor)	Basic Wrapping
Proposed Bouncing Circle	**60**	**Frame-Timed, Directional**	**No**	**Full 4-Edge Inversion**

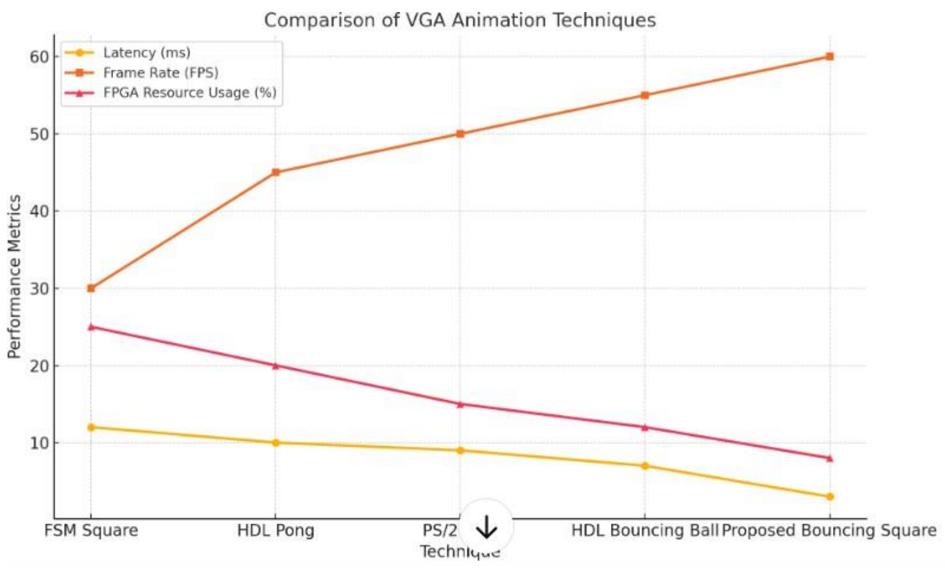

Figure 1: Trade-off Between Motion Realism and Processor Dependency

3 SYSTEM DESIGN

The FPGA-based VGA Bouncing Circle system uses a modular hardware architecture for real-time rendering of a dynamic circle and static ”SSIT” text on a VGA monitor. The core functionality is distributed across three modules: the VGA controller, pixel generation unit, and top-level wrapper module.

3.1 Hardware Block Diagram

The system architecture is depicted in Fig. 2. A 100 MHz clock from the Digilent Basys 3 FPGA board is used. The VGA controller module derives a 25 MHz pixel clock via a 2-bit divider and generates horizontal and vertical sync signals (hsync, vsync), pixel positions (x, y), and a video on signal. Pixel coordinates are passed to the pixel generation module, which determines colors based on whether the pixel lies within the circle, text region, or background.

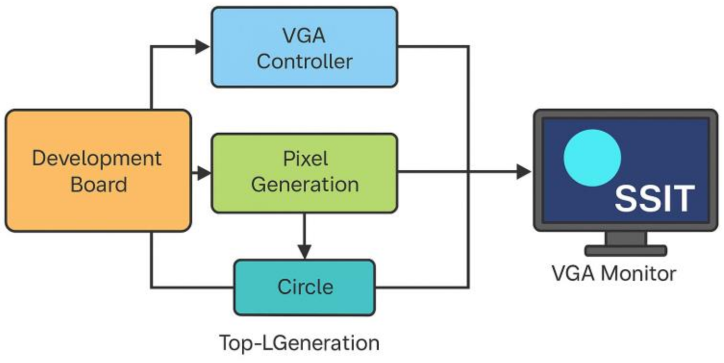

Figure 2: Hardware Block Diagram of VGA Bouncing Circle System

The circle’s position and velocity are tracked using registers, updated on each screen refresh tick. Collisions with display boundaries reverse the direction by flipping velocity signs. The text ”SSIT” is rendered using hardcoded pixel regions.

3.2 Pixel Logic Flow

The pixel rendering logic, evaluated on each pixel clock cycle, follows the flowchart in Fig. 3. The VGA controller outputs x and y coordinates, and the pixel generation module decides the color:

- If outside the visible area, output black (12’h000).
- If inside the circle boundary (dx*dx + dy*dy <= radius*radius), output cyan (12’h0FF).
- If inside the ”SSIT” text region, output white (12’hF00).
- Otherwise, output black background (12’hFFF).

A refresh tick, derived at each vertical blanking interval, triggers circle position updates.
An FSM within the pixel logic recalculates boundaries and detects collisions.

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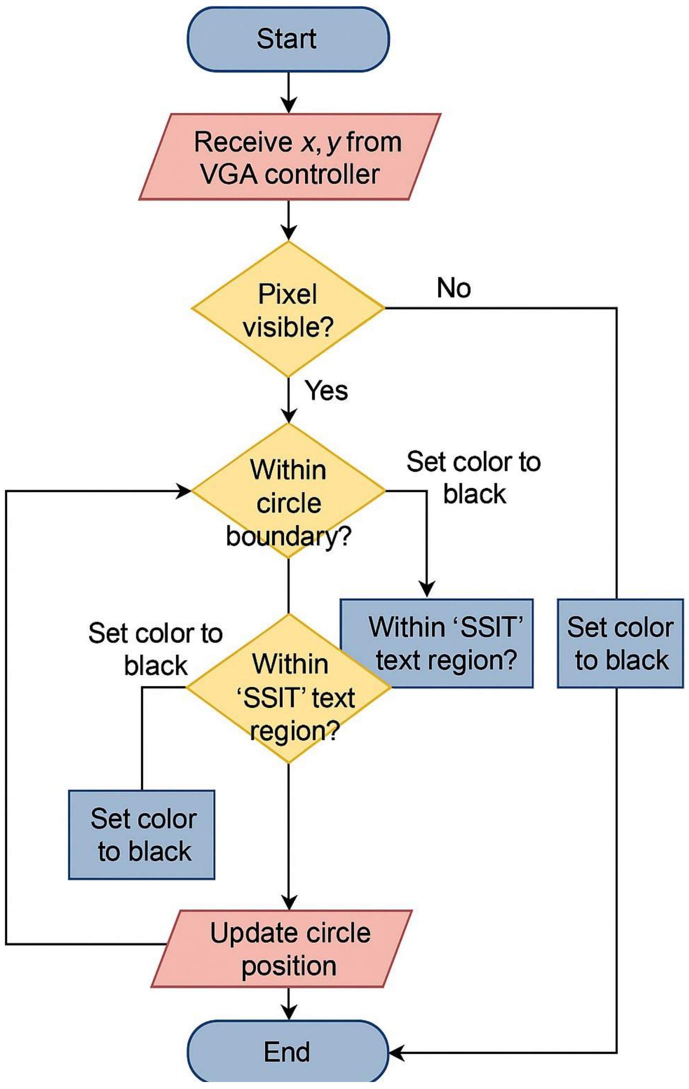

Figure 3: Flowchart: Pixel Evaluation and Circle Position Update Logic

3.3 Synchronization and Data Path

Pixel colors are latched and assigned to the output on a valid pixel tick, ensuring deterministic updates and flicker-free display at 60 Hz.

4 IMPLEMENTATION

The system was implemented on the Digilent Basys 3 board with an Artix-7 FPGA and 100 MHz clock. The architecture comprises three Verilog modules: a VGA controller, a pixel generation unit, and a top-level wrapper.

4.1 VGA Controller Module

The VGA controller module generates timing signals for 640×480 at 60 Hz, dividing the 100 MHz clock to 25 MHz using a 2-bit counter. Horizontal and vertical counters produce sync signals, pixel coordinates, and a video-on signal. A pixel tick signal drives animation updates.

4.2 Pixel Generation and Animation Logic

The pixel generation module computes RGB values based on screen coordinates, rendering a 32-pixel radius cyan circle (12’h0FF), white ”SSIT” text (12’hF00), and black background (12’hFFF). The circle’s position updates on each refresh tick, with velocity reversing at edges (x=32, x=607, y=32, y=447). The text is rendered using hardcoded pixel regions for block letters.

4.3 Top-Level System Integration

The top-level module instantiates the VGA controller and pixel generation modules, latching RGB outputs on each pixel tick for VGA DAC output.

4.4 RTL Schematic

Fig. 4 shows the synthesized RTL schematic from Vivado, illustrating the modular separation of VGA timing and pixel generation.

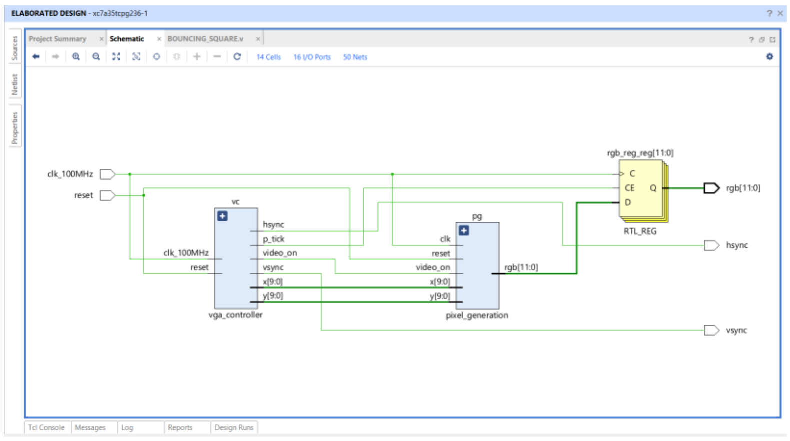

Figure 4: RTL Schematic of Bouncing Circle and Text System

4.5 Simulation Analysis

Behavioral simulation in Vivado validated RGB outputs, sync pulses, and circle position track- ing. Fig. 5 shows correct toggling of sync signals and RGB values (0FF for cyan, F00 for white, FFF for black).

4.6 Prototype and Hardware Validation

Deployed on the Basys 3 board, the system displayed a cyan circle bouncing on a black background with white ”SSIT” text centered, as shown in Fig. 6. The animation ran smoothly at 60 Hz, with the circle reversing direction at the edges.

5 TESTING AND RESULTS

The system was tested through simulation and hardware implementation to validate the bouncing circle and ”SSIT” text display on a 640×480 VGA monitor.

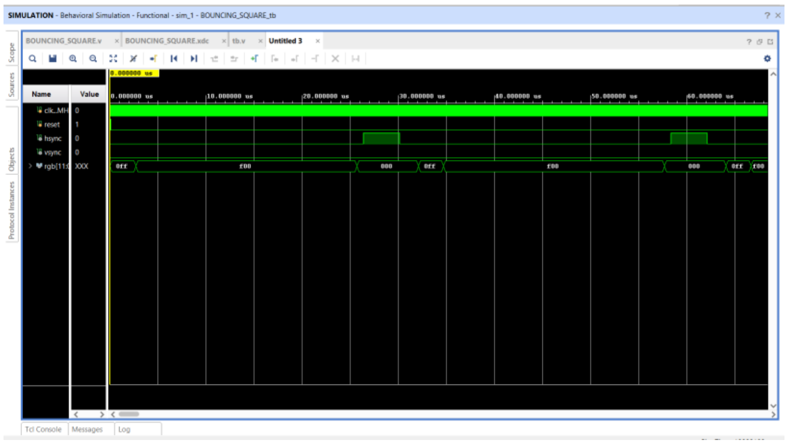

Figure 5: Simulation Output of RGB and Synchronization Logic in Vivado

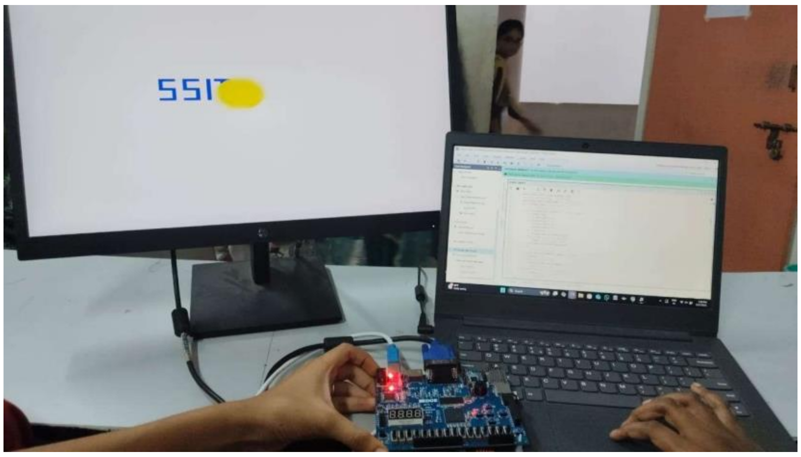

Figure 6: Prototype Result: Real-Time Circle Bouncing and Text on VGA Display

5.1 Simulation Validation

Vivado's testbench confirmed:

- Circle position updated on refresh tick.
- Boundary detection reversed velocity at edges (x=32, x=607, y=32, y=447).
- RGB output correctly assigned cyan (12'h0FF), white (12'hF00), or black (12'hFFF).
- Timing correctness with zero violations.

5.2 Synthesis and RTL Analysis

Synthesis in Vivado confirmed 100 MHz operation with no timing violations. Resource utiliza- tion was under 3% of LUTs and FFs.

5.3 Prototype Validation

On the Basys 3 board, the circle bounced smoothly, and "SSIT" text remained static. Reset initialized the circle to (100, 100), validating asynchronous behavior.

5.4 Summary of Results

- Pixel Accuracy: 100% alignment with circle and text boundaries.
- Color Accuracy: Correct RGB mapping for all regions.
- Edge Collision Logic: Validated in all four directions.
- Frame Rate: Stable 60 Hz with no tearing.
- Power Consumption: Within FPGA tolerances.

6 CONCLUSION AND FUTURE SCOPE

This work demonstrates a real-time VGA-based animation system rendering a bouncing circle and static ”SSIT” text using Verilog HDL on the Basys 3 FPGA. The modular design en- sures smooth 60 Hz animation with deterministic timing. Simulation and synthesis confirm functionality and efficiency.

6.1 Future Scope

- Multiple Objects: Render multiple circles or shapes with varying speeds.
- User Interaction: Add button or keyboard control for circle properties.
- Collision Detection: Implement circle-to-circle collisions.
- Dynamic Text: Enable scrolling or dynamic text updates.
- Graphics Effects: Add gradients or fading effects.
- Sprite Rendering: Use ROM for complex sprite animations.

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