Very Low Bandgap Voltage Reference with High PSRR Enhancement Stage

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Abstract—A low voltage bandgap reference with a high power supply rejection ratio is implemented in TSMC 90nm 1P9M 3.3V CMOS Process Technology.
Its power supply rejection ratio is improved by an enhancement stage so as to achieve a high performance analog and digital system which is usually limited by the PSRR of the bandgap reference. The design operates within a range of 2.6 to 3.6 V and has very small temperature and supply sensitivities measuring respectively. The circuit's current consumption is around 127.117 µA and produces an output voltage of 213.982 mV.

Index Terms—*Voltage Reference, Low Voltage Bandgap,Power Supply Rejection Ratio (PSRR).*

I. INTRODUCTION

Analog circuits incorporate voltage and current references extensively. Such references are dc quantities and exhibit little dependence on supply and process parameters and a well-defined dependence on temperature. The most common voltage reference circuit used in integrated circuits is the bandgap voltage reference due to its accuracy, reliability and compatibility with CMOS technologies [1]. A bandgap voltage reference circuit generates robust voltage against temperature, power supply and process variations [2]. The circuit is widely used to provide stable current and voltage references in analog circuits as well as mixed-mode CMOS circuits.

Conventional structures allow us to achieve a reference voltage of about 1.2 V with minimum sensitivity to temperature variation. Of course, when the supply voltage goes down below 1.2 V it is no longer possible to use the conventional structures and, also, designing the required operational amplifier becomes quite difficult.

Generally a bandgap reference circuit consists of a supply-independent biasing circuit, a diode connected BJT transistor generating a voltage with negative temperature coefficient, a PTAT circuit and some kind of feedback mechanism to improve the performance. In this paper, a measurement and addition circuit is implemented to output the reference voltage.Current mirrors with current feedback mechanism are used to minimize supply dependence. Feedback mechanism is implemented by a simple 2-stage single-ended differential amplifier. The circuit has been optimized for minimum temperature and supply dependence with simplest implementation.

A high power supply rejection ratio (PSRR) bandgap voltage reference circuit is desired to achieve high performance analog and digital systems. There are several techniques to achieve high PSR reference circuit but this paper's design approach involves designing a high gain operational amplifier with frequency compensation which can be supplied with low voltage and simple startup circuit to operate the bandgap voltage reference.

II. THE CIRCUIT

Bandgap Reference

A reference voltage is generated by adding two voltages that have temperature coefficients of opposite sign with suitable multiplication constants. The resulting voltage obtained is independent of temperature. The diode voltage drop across the base-emitter junction VBE, of a Bipolar Junction Transistor (BJT) changes Complementary ToAbsolute Temperature (CTAT). [3] Whereas if two BJTs operate with unequal current densities, then the difference in the base emitter voltages, ΔVBE, of the transistors is found to be Proportional To Absolute Temperature (PTAT). The PTAT voltage may be added to the CTAT voltage with suitable weighting constants to obtain a constant reference voltage.

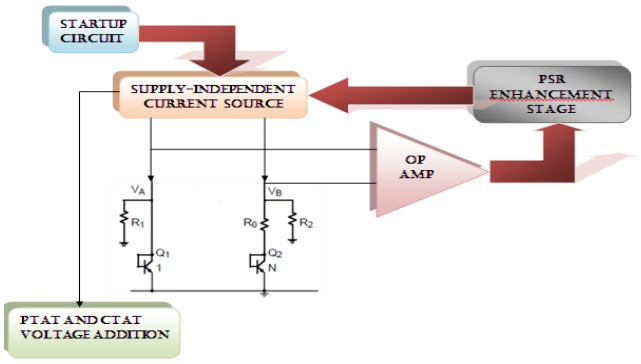

Fig:1 Bandgap Circuit Block Diagram

Supply Independent Current Source

The current mirror configuration of the PMOS transistors Mp1 and Mp2 shown in Fig. 2 is designed to have larger channel lengths so as to neglect channel length modulation and I_{ref} does not vary with VDD thus producing currents that are independent of the supply thus improving the PSR of the reference. The dependence on the OPAMP gain may be reduced if channel length modulation is minimized. A longer channel also improves circuit symmetry making it less sensitive to process variation and giving it the ability to generate stable currents. The transistors are sized to operate on a small V_{ds} *at* to achieve a low voltage bandgap core.

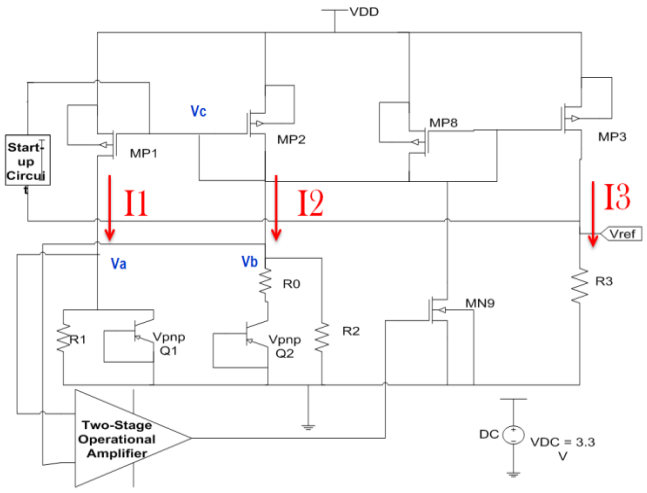

Fig:2 Bandgap Circuit Schematic

Startup Circuit

In the circuit of bandgap core, if all of the transistors carry zero current when the supply is turned on, they may remain off indefinitely because the loop can support a zero current in both branches. So it is needed to inject current in the bandgap core for proper operation of the circuit. Start up circuit does this job. This circuit also turns off when steady state is reached. A very simple start up circuit is used in this bandgap circuit.

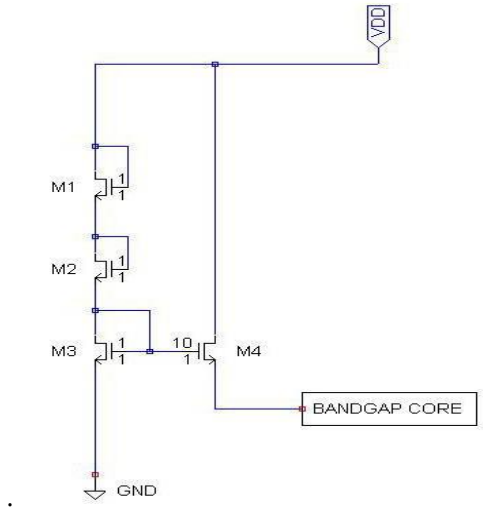

Fig:3 Startup circuit

Operational Amplifier

Operational Amplifier used in this circuit is basically a two stage differential amplifier. The main function of the operational amplifier is to drive the bandgap core. Operational Amplifier is designed in such a way that its output is insensitive to variation in supply. This helps to establish a reference voltage which is insensitive to supply.

The amplifier in Fig. is designed to have a high gain so as to make the start up circuit simple and to have a high PSR operational amplifier. Dominant pole frequency compensation is achieved by the compensation capacitor *C*, implemented as a MOSFET whereas the resistor *R* is added to improve the phase margin.

PSRR of the bandgap voltage reference in Fig. 4 is improved with the PSRR enhance stage consisting of PMOS M_8 and NMOS M_9. The PSRR enhancement stage not only increases the loop gain, but also effectively feeds the supply ripple into the PTAT loop.

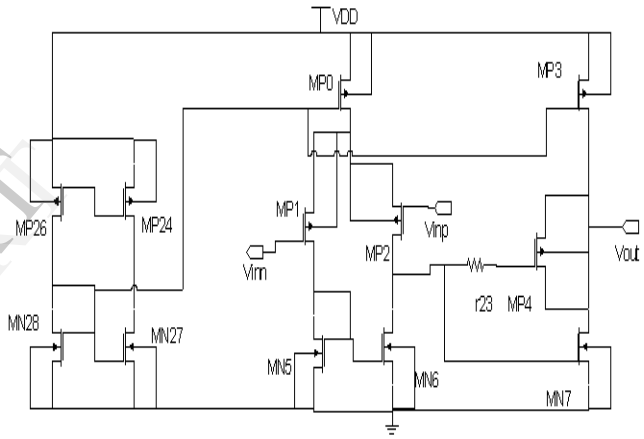

Fig:4 Two Stage Operational Amplifier

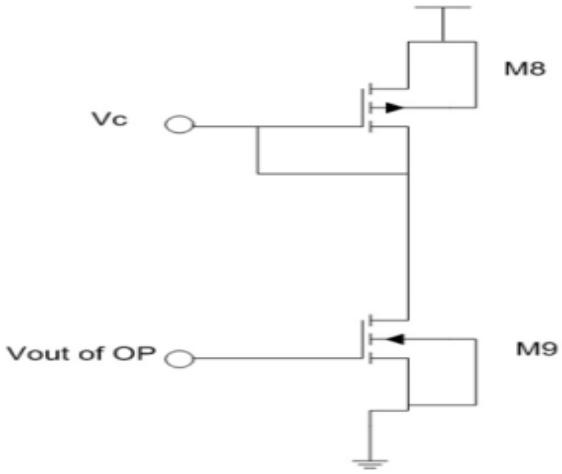

Fig:5 PSR Enhancement

The operational amplifier used has an excellent positive PSR due to its high gain and supply independent source. So the ripple at the output of the opamp can be neglected, thus the PSR at node V_c mainly depends on the "diode-connected" PSR enhancement stage, the "diode-connected" Mp_8 has a low impedance of $1/g_{m8}$, where g_{m8} is the transconductance of Mp_8. The PSRR at node V_c is given by (1)

$$A_{dd} = \frac{V_g}{V_{dd}} = \frac{r_{ds9}}{1/g_{m8}+r_{ds9}} \approx 1 = 0\,dB \qquad (1)$$

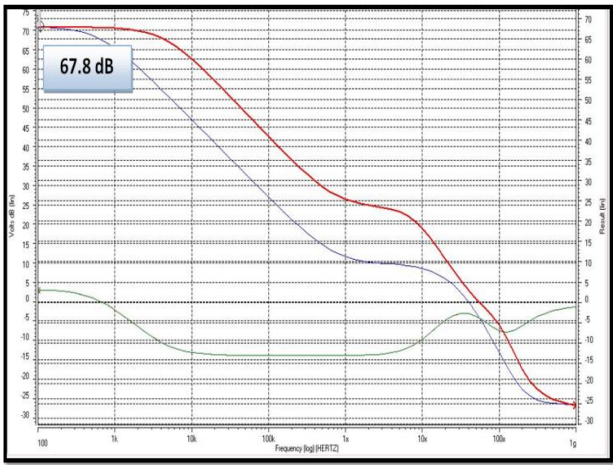

Fig:6 PSRR Simulation Result

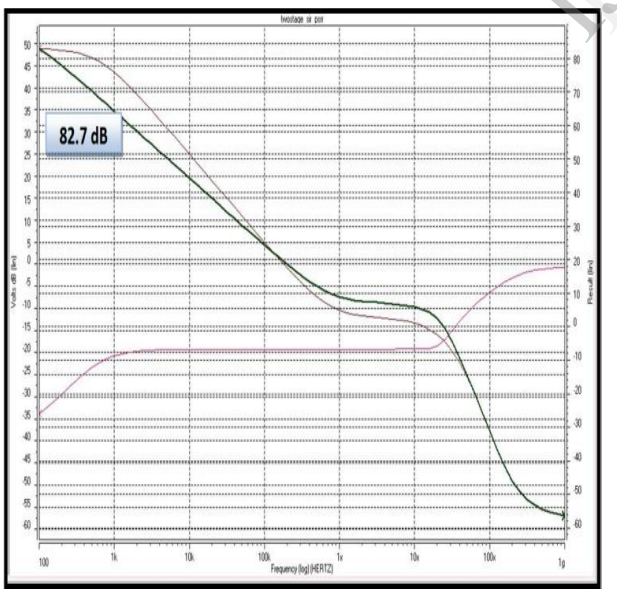

Fig:7PSRR Simulation Result after Enhancement Stage

!V . SIMULATION RESULTS

The simulation of the schematic was carried out in TSMC 90nm 1P9M 3.3V CMOS Process Technology. Figs. 8 and 9 show the performance of the design bandgap reference simulation of the temperature and power supply VDD independence, respectively. It also shows the pre and post simulation results comparison in TT corner using Synopsys Custom Designer tool. The design bandgap output voltage is measured with temperature variation of -20 to +120 °C and power supply variation of 2.2 to 3.6 V.

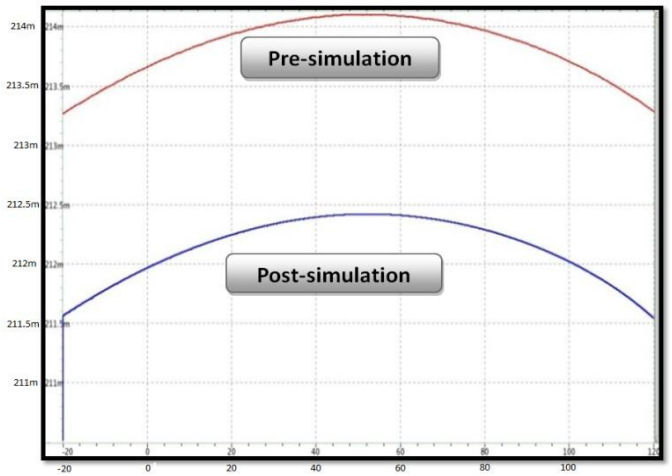

Fig:8 Temperature Variation (-20 to +120 °C)

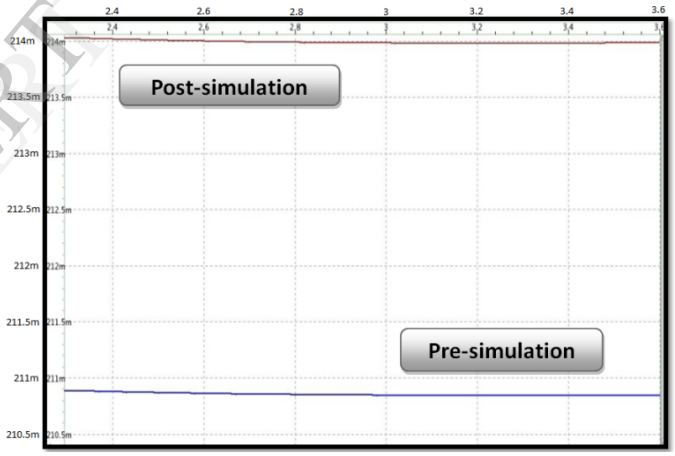

Fig:9 VDD Variation (2.2V – 3.6V)

V. CONCLUSION

The researcher was able to achieve a bandgap circuit design in *TSMC 90nm 1P9M 3.3V CMOS Technology Process* with a temperature sensitivity of 6 ppm/(°C) at -20 to +120 °C and supply variation sensitivity of 20 µV/V within the range of 2.6V to 3.6V. The circuit has a high PSRR value of is 82.7dB and consumes a total current of 127. 1169µA.

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