Vbyone To Lvds Conversion Using Kintex-7 FPGA

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Abstract— **In London 80 years back the first public demonstration of TV was held in a crowded laboratory. From there the journey of television was made a historic way. There were many changes in television such as analog transmission, digital transmission and also in the quality of video. Now the quality of video changed from 720p, 1080p, 2K, 4K and now at 8k. For 4k resolution video the frame rate will be 30Hz, because the present signaling standard can drive at this frequency. Vbyone is a signaling standard which is used for high speed data transmission and can drive frame rate at 60Hz. In this paper a video is being transmitted at a rate of 3.75Gbps using Vbyone and this video is interfaced with a 4k resolution LCD panel. But in the present scenario Vbyone cannot directly interfaced with the LCD panel. Using Lvds which is another signaling standard the video signals can be interfaced with the LCD panel. This paper implements the data acquisition from a Vbyone source and data transmission to a FPGA where the acquired Vbyone signal will be converted to Low voltage differential signaling standard and then transmitted to the LCD panel.**

Keywords—Vbyone, Lvds, High Speed Data Transmission

I. INTRODUCTION

After years of foresight High Definition has gone mainstream in professional video. High definition video contains a higher resolution than a normal resolution. Usually a video image more than 480/576 horizontal lines are considered as high definition video. The world is moving from standard resolution to high resolution. Generally high resolution videos have more number of pixels than standard resolution. So as the number of pixels is increasing the size of the video is also increasing. Each frame of high resolution video consists of more pixels compared with standard resolution.

As the size of the frames are increasing the bottle neck is high speed video transmission. 4k resolution at 60Hz is achievable through high speed data transmission. 4K resolution is known as ultra high definition resolution which is a generic term for display devices content which is having horizontal resolution on the order of 4,000 pixels. The television industry recently has adopted ultra high definition television as its 4K standard. For that purpose their needs dedicated signaling standard for high efficiency. In normal high speed data transmission lvds is being used. The major drawback of this signaling standard is that the speed is limited to 675Mbps. But the data rate for high definition videos will be equal to 3.75Gbps. In order to drive this much high data rate the signaling standard recommended is Vbyone which has a capability of 3.75Gbps data rate. V-by-One is originally developed to replace interfaces of digital pixel displays. LCDs have to use digital signaling to show their each pixel. However, the fact that LCDs required a higher definition

transmission, more color depth and also more frame rate, LVDS has a disadvantage that input pixel data for LCDs has increased and the number of LVDS cables also increased. Due to its higher-speed data transmitting ability, V-by-One expects to reduce the numbers of cables and connectors and thus the space in internal circuit and also the cost. Ultra definition panel which consists of 3840 horizontal and 216 vertical pixels requires only 16-pair cables with V-by-One technology. But Lvds needs 96 pairs of general cables. V-by-One also supports wide range of transmitting speeds. Engineers can interface Vbyone with significant changes from the existing LVDS interface. Since the panel cannot interface with Vbyone, Vbyone is converted to lvds using evaluation board of Kintex-7 FPGA (KC 705). The converted lvds is interfaced with the LCD panel.
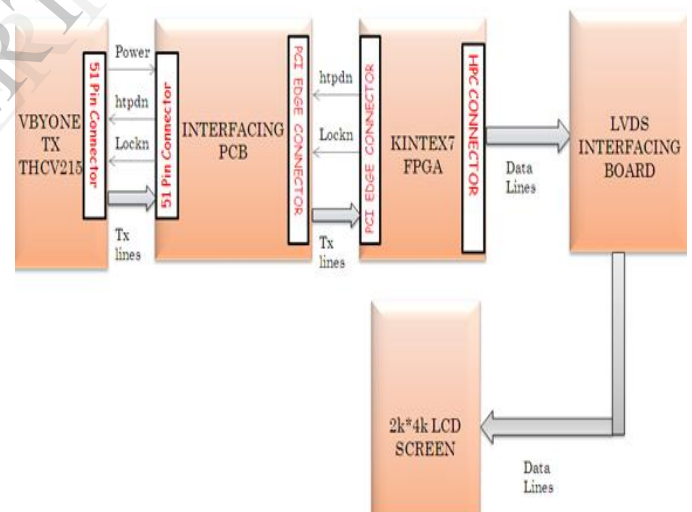
II. BLOCK DIAGRAM

Fig 1 Block Diagram

There are three stages.

1. Video generation and transmission
2. Video processing
3. Reception and display of video

A. Video generation and transmission

There is a FPGA board which generates a video which is used input signal. The FPGA board KC705 generates a color bar pattern of 3840*2160 pixels. The color bar is generated at a refresh rate of 60 frames per second. The generated video is given to a LVDS interfacing board. From the LVDS interfacing board it is given to THCV 215- 8 lanes. Here the

lvds input is converted to Vbyone and is transmitted. The data rate of video signals transmitted will be 3.75Gbps.

B. Video processing

The high speed data is given to an Interfacing PCB. Interfacing PCB consists of a level convertor for Lockn signal coming from the FPGA board. There is a 51 pin connector at the receiving side and a PCI edge connector at the transmitting side. The 51 pin connector is connected to the THCV215 board and the pci edge connector is connected to the pci edge connector in the FPGA board. The video signals will be transmitted through pci edge connector and will reach the FPGA. In the FPGA signal will be processed. The Vbyone is converted in to lvds and is transmitted from the HPC connector of the FPGA board.

C. Reception and display of video

The transmitted signals are received in an lvds board. The lvds board is connected to the 4k resolution panel.

III.   INTERFACING PCB

Interfacing PCB is used to interface the input signal to the FPGA board. Interfacing PCB consists of two connectors, two voltage regulators and one level shifter. There is a 51 pin connector at the receiving side of the interfacing board. There are 8 lanes of data lines. Differential signaling standard is used for data transmission. So each data line consists of differential signals. This is to reduce the noise and electromagnetic interferences in the signals. From the 51 pin connector the differential signals are given to pci edge connectors. There are two control signals from FPGA to the transmitting side which controls the transmission. They are the following

1.   HTPDN signal
2.   LOCKN signal.

Max current drawn from level shifter = 0.1mA
Power dissipated across 3.3v voltage regulator
   = (input voltage – output voltage) * current drawn
   = (12 – 3.3) * 0.1mA
   = 0.87mW

Power dissipated across 1.8v voltage regulator
   = (12 – 1.8) * 0.1mA
   = 1.02mW

Maximum power dissipated across Level shifter,
P (max) = (Tj (max) - Ta)/ θj-a

  Where   Tj the maximum junction temperature
               Ta the ambient temperature
               θj-a the ambient thermal resistance

P (max) = (125 – 25)/300
   = 0.33W

Power dissipated in voltage regulator is within the range of maximum power dissipation. Exceeding the maximum allowable power dissipation will cause excessive die temperature and the regulator will go down to thermal shutdown.

IV.   SYNC GENERATION

For Sync Generation there are four signals to be considered.

1.   Hsync
2.   Vsync
3.   Data enable
4.   Pixel Clock
5.   Data

Hsync is a signal which is generated before each horizontal scanning starts. Vsync is a signal which is generated before each frame starts. It needs to generate hsync, vsync, De, Pixel clock and data from FPGA. Hsync performs the horizontal scanning and vsync performs the vertical scanning. Based on pixel count (clock count) could generate vertical color bars. Based on line count (hsync) could generate horizontal color bars. Based on vsync could generate different frames.
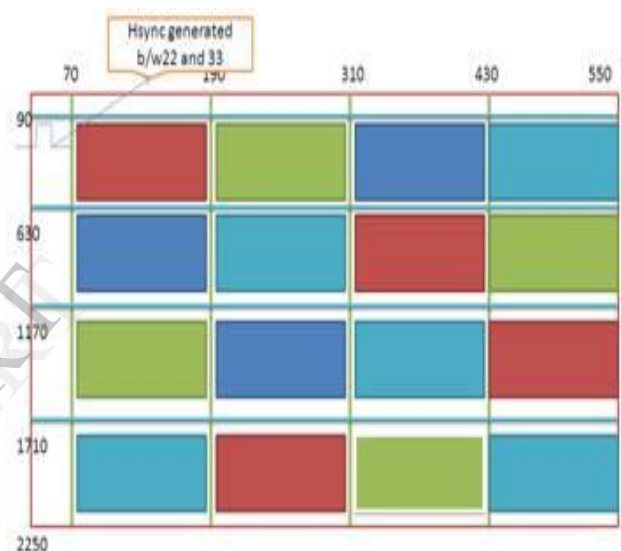

Fig 2 Color Bar

The total panel consists of 4400 vertical lines and 2250 horizontal lines. This includes the vertical front and back porch and horizontal front and back porch. In this the visible area consists of 3860 vertical lines and 2160 horizontal lines. The pixel clock frequency is calculated as horizontal lines * vertical lines * number of frames.

$$Pixel\ Clock = 4400 * 2250 * 60$$
$$= 594\ MHz$$

The FPGA cannot drive such a high frequency clock. So the pixel clock frequency is divide by 8 which gives 74.25MHz frequency. So 8 pixels are synchronized with the pixel clock frequency. In a single pixel clock 8 pixels will be scanned. Each pixel is 30 bit data. There are three primary colors for a video data. They are Red, Green and Blue. Each color is indicated by 10 bit. Thus total of 30 bits.

Horizontal active area is from 70 to 550 = 480 (clocks/ 8 pixels) and blanking (inactive) period is from 0 to 70 (which includes horizontal back porch, sync width and front porch). Vertical active area is from 90 to 2250 = 2160 (lines or hsyncs) and blanking (inactive) period is from 0 to 90 (which includes vertical back porch, sync width and front porch). For

Hysnc and Vsync are active high (during sync width/retrace hsync/vsync will be high). Each pixel clock contains 8 pixels. Hsync is generated for each line in between 22 and 33 pixel clocks. Vsync is generated for each frame in between.
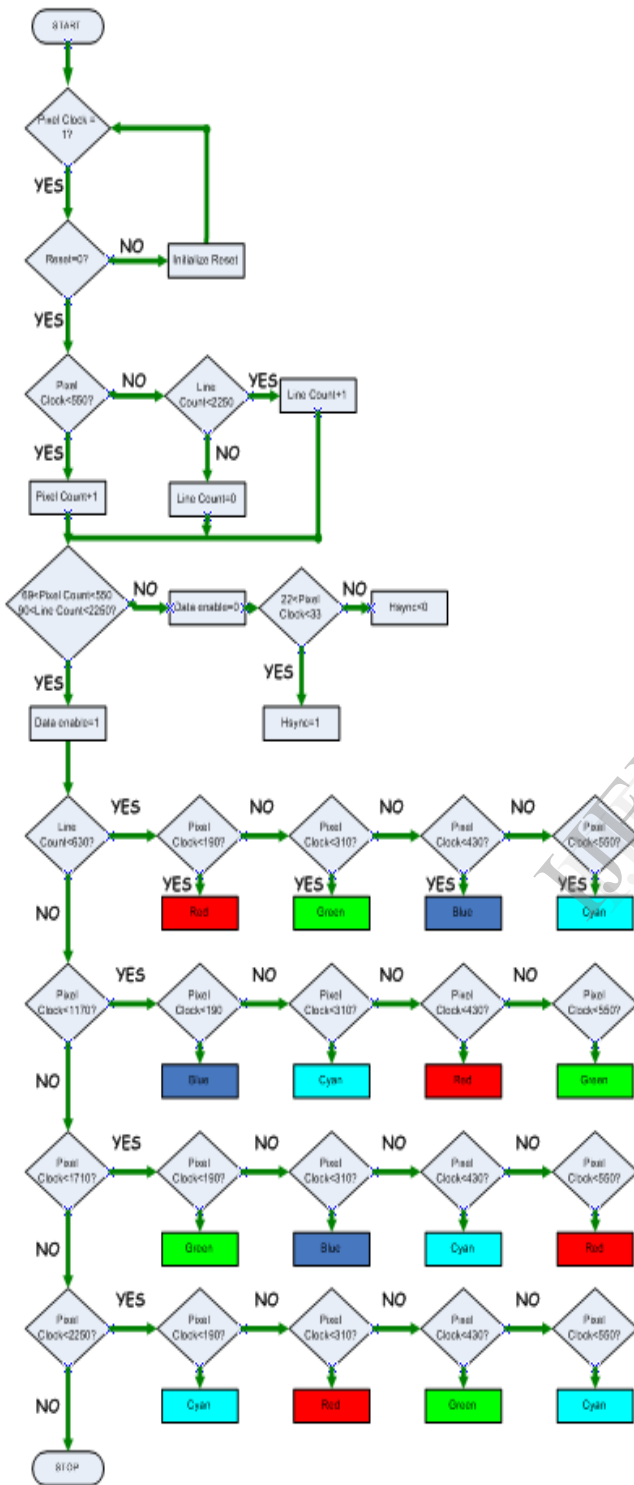

Fig 3 Flow Chart of Sync Generation

V. INTERFACING WITH BLOCK RAM

Kc-705 is the evaluation board for Kintex-7 FPGA. KC-705 contains Block Ram which is a primitive in FPGA. From the transmitter the signal is interfaced to the block ram of FPGA. Each Block Ram has 36Kbits of memory. 8 such Block Rams are used for data read and write operation. Each block ram will read and write 960 pixels. So 4 block ram is used for a single frame. For each frame the total pixels are stored in 4 block rams. Reading and writing from the block ram is done simultaneously.

On first Hsync high the data enable will be high, thus data will be written to Block Ram1. On the next Hsync high Block Ram 1 will be full thus Output Logic Block will show a high. When Block Ram 1 is full the next frame will be written to Block Ram 2 simultaneously Block Ram 1 will perform Read operation. Literally a ping pong operation will be followed. When one Block Ram is read other Block Ram will be written. But count the Output logic block high after the first Hsync then all together there will be missing one OLB high at the end which causes a pixel missing. In order to rectify this there needs a delay Hsync and data enable for one clock. For that have to initialize FIFO. The Hsync and data enable is called through the FIFO. Thus it is delayed by one clock. At the meantime Block Ram 1 will be full and simultaneously delayed Hsync will be high. This delayed Hsync will be used as reference for write and read from Block Ram 1 and Block Ram2.

VI. VBYONE TO LVDS CONVERSION

Oserdes is a serializing and deserializing unit which is a primitive in FPGA. Here the data coming will be serialized and then deserilaized. An Oserdes in FPGA converts the Vbyone signaling standard to Lvds signaling standard. Each pixel contains 30 bits. In these 7 bits which is transmitted parallel is converted to serial by Oserdes. 7 bits are serially converted to 1 line. So literally FPGA needs 5 Oserdes for one pixel and one line is exclusively for the clock. FPGA needs two clock signals, pixel clock and high frequency clock. These two clocks are phase aligned to ensure correct serialization in the oserdes. By using mixed mode clock manager two different clocks frequency is generated. An oserdes is a primitive which transmits 7 bit serial data. Parallel data coming will be serialized in oserdes. Each pixel contains 30 bits. Each line carries 7 bits so a total of 5 lines are required and one line is reserved for clock. Each line is connected to the LCD panel for display.

VII. RESULT

The video is seen in a 4k resolution LCD panel. LCD panel consists of 8 ports. Each port contains 5 data lines and 1 clock line. Each line is a differential pair. Through the 8 ports 8 pixels will be transmitting. Each pixel consists of 30 bits. As said one port contains 5 data lines and 1 clock line. 1 data line consists of 7 bits. So a total of 35 bits in which 5 bits will not be used.
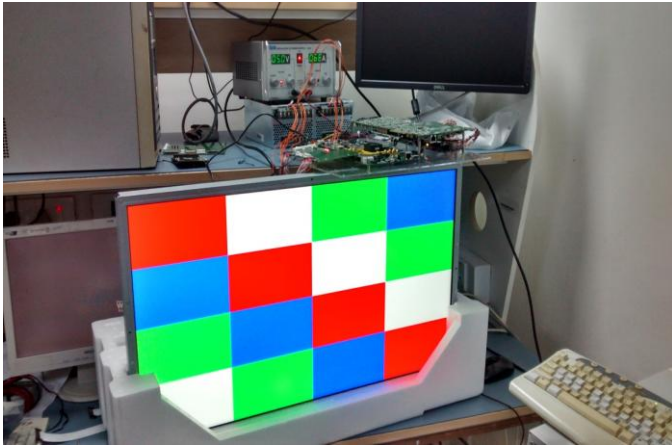
Fig 4 Result in 4K LCD Panel

VIII. CONCLUSION

High Definition television was first introduced in 1969. The system becomes mainstream in the late 1990s. In the early 2000s, there was a heavy competition in high definition TV market. Now from high definition the competition has grown to higher level which is ultra high definition. As the resolution is increased the frame rate also increased. For normal high speed data transmission signaling standards have lot of drawbacks such as low pixel clock, low data rate etc. Increased frame rate increases the picture quality. For high speed data transfer Lvds opts for more cables and thereby increases the size of the board. Whereas Vbyone reduces the cable size and number of connectors on the other hand has increased data transmission. So in near future Vbyone will be the signaling standard for high speed data transmission.

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