International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 11 Issue 06, June-2022

Various Full Adder based 32-Bit Wallace Tree Encoder

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***Abstract*: Now a days in Analog to Digital conversion using, an analog to digital converter (ADC), converts any analog signal into quantifiable data, which makes it easier to process and store, as well as more accurate and reliable by minimizing errors. Wallace tree encoder plays a crucial role and it based on converting thermometer code into binary code in ADC. In this project we design 32-bit Wallace tree encoders with Various Full Adder Techniques like CMOS, Pass Transistor Logic (PTL), Hybrid technique, Gate Diffusion Input (GDI) and Proposed Modified Gate Diffusion Input (M-GDI) Technique. The proposed MGDI technique provide Less Delay, Less Power Consumption, Better Power Delay Product and a smaller number of transistors compared to existing techniques. The proposed designs are designed and simulated using Mentor Graphics Tool with 90nm CMOS technology.**

***Keywords*: ADC, Wallace tree encoder, CMOS, PTL, GDI, MGDI, Hybrid**

I. INTRODUCTION

Speed, power dissipation and area are very important parameters of any VLSI based systems. Data conversion circuit plays an important role in high-rate data communications. Analog to Digital Converter (ADC) is an electronic integrated circuit used to convert the analog signals such as voltages to digital or binary form consisting of 1s and 0s. Most of the ADCs take a voltage input as 0 to 10V, -5V to +5V, etc., and correspondingly produces digital output as some sort of a binary number.

In analog to digital conversion process, Wallace tree encoder is utilized in the process of converting the thermometer code to binary. This can be termed to be a high-speed application and a flash type of flash ADC, which is a resistor ladder, encoder and comparator circuit. In electronics, an analog-to-digital converter (ADC, A/D, or A-to-D) is a system that converts an analog signal, such as a sound picked up by a microphone or light entering a digital camera, into a digital signal.

II. LITERATURE SURVEY

Yamini Shanmugam, Gopika Sundari P B, Rithika S and Sanjeev V (2021) proposed an "Comparative Analysis of Low Power Wallace Tree Encoder with Modified Full Adders". They designed a 16-bit low power Wallace tree encoder with modified full adders. Wallace tree encoder consumes more power so, by constructing low power, high performance Wallace tree encoder using PTL resistor ladder logic with modified full adders, the power can be conserved. To design this Wallace tree encoder, they used different types of full adders. The proposed design will be designed and simulated using Tanner EDA V16 tool. The proposed system aims in reducing the number of transistors to get better power efficiency and delay comparator. It has the advantage of correcting bubble error without the need of an extra bubble error correcting block. The proposed Wallace tree encoders are compared with other encoders using full adder. The results show that power consumption, delay and the power transistor count delay will be calculated. Finally, they are selected 16-bit low power Wallace tree encoder with modified full adders to improve high performance [1].

J.M. Mathana, R. Dhanagopal , R. Menaka (2020) proposed an "VLSI Architecture for High Performance Wallace Tree encoder". In the research, the VLSI architecture design for Wallace tree encoder with modified full adder is proposed. In the proposed work, a low power Wallace tree encoder is designed using only pass transistor logic (PTL) full adder. The circuit is designed using CADENCE 5.1.0 EDA equipped and simulated with the application of spectre virtuoso [2].

Rajkumar Sarma and Veerati Raju (2012) proposed as "Design and Performance Analysis of Hybrid Adders for High-Speed Arithmetic Circuit". In this research, a hybrid full adder is designed and analysis the performance for high-speed arithmetic circuit. In this paper, they proposed Gate diffusion technique (GDI) & PTL-GDI technique. Only 10 transistors are used to implement the SUM & CARRY function for both the designs. The SUM and CARRY cell are implemented in a cascaded way. By comparing both the techniques of adders the power delay product and power consumption will be observed. The significance of these designs is substantiated by the simulation results obtained from Cadence Virtuoso 180nm environment [3].

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III. IMPLEMENTATION

3.1 Existing Full Adders

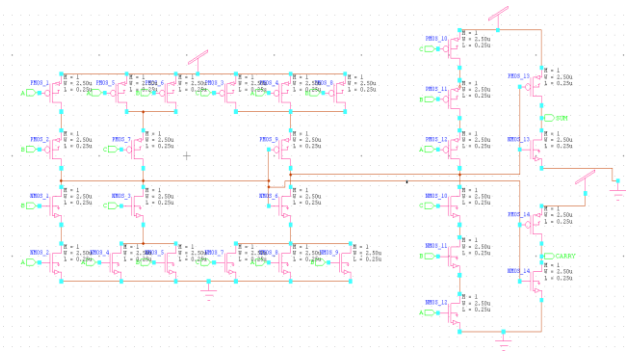

Figure 1: 28T CMOS Full Adder Schematic Diagram

One of the most well-known full adders is the standard CMOS full adder that uses 28 transistors as shown in figure. This design requires 28 transistors thus, the silicon area and the complexity are more for larger designs.

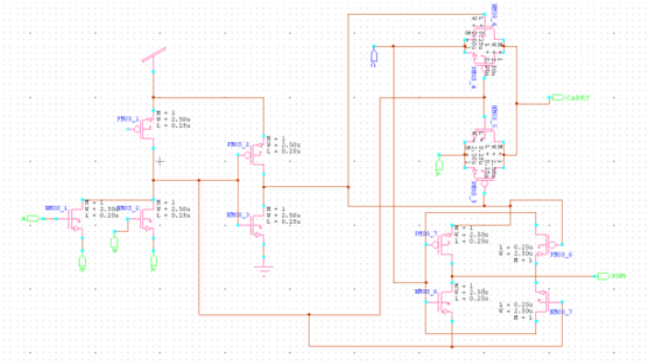

Figure 2: 13T Hybrid Full Adder Schematic Diagram

The Hybrid based Full Adder is shown in above figure. The adder is enhanced in a tree-like structure for further acceleration. It Reduces time delay. Has low energy and power consumption, smaller area can be achieved. Addition can be made faster. The area is also satisfyingly less because the proposed design used only 13 transistors.

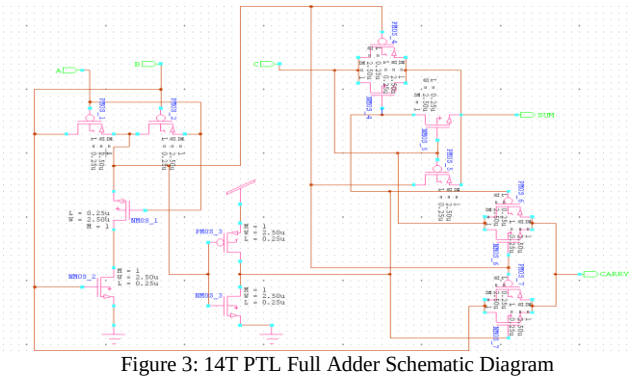

Figure 3: 14T PTL Full Adder Schematic Diagram

The PTL based Full Adder is shown in above figure. The design has totally 14 transistors using PTL technique. The 14Transistor full adder worked well with high performance with much less strength dissipation. On the other hand, the adder did not show the development in threshold strength loss. In addition, the 14Transistor full-adder would consume momentous power as compared to the other full adders.

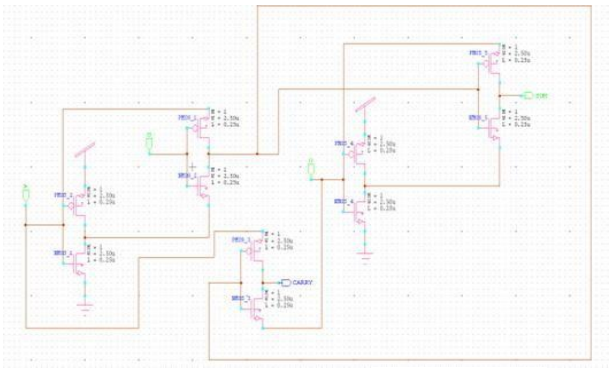

Figure 4:10T GDI based Full Adder Schematic Diagram

The GDI based Full Adder is shown in above figure. The design has totally 10 transistors using GDI technique. This in turn reduces the surface area and also the power dissipation.

3.2 Proposed Full Adder

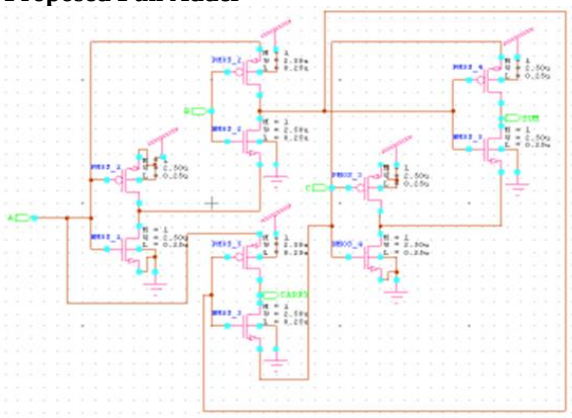

Figure 5:10T MGDI based Full Adder Schematic Diagram

10T MGDI full adder circuit design is mainly consisting of 10 transistors with modified technique. Sum and carry are the two expressions of the 10T MGDI full adder. The proposed full adder circuit has its low power and it contains lesser transistors when differentiated to the 10T gate diffusion full adder, the 13T hybrid full adder, the CMOS full adder. This is the best technique in low power applications. The benefits of 10T MGDI design are its speed. The operation of this full adder contains three inputs those are nothing but A, B, C and two outputs those are nothing but SUM and CARRY.

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3.3 Wallace tree encoder

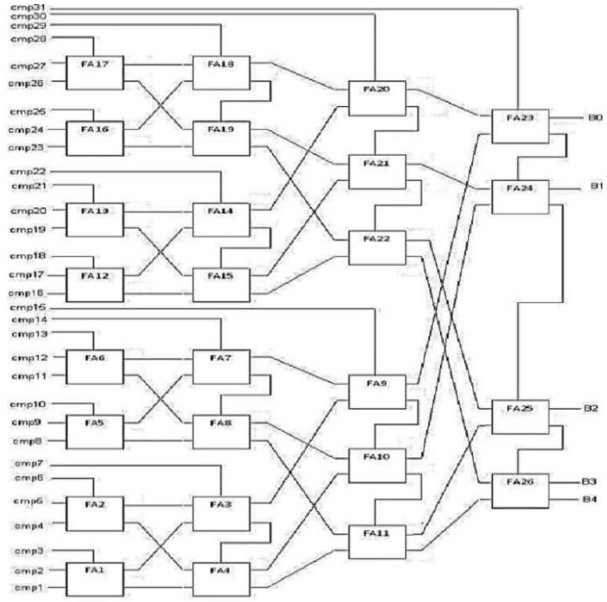

Figure 6: Block diagram of 32-bit Wallace tree encoder

Figure.3.2 shows a 32-bit Wallace tree encoder with full adder as its basic cell. The full adders count the number of logics "1" at their input to give final binary output. The full adders are arranged to sum the inputs so as to form Wallace tree. The Wallace tree encoder also called as one's counter is built with full adder cells. In analog to digital conversion process, Wallace tree encoder is utilized in the process of converting the thermometer code to binary.

IV. SIMULATION RESULTS

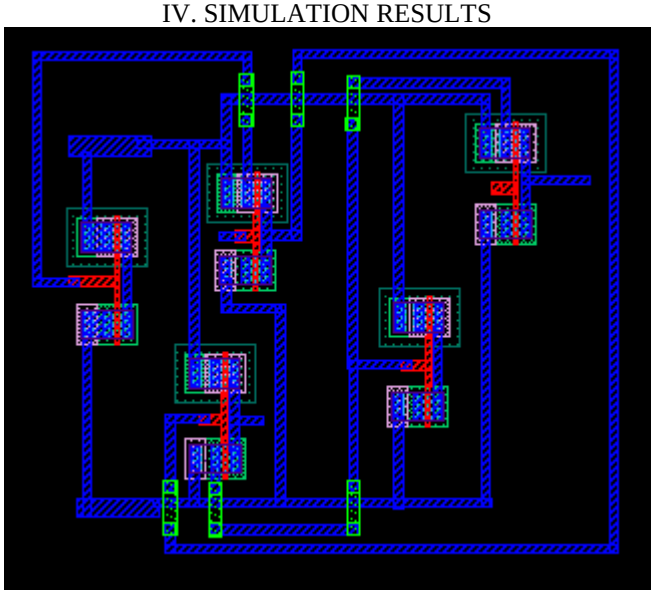

Figure 7: 10T Proposed M-GDI Based Full Adder Layout Diagram

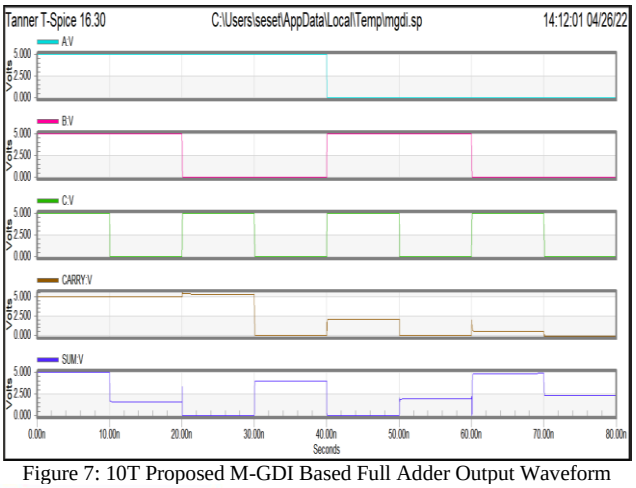

Figure 7: 10T Proposed M-GDI Based Full Adder Output Waveform

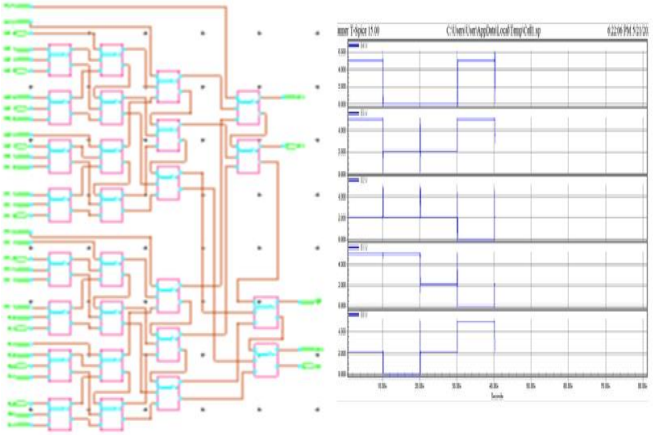

Figure 7: CMOS Based Wallace Tree Encoder Schematic Diagram and output waveform

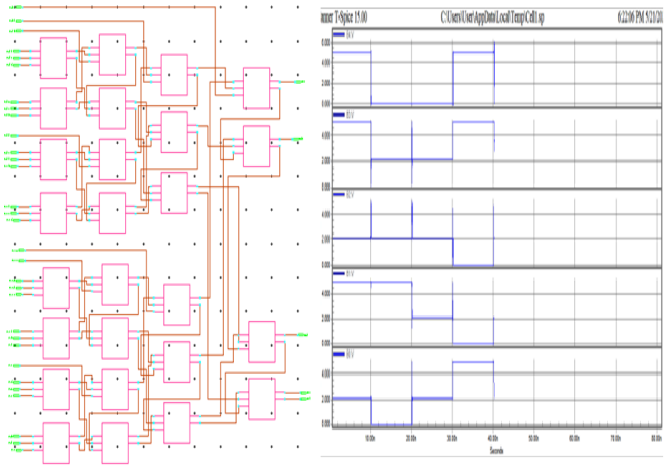

Figure 8: Hybrid Based Wallace Tree Encoder Schematic Diagram and output waveform

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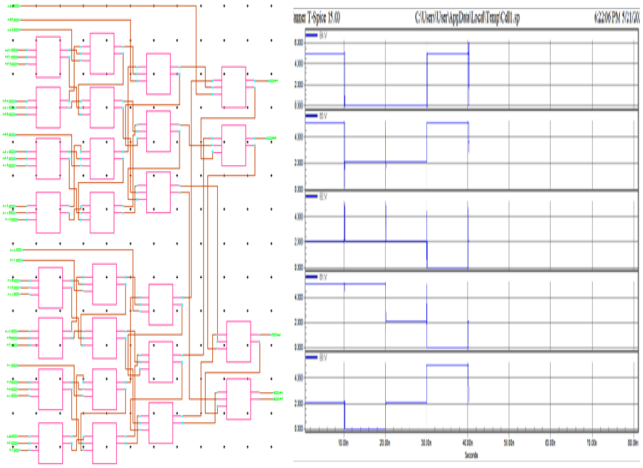

Figure 9: PTL Based Wallace Tree Encoder Schematic Diagram and output waveform

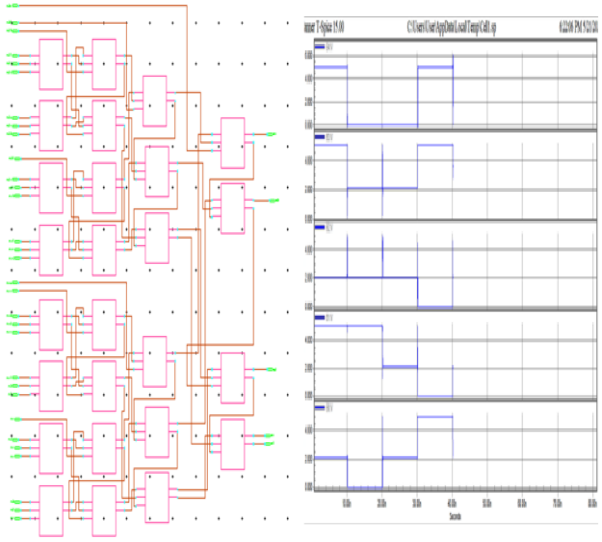

Figure 10: GDI Based Wallace Tree Encoder Schematic Diagram and output waveform

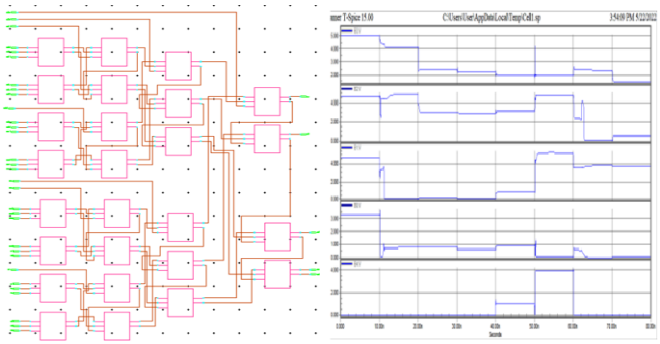

Figure 11: MGDI Based Wallace Tree Encoder Schematic Diagram and output waveform

4.1 Comparison Table

Table 1: Comparison between different Full Adders

FULL ADDERS	No. of T	POWER	DELAY	PDP
CMOS	28	0.3206uw	50.0518ns	1.6053e^-14J
PTL	14	0.62uw	40.0507ns	2.4831e^-14J
Hybrid	13	0.155uw	50.0518ns	7.75802e^-14J
GDI	10	0.536uw	40.0073ns	2.14439e^-12J
MGDI	10	0.532uw	30.0494ns	1.59864e^-19J

Table 2: Comparison between different Wallace tree encoder

Wallace Tree Encoder	No. of T	POWER	DELAY	PDP
CMOS	728	0.4171uw	30.220ns	1.2604e^-14J
PTL	364	0.218uw	40.05ns	0.87309e^-14J
Hybrid	338	0.195uw	40.55ns	0.79072e^-14J
GDI	260	33.42uw	30.550ns	1.0209e^-12J
MGDI	260	28.38pw	30.150ns	8.25509e^-19J

V. CONCLUSION & FUTURE SCOPE

5.1 Conclusion

Various Wallace tree encoders have been presented in this project such as MGDI Based 32-Bit Wallace tree encoder has the advantage of low energy, less computing complexity. It consumes the Power about 28.38pW which is less compared to other encoder and has a minimum delay of about 30.1501ns. The number of transistors required for designing Wallace tree encoder is 260. This reduces the complexity of the circuit. The circuit optimization is easy to detect the fault in the circuit. This is formulated using Mentor Graphics Tool with 90cm CMOS technology

5.2 Future Scope

Proposed Wallace tree encoder is designed for 32-Bit the design can be extended to higher resolution bit (64-Bit,128-Bit...). In this proposed design MGDI Based Full adder technique is used, in future it can be designed by using any other types of Full adder techniques. In proposed design Wallace tree encoder is used to converting the thermometer code into binary values, in future we can design ADC using different types of Techniques.

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International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 11 Issue 06, June-2022

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