Universal Logic Gates using Nano-Electro-Mechanical Switches

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***Abstract*—Nano-Electro-Mechanical Switches (NEMS) offer almost zero leakage in the off-state due to the absence of a pn junction and a gate oxide, as well as remarkable drive current in the on-state due to a metallic channel. Laterally actuated NEMS switches have little compensation more than the existing structures such as ability to co-fabricate the actuator, resistant to impact bouncing and free vibrations. This paper presents a novel design of NEMS logic gates using laterally-actuated double- electrode NEMS structures that can implement logic functions similar as logic devices that are made of solid-state transistors. The proposed logic gates uses only two NEMS switches instead of using 6-14 individual transistors as in CMOS. Then decreasing the transistor counts, our approach gives better yield, reproducibility, speed and reduce the complexities of making digital circuits such as adders and multipliers. One exclusive feature of this device is that it can work as either NAND gate or NOR gate functions with the same mechanical structure depending on the bias conditions of electrical interconnects.**

Keywords—laterally-actuated NEMS, NEMS switch, logic design, logic gates.

I. INTRODUCTION

The continuous improvement to increase the processing performance of electronic components has been attain by a constant reduction of the transistor size in metal-oxide semiconductor (MOS) technology. The increased performance of integrated circuits (ICs) is also associated with increase in packing density (i.e., the number of 'diminish' transistors in a single chip), which reduces cost. But these MOS devices cannot be used under extreme temperature and radiation conditions [1, 2] which limit their use in military and space applications. The physical limitations of the current technology have motivated researchers to look for alternative ways to process information for specific applications. The proposed NEMS logic gate is a NEMS device capable of performing Boolean logic functions, similar to conventional solid-state logic gates, still inheriting all the features of a MEMS switch and thus expected to have diverse range of applications than existing switches. NEMS switches are substitute for CMOS transistors in terms of resulting in higher efficiency, high isolation, near zero sub threshold leakage, extremely low sub threshold swing values [4, 3] etc. It also offers flexibility of making digital interface in the NEMS structure itself and thus reduces the difficulty of realizing NEMS based SoC(system on chip) systems[2]

J R et. al., [6] demonstrated the design of mechanical transistor which works like a conventional solid state transistor. It requires two laterally actuated double electrode NEMS device to implement the logic gates such as Inverter, NAND, NOR and Ex-OR. This paper presents a design of NEMS logic gates that can be fabricated by surface micromachining. In this configuration single mechanical structure can be used to perform logic functions such as NAND and NOR gate by changing electrical interconnect scheme externally.

II. BASIC DEVICE STRUCTURE AND OPERATING PRINCIPLE

NEMS switch is designed hinged on the principle of electrostatic actuation of cantilever beam. Fig.1 (a) shows a top view of the device structure which consists of two Gate electrode (Gate A & Gate B), Source (Cantilever beam) and Drain (Output). Gate electrodes can be excited separately for the deflection of cantilever beam by applying the voltage. If a potential difference endures between a Gate and the cantilever, the electrostatic force is created which deflects the beam towards that Gate. If the difference in voltage is greater than pull-in voltage of the beam then the cantilever beam touches the drain in the direction of the respective Gate (right or left). When the beam touches the drain the conduction path is created between source and drain. For instance, source is in VDD,the voltage applied to Gate A and Gate B are called configuration-1 and configuration -2 respectively.

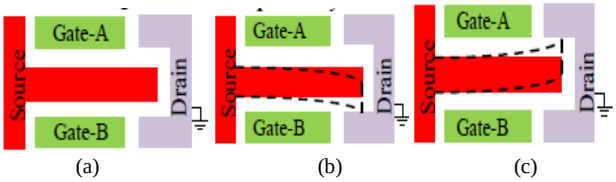
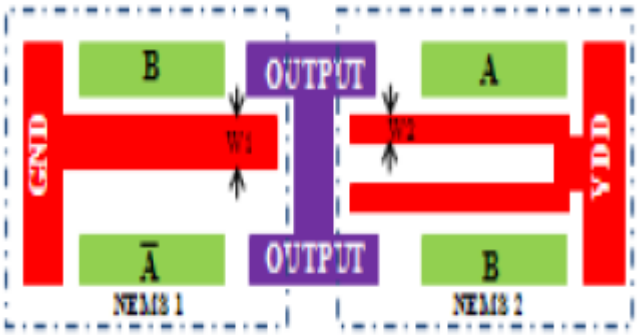


Fig1: Laterally-actuated double-gate NEMS switch (a) Top view (b) Operation of NEMS structure in configuration-1,(c)Operation of NEMS structure in configuration-2

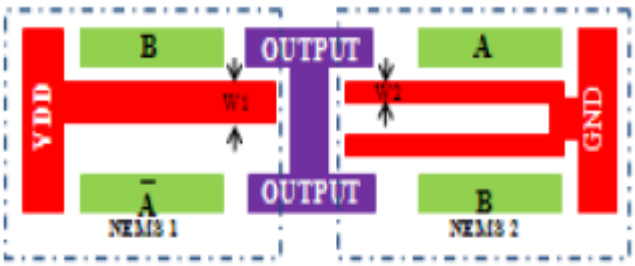
III. LOGIC GATE DESIGN

The NEMS switch based two input logic gates such as NAND and NOR gates realized using the laterally actuated double electrode NEMS devices are shown in Fig.2 and their

truth tables are summarized in Table 1. The NAND gate is implemented using two NEMS switches as shown in Fig.2 (a). The Fig.2(a) shows that the cantilever beam of NEMS1 is purposely intended to be a single wider beam than that of NEMS2 (W1 > W2) and is placed very nearer to input of B. On account of such realization, extra force is needed to deflect the cantilever of NEMS1 compared to that of NEMS2 since wider beams are stiffer. In this proposed design, W1 is selected such that when both the inputsare 'high', the beam can be bended to connect the drain terminal and to export the output as GND. The basic operation of the NAND gate can be illustrated as follows. If both the inputs are 'low', the cantilever of the NEMS2 deflected towards the output terminal to produce output as VDD. If only one of the inputs either A or B is 'low', NEMS2 again turns ON while NEMS1 stays OFF since the width of beam W1 is larger than W2, the electrostatic force created by NEMS1 is smaller than NEMS2. Lastly, when both inputs are high, NEMS1 is ON and inputs A and B can-not able to produce adequate amount of electrostatic force to turn ON NEMS2.Similarly implementation of NOR gate is shown in Fig.2 (b).Whereas altering the bias voltages on the NEMS1 and NEMS2, the logic function of the NAND gate changed into a NOR gate. Hence, the same mechanical structure perform as 'NOR' gate and 'NAND' gate with different electrical interconnects.



(a)



(b)

Fig.2.Design of gates using laterally-actuated double gate NEMS switch (Top view) (a) NAND (b) NOR gate

Table 1.Truth table for NAND and NOR gate

	NANDGate			NORGa		
	NEMS	NEMS	OUT	NEMS	NEMS	OUT
A='0'&B	OFF	O	1	O	OFF	1
A='0'&B	OFF	O	1	OFF	O	0
A='1'&B	OFF	O	1	OFF	O	0
A='1'&B	O	OFF	0	OFF	O	0

IV. NUMERICAL SIMULATION

To study the behavior of proposed NEMS logic gates, simulation is carried out using finite element MEMS design software CoventorWare. The material properties and dimensions used for simulation are listed in the Table.2.

Table.2: The material properties and geometry used for NEMS switch

Description	Value
Lengthof thebeam(*nm*)	500
Lengthof the Gate electrode(*nm*)	200
Width of the NEMS1 beam (W1) (*nm)*	35
Width of the NEMS2 beam (W2)(*nm)*	25
Distance between Gate electrode and beam (*nm)*	25
Young's modulus of the structure (*Gpa*)	160

V. CONCLUSIONS

The logic gates are designed using two double-electrode Nano-Electro-Mechanical Switches (NEMS) structures. Logic gates such as NAND and NOR gates are constructed using same mechanical structure by altering bias conditions of the electrical interconnects. The characteristics of the device are investigated using MEMS design CAD tool CoventorWare. This design simplifies the realization of arithmetic circuits such as adders and multiplexers.

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