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Ultralow-Voltage Schmitt-Trigger-Based SRAM Design

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Abstract

In this paper we are going to propose the differential sensing static random access memory (SRAM) bit cells for ultralow-power and ultralow-area Schmitt trigger operation. The ST-based differential sensing SRAM bit cells address the fundamental conflicting design requirement of the read versus write operation of a conventional 6T bit cell. The ST operation gives better read-stability as well as better write-ability compared to the standard 6T bit cell. The proposed ST based circuit will be having the feedback mechanism with in itself. The ST-2 bit cell is practically proved that it gives the ultra low power and ultra low are compared with the existing design. Design and Simulations will be done using DSCH and Microwind.

Index terms- *Read failure , Write failure, access time failure, Schmitt-Trigger*

1.Introduction

As rapid increase in the technology power and area plays a key role, so there is a need to maximize the battery life time with the low power requirement. There are more device-/circuit-/architectural-level techniques have been implemented to minimize the power consumption [1]. The overall power dissipation will depends on the supply voltage scaling. If there is any reduction present in the supply voltage then there will be reduction in the dynamic power and the leakage power quadratic ally and linearly (to the first order) respectively. By the reduction in the supply voltage, the sensitivity of circuit parameters to process variations will get increase. This causes to limit the circuit operation in the low-voltage regime and particularly for SRAM bit cells employing minimum-sized transistors [2].The combined effect of the lower supply voltage along with the increased process variations may lead to increased memory failures such as

read-failure, hold-failure, write-failure, and access-time failure [4]. The process constraints such as gate-oxide reliability limits are used to determine the maximum supply voltage V_{max} which is used for the transistor operation. V_{max} is getting reduce with the technology scaling due to scaling of gate-oxide thickness. The minimum SRAM supply voltage (V_{min}) for a given performance requirement is limited by the increased process variations i.e., both random and die-to-die and the increased sensitivity of circuit parameters at lower supply voltage. Moreover, to enable SRAM bit cell operation across a larger voltage range V_{min}, has to be further minimized to low. In the case of six-transistor bit cell, the SRAM V_{min} can be lowered with out adding extra transistors. In this work, we focus only on various configurations of bit cell. Hence, We believe that to reduce the V_{min} we apply the read-write assist circuits to these bit-cell configurations.

The remainder of this paper is organized as follows. Section I describes Introduction, Section II describes various existing SRAM bit cells. Section III briefly presents the Schmitt-Trigger (ST)-based SRAM bit cells. Section IV shows the detailed V_{min} comparison of various bit cell topologies. Section V presents the results. Section VI summarizes the low-voltage SRAM design discussion.

2.Existing SRAM Bit Cells

The existing SRAM bit cells have been developed with different design goals such as low power, bit density, architectural timing specifications, bit cell area and low voltage operation. As shown in the below Fig.1, the 6T bit cell is having the two crossly coupled inverters, which is the de facto memory bit cell used in the present SRAM designs.

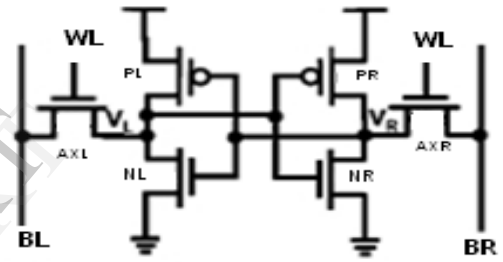
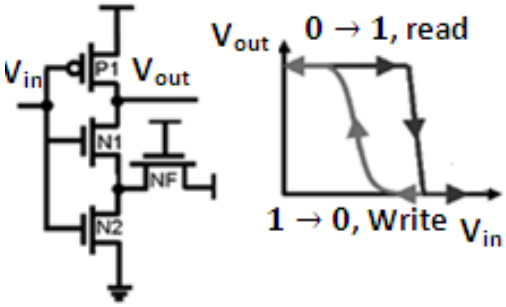


Fig.1. Conventional 6T SRAM bit cell configuration

By modulating the virtual-VCC and virtual-VSS of one of the inverters the write ability will be achieved. In all the existing bit cell configurations the cross-coupled inverter pair plays a vital role. To decouple the read and write operations we need to add the extra transistors. None of the existing bit cells incorporate process variation tolerance for improving the stability of an SRAM bit cell. The stability of the cross-coupled inverter will decides the SRAM operation under PVT variations.



Input transition dependent characteristics

Fig.2. Conceptual ST schematics: the gate connection of the feedback transistor is connected to the VCC to show the feedback mechanism during $0 \leftarrow 1$ input transition.

However, the bit cell stability can not be affected by the device sizing at very low supply voltage. For successful low voltage SRAM design in nano scaled technologies we need a different approach. The proposed Schmitt Trigger based SRAM bit cell having built-in feedback mechanism that exhibits the process variation tolerance with ultra low power and area

3.Schmitt Trigger SRAM Bitcells

To resolve the conflicts present between the read and write design requirements in the conventional 6T bit cell, we need to apply the Schmitt Trigger (ST) principle for the cross-coupled inverter pair. Depending on the direction of the input transition, the Schmitt trigger will modulate the switching threshold of an inverter. The feed back mechanism is used in the pull-down path in this proposed ST SRAM bit cells, as shown in Fig. 2. By raising the source voltage of pull-down n MOS(N1), the feed back transistor (NF) tries to preserve the logic "1" while the input transition is made as $0 \rightarrow 1$. This results in higher switching threshold of the inverter with very sharp transfer characteristics. Since a read-failure is initiated by a $0 \rightarrow 1$ input transition for the inverter storing logic "1," higher switching threshold with sharp transfer characteristics of the Schmitt trigger gives robust read operation. During the $0 \rightarrow 1$ transition the feedback mechanism is not present. This results in smooth transfer characteristics that are essential for easy write operation. Thus, input-dependent transfer characteristics of the Schmitt trigger improves both read-stability as well as write-ability of the SRAM bit cell. The two proposed bit cell designs are as follows.

A. ST-1 Bit cell

Fig. 3 shows the schematic diagaram of the ST-1 bit cell. The ST-1 bit cell utilizes differential sensing with ten transistors, two bit lines (BL/BR),and one word-line (WL). Transistors PL-NL1-NL2-

NFL, PR-NR1NR2-NFR form another ST inverter. Feedback transistors NFL/NFR raise the switching threshold of the inverter during the $0 \rightarrow 1$ input transition giving the ST action. Detailed operation of the ST-1 bit cell can be found in [6].

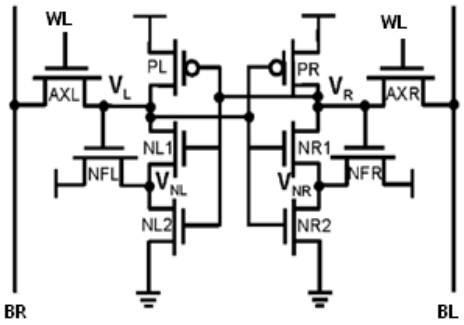
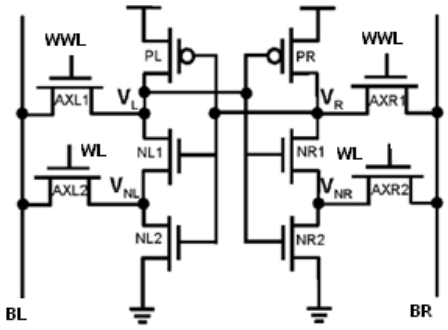


Fig.3. ST-1 bit cell schematic diagram.

B. ST-2 Bit cell

Fig. 4 shows the schematic diagram of the ST-2 bit cell utilizing differential sensing with ten transistors, two word-lines (WL/WWL), and two bit lines (BL/BR). The WL signal is asserted during read as well as the write operation, while WWL signal is asserted during the write operation. The WL and WWL are remains OFF during hold -mode. In the ST-2 bit



	WL	WWL
Read Mode	**1**	**0**
Write Mode	**1**	**1**
Hold Mode	**0**	**0**

Fig.4. ST-2 bit cell schematics

cell, feedback is provided by separate control signal (WL) unlike the ST-1 bit cell, where in feedback is provided by the internal nodes. In the ST-1 bit cell, the feedback mechanism is effective as long as the storage node voltages are maintained. Once the storage nodes start transitioning from one state to another state, the feedback mechanism is lost. To improve the feedback mechanism, separate control signal WL is employed for achieving stronger feedback. Detailed operation of the ST-2 bit cell is explained in our earlier work .

4. SRAM Bitcell V_{min} Analysis

A. Iso Area Bit cells

The ST bit cells consumes approximately 2X area compared with the 6T min cell [6]. Hence, in order to estimate the minimum supply voltage V_{min}, it is only fair to compare the bit-cells under iso area condition.. In general, the SRAM bit cell area is dominated by the contact and the diffusion spacing. Careful examination of various industrial minimum–sized 6T bit cell layouts reveal that only 30%–35% of the lateral dimension contributes to the device widths while remaining lateral dimension is used for the contact and diffusion spacing. Note that, the channel lengths of SRAM transistors may not be set to arbitrary value in a scaled process due to lithography limitations. Increasing the channel length increases bit cell area along the bit line direction. This would increase the bit line capacitance and hence the bit-line power consumption. Since bit line power is the dominant component of the overall power consumption, the vertical dimension along the bit line is unchanged (=2poly-pitch) for the bit cell upsizing. Any upsizing is realized in the lateral direction by increasing the device widths along the word-line. This would increase word-line capacitance and hence word-line switching power. However, only one word-line in the sub array is active during a read/write operation. Hence, this approach of bit cell upsizing would result in minimal increase in power dissipation

1.6T Iso-Area Bit cell:

In this work, we use 6T min cell device widths of 100, 100, and 200 nm for pull up/access/pull-down transistors, respectively. We can upsize the 6T min cell in various ways. If the bit cell is upsized to be more read-stable, it would affect its write-ability and vice versa. Hence, all transistors in the 6T min cell are upsized uniformly to improve the read-stability and write-ability simultaneously. As seen in Fig. [5], increasing device widths linearly increases the bit cell area sub linearly. For 2X larger area, the 6T min cell device widths need to be upsized by 4XThe bit cell area is estimated following the layout rules and the differential sensing is assumed to be 50% and 70%

respectively

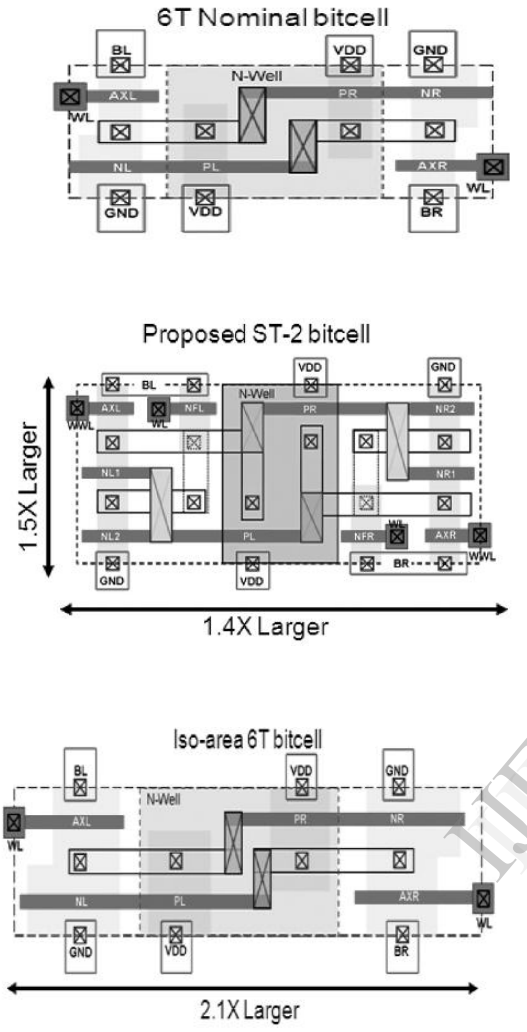


Fig.5.Transistors are upsized by 3 compared to the 6T min cell case

B. Read-Failure Probability

Read static noise margin (SNM) is used to quantify the read-stability of the SRAM bit cells. The SNM is estimated graphically as the length of a side of the largest square that can be embedded inside the lobes of the butterfly curve. Read-failure probability ($P_{read\text{-}fail}$) is estimated as

$$P_{read\text{-}fail} = probe.(\text{read SNM} < kT).$$

If read SNM is lower than the thermal voltage (kT= 26 mV at 300 K), the bit cell contents can be flipped due to thermal noise. Note that any other suitable threshold criteria can be used in estimating read-failure probability. Read-V_{min} is determined at the 6-sigma read-failure probability (i.e $P_{read\text{-}fail= 1e\text{-}9}$).

Fig. 6. plots read-failure probability versus supply voltage for various 6T bit cell sizing. It is found that built-in process tolerance in the ST-2 bit cell gives lower read-failure probability compared with the iso-area 6T bit cell.

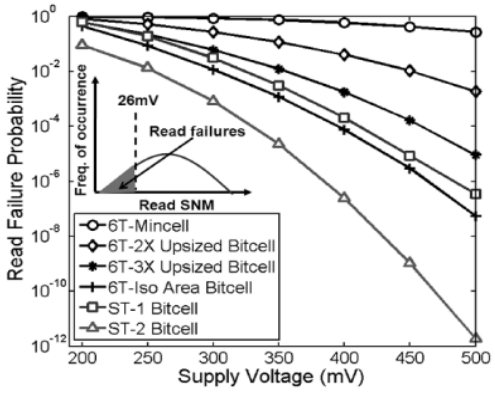


Fig.7. 6T versus ST bit cell: read-failure probability comparison.

C. Hold-Failure Probability

Similar to the read stability case, hold-stability is estimated by computing the hold SNM. Fig. 8 shows the hold-failure probability variation versus supply voltage for 6T and ST bit cells. As shown in inset, hold-failure probability ($P_{hold\text{-}fail}$) is estimated as

$P_{hold\text{-}fail}$ = *prob*.(hold SNM *k*T).

Hold-V_{min} is determined at the 6-sigma hold failure probability (i.e., $P_{hold\text{-}fail}$ =1e-9). It is observed that upsizing 6T device dimensions give robust inverter characteristics. This gives lower hold-failure probability and lower hold-V_{min} compared to the minimum sized ST-1 and ST-2 bit cells. Note that ST-1 bit cells having internal node-based feedback give improved hold-failure characteristics compared with the ST-2 bit cell. For the ST-2 bit cell, WL and WWL control signals are OFF during the hold-mode (Fig. 4).

D. Write-Failure Probability

Write-ability of a bit cell gives an indication of how easy or difficult it is to write to the bit cell. Fig. 9 shows the write-failure probability variation versus supply voltage. As shown in inset, write-failure probability ($P_{write\text{-}fail}$) is calculated as

$P_{write\text{-}fail}$ = Prob.(write-trip-point < 0 m V)

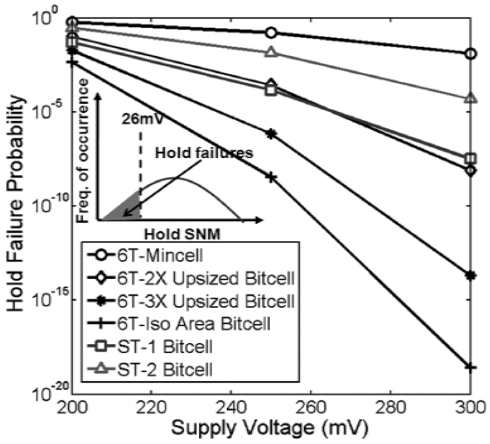


Fig.8. 6T versus ST bit cell: hold-failure probability comparison.

$P_{write\text{-}fail}$ = Prob.(write-trip-point < 0 m V)

Write-V_{min} is determined at the 6-sigma write-failure probability (i.e., $P_{write\text{-}fail}$ = 1e-9). In case of ST-1 and ST-2 bit cell, absence of a feedback mechanism and series-connected pull-down n MOS transistors result in higher write-trip point compared with the 6T bit cell. Consequently, the proposed ST bit cells give lower write-V_{min} compared with the 6T bit cell. For ST-2 bit cell, WL and WWL control signals are asserted, resulting in lower write-failures compared with the ST-1 bit-cell.

Fig.9. 6T versus ST bit cell: write-failure probability comparison

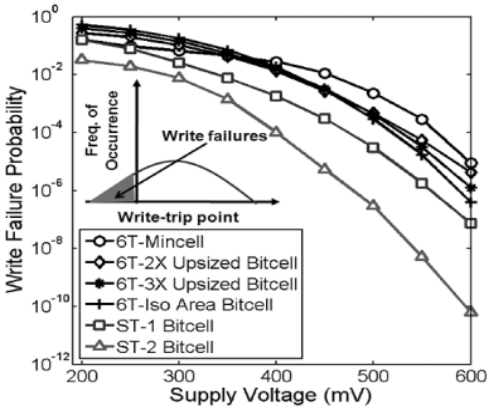


Fig.9. 6T versus ST bit cell: write-failure probability comparison.

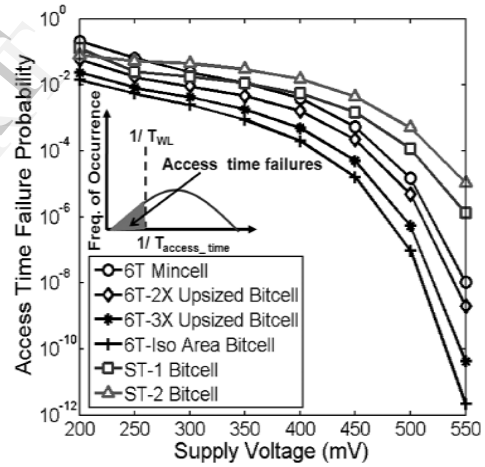
E. Access-Time Failure Probability

Access-time (T_{access}) is defined as the time required to produce a pre specified voltage difference ($\Delta V_{BL} \approx$ 50 mV) between two bit lines. If this bit line differential is less than the sense amplifier input offset voltage, sense amplifier's output may not resolve correctly resulting in incorrect data value. For a given supply voltage, the access-time failure depends on array organization viz. bit cell read-current, bit line capacitance (number of bit cells/column), word-line pulse-width, bit line leakage, column multiplexer series resistance and sense amplifier offset voltage. Hence, access-time failure probability ($P_{access\text{-}time\text{-}fail}$) is calculated as

$$P_{access\_time\_fail} = prob.(1 \div T_{access} < 1 \div T_{WL})$$

Where T_{WL}= word-line pulse-width. And Access – V_{min} is determined at the 6-sigma access time failure probability (i.e.,$P_{access\_time\_fail}$ =1e-9)

Fig.10. 6T versus ST bit cell: access-time failure probability comparison.



.Access time failure probability variation versus supply voltage for 6T and ST bit cells. It is found that upsized 6T bit cells give higher read-current compared with ST-1 and ST-2 bit cells, resulting in lower access-time failure probability and lower access-V_{min} . ST-2 bit cell gives higher read current compared with the ST-1 bit cell. However, ST-1 bit cell shows

better access-time failure probability due to lower bit line capacitance compared with the ST-2 bit cell case. The delay from RWL turn-ON to global bit line (GBL) evaluation is termed as the access-time.

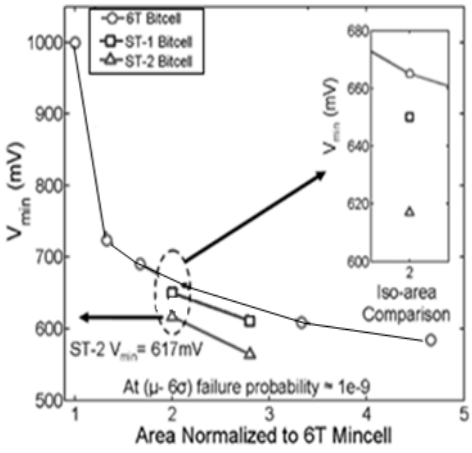


Fig. 11. Iso-area V_{min} comparison of 6T/ST bit cells.

Iso-Area V_{min} Comparison

As seen in Fig. 11, the ST-2 bit cell shows the lowest V_{min} of 617 mV. Built-in feedback mechanism in ST-2 bit cell improves the read-stability ST-2 bit cell improves the write-ability. For this technology, 6T min cell transistor widths need to be upsized by 8* (bit cell area increased by 3.3*) to achieve V_{min} same as the ST-2 bit cell. Note that the upsized ST bit cells show further V_{min} reduction. In this bit cell V_{min} analysis, we do not account the effect of various read/write assist techniques [5]. We believe that these techniques can be applied to the bit cell topologies for further V_{min} reduction

5.RESULTS

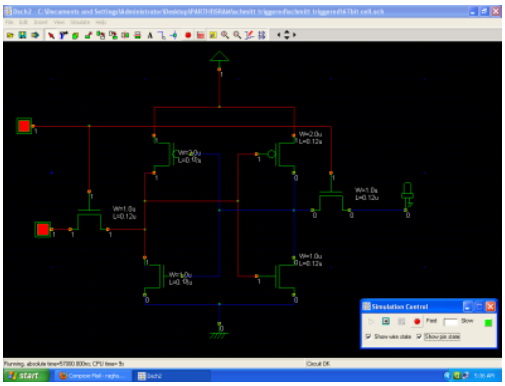


Fig.12. design of 6T SRAM Bit Cell

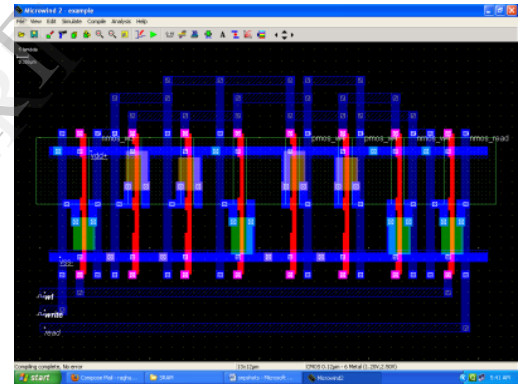


Fig.13.Layout of 6T SRAM Bit Cell

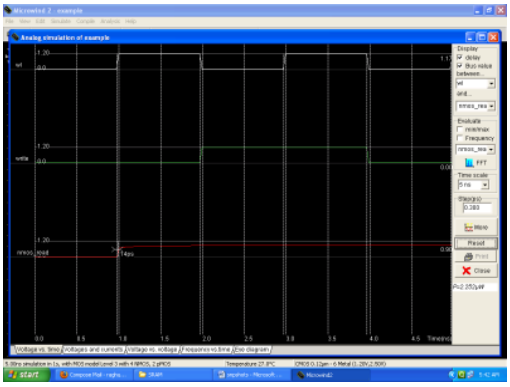


Fig.14. Simulation Results of 6T SRAM Bit Cell

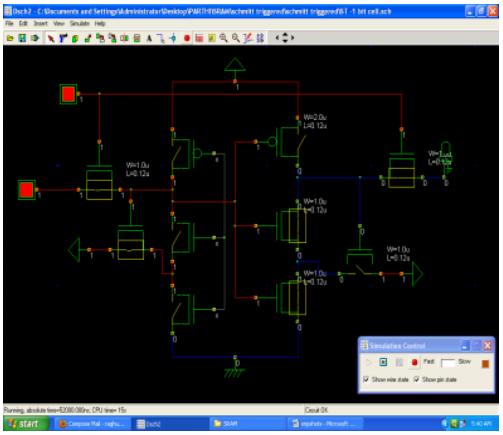


Fig.15.Design of Schmitt Trigger 1(ST 1) Bit Cell

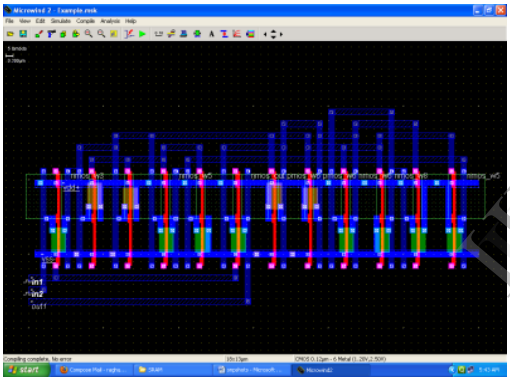


Fig.16.Layout of Schmitt Trigger 1(ST 1) Bit Cell

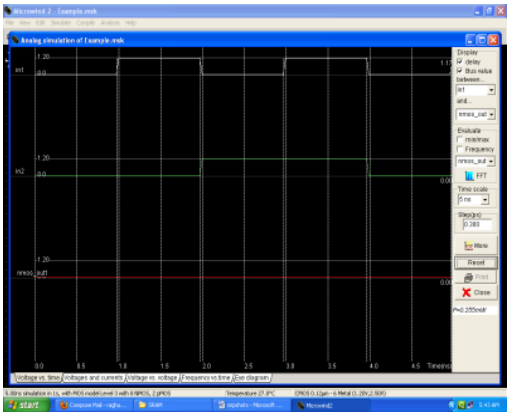


Fig.17.Simlation Result of Schmitt Trigger 1(ST 1) Bit Cell

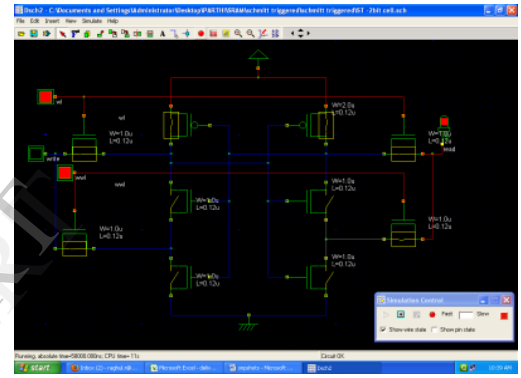


Fig.18.Design of Schmitt Trigger 2(ST 2) Bit Cell

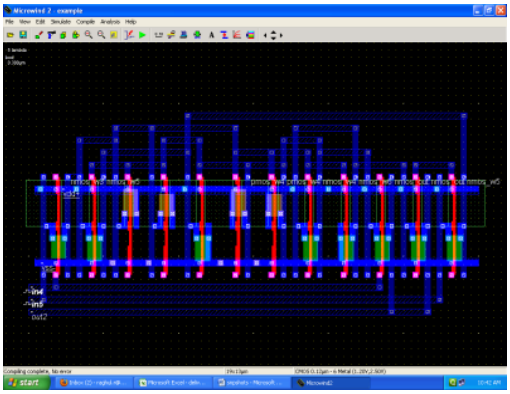


Fig.19.Layout of Schmitt Trigger 2(ST 2) Bit Cell

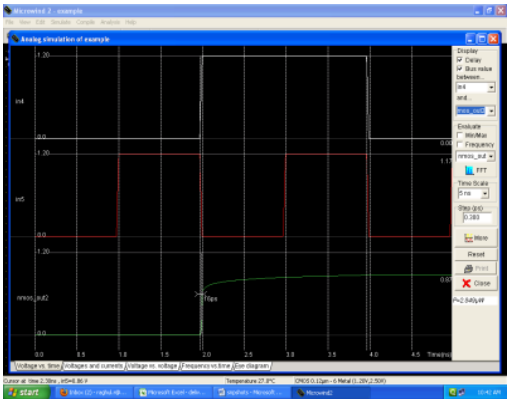


Fig.20.Simulation Result of Schmitt Trigger 2(ST 2) Bit Cell

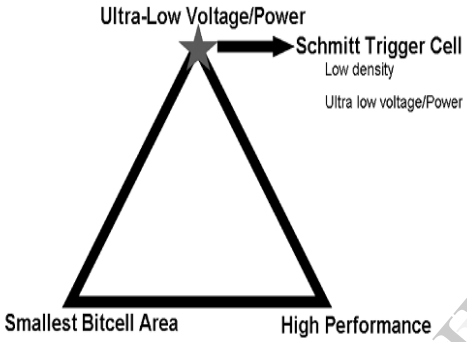


Fig. 21. ST SRAM bit cells: application space

Fig. 21 shows the possible application space for the proposed ST-2 bit cell. Since the ST bit cells consume 2*larger area compared with the 6T min cell, at iso area, the up-sized 6T bit cell has better performance compared with the ST bit cells. However, due to built-in process tolerance the proposed ST

	AREA	POWER
6T SRAM Bit cell	13X12µm	2.252µW
ST-1 bitcell	18X13µm	0.255mW
ST-2 bitcell	19X13µm	2.849µW

bit cells can potentially be useful in applications requiring ultra low voltage. Recently, Wilk reseal. have proposed the use of ST-1 bit cell for tag-arrays to achieve low voltage cache operation

TABLE I

Area and Power Comparision of 6T and ST Bit Cells

6. CONCLUSION

Lowering the supply of voltage is an effectiveness way to achieve ultra-low-power operation. In this work, we evaluated ST-based SRAM bit cells suitable for ultra-low-voltage applications. The built-in feedback mechanism in the proposed ST bit cell can be effective for process-tolerant, low-voltage SRAM operation in future nano scaled technologies. Monte Carlo simulations in 65-nm technology predict lower for the proposed ST-2 bit cell under the iso area condition. Measurement results with a 130-nm test-chip clearly demonstrate the

effectiveness of the proposed ST-2 bit cell for successful ultralow-voltage operation

A. Future Work

In this paper, 6T/ST SRAM bit cell topologies are analyzed for achieving low voltage operation. ST bit cells offer low voltage operation with 2 area overhead. On the other hand, various read/write assist techniques achieve significant reduction, with lower area overhead. Hence, for a given constraint, optimal combination of the bit cell topology read/write assist technique should be chosen for minimal area/power overhead. Thus, the effectiveness of read/write assist techniques for each of the bit cell topology needs to be investigated for achieving lower .

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