Ultra Low Power High Speed Comparator for Analog to Digital Converters

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Abstract --Dynamic comparators with high speed, low power and low offset voltage are the main prerequisite features of all ADCs. A low power high speed and low offset dynamic comparator is being introduced in this paper. In all ADC converter architecture the basic building block is a latched comparator. The circuits are simulated in Cadence® Virtuoso Analog Design Environment in GPDK 180nm and 45nm technology. A comparison of the previous architecture and proposed comparator is shown in 180nm. The power consumption of the proposed architecture is 56% less than the previous architecture. The Circuit reduces the amount of kickback noise and the offset voltage making it favourable for the pipeline data conversion and flash applications.

Keyword - Comparator, low power, low offset, Kickback Noise.

I. INTRODUCTION

In today's world due to increase in demand for the portable battery powered devices, the necessity arises for dynamic latched comparators with high speed, low power consumption and full swing output. These comparators can become a part of high speed ADCs, sense amplifiers used in SRAM read/write circuitry and data receivers. The power in a circuit can be reduced by scaling down the feature sizes. Consequently the process variation and all other non-idealities become more significant as we move toward smaller feature sizes. The term accuracy for the Comparators is tightly constrained with its offset voltage. The power consumption is of keen interest in achieving overall higher performance in ADCs. The main drawback of pre-amp based static comparators is its high power consumption. To minimize this problem dynamic comparators are often used that makes a comparison once in every clock period and requires much lesser power.

The dynamic comparators are of three types namely Resistor divider [2], Differential pair and capacitive-differential pair dynamic comparator.

From these three basic architectures other structures are derived [3],[4]. We choose differential dynamic comparator for a thorough analysis in this paper [1]. We propose new differential dynamic comparator architecture comprised of two stages namely preamplifier stage and a cross coupled latch stage.

This paper is organized as follows: in section II analysis of convenitions dynamic comparator, section III presents the proposed comparator architecture, section IV gives the analysis of proposed design, section V shows simulation results and section VI concludes this paper.

II. DYNAMIC COMPARATOR DESIGN

A. Differential pair comparator

Fig.1 shows a pre-amplifier based dynamic comparator circuit [1]. It consists of pre-amplifier stage and a cross coupled latch circuit.

The latch circuit only triggers when the preamplifier induces a sufficiently large differential voltage at the internal node of the latch. The offset due to the mismatch of cross coupled latch kicks in as soon as the amplifier begins to operate [8]. The trip point of the latch can be adjusted by sizing the input transistors [5], [6]. This dynamic comparator suffers from large kickback noise and moreover it generates a mismatch as soon as it's connected to other circuit as an input source which leads to improper operation of the Latch circuit.

III. PROPOSED COMPARATOR

A. Circuit architecture

Fig.2 shows the proposed comparator architecture. It consists of two stages. The first stage is comprised of a preamplifier stage and the second stage is a latch stage. The first two stages are fed with clock Clk1 and Clk2. The mismatch effect inside the latch circuit is being overcome by separating the input transistors [1]. At the first phase both Clk1 and Clk2 are high which discharges the output node to the ground. During the second phase the Clk1 goes low which turns on the transistor M7 and M9 and the current starts to flow and charges up the node capacitor till Clk2 goes low. As soon as Clk2 goes low transistor M12...
and M_{1,2} goes off which cuts the path from the input to the
cross coupled latch. This separation helps to fight back the
kickback noise which is generated at the latch during
decision phase. The voltage difference between the input
branches and the reference differential voltage gives rise to
the current $I_{in^+}$ and $I_{in^-}$. This process takes place during the
amplification phase. During the third phase the

![Fig 2: schematic of the Proposed Comparator](image)

Differential voltage is boosted in the regenerative loop of
the cross coupled inverter.

B. Time variant modelling of transistor

During the power analysis of a dynamic comparator, the
time variant model is used which emulates the operation of
the transistor during dynamic operation. Existing model of
MOSFET based on the separate expression for each
operating region often suffers from inaccuracies near the
boundaries between such regions. A single expression for
drain current present in [7] is valid for all region of
operation. The expression is given as follows

$$i_d = \frac{i_z}{\phi t} \ln \left[ 1 + e^{V_p - V_{ds}/\phi t} \right] - \ln \left[ 1 + e^{V_p - V_{gd}/\phi t} \right]$$

$\phi$ is the thermal voltage and $V_p$ is the pinch off voltage.
This model shows a good accuracy for low voltage
operation in all regions.

IV. ANALYSIS

A. Decision point

A comparator compares the input differential voltage
with reference differential voltage $V_{in\,diff}$. The output nodes
$V_{out^+}$ and $V_{out^-}$ are discharged to the ground at the
beginning. The amplification starts as soon as the clock
Clk1 goes low and Clk2 still remains high. The current
charges the output capacitor $C_l$ so the output rises linearly
over time. The transistors $M_7$ and $M_8$ operate in linear
region which acts as a resistor to the input transistor $M_5$
and $M_6$. At the beginning of the third phase the initial voltage
at the output nodes are $V_{out^+} = I_{in^+}t_{amp}/C_l$, $V_{out^-} = I_{in^-}t_{amp}/C_l$.
Once the comparator enters into the third phase the sign of
the Vout+ and Vout- determines which way the comparator
swings. The input currents are controlled by $V_{in^+}-V_{ref^+}$
and $V_{in^-}-V_{ref^-}$. Power is drawn only when the circuit is latched.
The body terminals are shorted to their immediate sources
to avoid body effect.

B. Sensitivity analysis

The offset of a comparator depends on different
variables for that sensitivity analysis is required. The main
variables for a comparator are transistor’s length, width,
threshold voltage, carrier mobility, input and reference
voltage clock signal and different parasitic capacitances.
Robustness is defined by the small sensitivity to these
variables. The comparator offset will be zero if the
comparator is symmetric with respect to all idealities.
Sensitivity of the comparator is defined as $S_{V_{out}} = V_{os}/\Delta X$
[4]; where $\Delta X$ is the amount of imbalance in the variable
and where $V_{os}$ is the offset voltage.

C. Kickback noise

The output voltage variation in CMOS latched
comparators can spoil the input voltage as it is coupled to
the input transistor in the circuit shown in Fig 1. The use of
transistors $M_3$ and $M_4$ in the proposed circuit helps in the
reduction of the kickback noise to further extent [9].

D. Delay

The delay shown in Fig. 4 can be defined as the time
difference between the start of the amplification phase and
the time where 50% of the final output of the latch is
reached. The capacitance value used in this architecture is
less than 1fF.

E. Power analysis

During one period of comparison the average
power of the supply voltage is obtained from the equation

$$P_{power} = \frac{1}{T} \int_{0}^{T} V_{dd} I_{supply} \, dt$$

where $I_{supply}$ is the current drawn from the supply voltage ($V_{dd}$)
and $f_{clk}$ is the comparator clock frequency. During the
decision making phase when Clk2=V_{dd}, at first both the
transistor $M_{10}$ & $M_{11}$ both are on. As time passes, when one
of the outputs is charged enough to turn on one of NMOS transistor ($M_{12}/M_{13}$) regeneration will commence. Assuming that the case where $V_{in+}<V_{in-}$, Out, charges and eventually turns on $M_{11}$ which in turn charges node $V_{out-}$ to $V_{dd}$ during evaluation phase. A current is drawn from $V_{dd}$ from one of PMOS transistor during a short time in the dynamic operation of the decision making phase. The difference voltage in latch output($V_{out+}-V_{out-}$) changes in logarithmic manner as follows $\Delta V_{out}=\Delta V_0 \exp\left(\frac{G_m}{C_{load}}\right)$ where in this equation, $G_m$ is the effective transconductance of the PMOS and NMOS transistors of the back to back latch inverters , $C_{load}$ is the load capacitance at the comparators output and $\Delta V_0$ is the initial voltage difference [8].The most influential design parameters on power consumption of the comparators are based upon the clock frequency, size of the input transistor , supply voltage and the time during which comparison is made that is the time when the peak supply current is drawn. For instance there is a trade-off in the latch inverters while deciding the sizes of PMOS transistors. Parasitic capacitances increase leads to higher power dissipation if bigger transistors are used.

V. SIMULATION RESULT AND COMPARISON

The layout of the proposed comparator in 180nm technology is shown in Fig.6. The whole comparator takes an area of $185.26\mu m^2$. The proposed structure in Fig. 2 is designed in Cadence 0.18u process. In table 1 key value that are being used are shown. The amplification time for the proposed comparator was set to 100ps.The proposed comparator successfully detects a difference of 1mv.

The proposed comparator is simulated in 180nm and 45nm CMOS technologies. The power consumption of the pre-layout and post layout simulation in 180nm are shown in table 3.Comparison of the previous architecture with the proposed architecture is shown in Table 2.
From Table 4 it can be concluded that the comparator can work at a minimum supply voltage of 1.2v at 180nm process. Table 5 shows the variation of the power depending upon the input signal frequency. Fig. 9 shows the graph between power dissipation and the load capacitance from which it can be concluded that with the increase of the load capacitances the power dissipation increases and also at the same time the delay is increased. Table 5.a and 5.d gives the power dissipation verses input frequency in two different technologies.

<table>
<thead>
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<th>Input frequency</th>
<th>Power dissipation</th>
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<tr>
<td>20M HZ</td>
<td>32.06uW</td>
</tr>
<tr>
<td>40M HZ</td>
<td>32.14uW</td>
</tr>
<tr>
<td>60M HZ</td>
<td>32.08uW</td>
</tr>
<tr>
<td>80M HZ</td>
<td>32.07uW</td>
</tr>
<tr>
<td>100M HZ</td>
<td>32.28uW</td>
</tr>
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</table>

A new dynamic comparator with low power, high speed and low offset voltage has been proposed. The power dissipation of the comparator was calculated varying the supply voltage and the input frequency. The proposed comparator was simulated in 180nm and 45nm CMOS process and their results are shown in various table. The power consumption of the proposed comparator was 56% less than the previous architecture and the speed has been increased with further reduction of kickback noise and offset voltage. A post amplifier can be connected at the output when a full swing is required.

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REFERENCES


