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Ultra Low Power High Speed Comparator for Analog to Digital Converters

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***Abstract* --Dynamic comparators with high speed , low power and low offset voltage are the main prerequisite features of all ADCs .A low power high speed and low offset dynamic comparator is being introduced in this paper. In all ADC converter architecture the basic building block is a latched comparator. The circuits are simulated in Cadence® Virtuoso Analog Design Environment in GPDK 180nm and 45nm technology. A comparison of the previous architecture and proposed comparator is shown in 180nm. The power consumption of the proposed architecture is 56% lesser than the previous architecture. The Circuit reduces the amount of kickback noise and the offset voltage making it favourable for the pipeline data conversion and flash applications.**

Keyword - Comparator, low power, low offset, Kickback Noise.

I. INTRODUCTION

In today's world due to increase in demand for the portable battery powered devices, the necessity arises for dynamic latched comparators with high speed, low power consumption and full swing output. These comparators can become a part of high speed ADCs, sense amplifiers used in SRAM read/write circuitry and data receivers. The power in a circuit can be reduced by scaling down the feature sizes. Consequently the process variation and all other non-idealities become more significant as we move toward smaller feature sizes. The term accuracy for the Comparators is tightly constrained with its offset voltage. The power consumption is of keen interest in achieving overall higher performance in ADCs. The main drawback of pre-amp based static comparators is its high power consumption. To minimize this problem dynamic comparators are often used that makes a comparison once in every clock period and requires much lesser power.

The dynamic comparators are of three types namely Resistor divider [2], Differential pair and capacitive-differential pair dynamic comparator.

From these three basic architectures other structures are derived [3],[4].
We choose differential dynamic comparator for a thorough analysis in this paper [1]. We propose new differential dynamic comparator architecture comprised of two stages namely preamplifier stage and a cross coupled latch stage.

This paper is organized as follows: in section **II** analysis of conventions dynamic comparator, section **III** presents the proposed comparator architecture, section **IV** gives the analysis of proposed design, section **V** shows simulation results and section **VI** concludes this paper.

II. DYNAMIC COMPARATOR DESIGN

A. *Differential pair comparator*

Fig.1 shows a pre-amplifier based dynamic comparator circuit [1]. It consists of pre-amplifier stage and a cross coupled latch circuit.

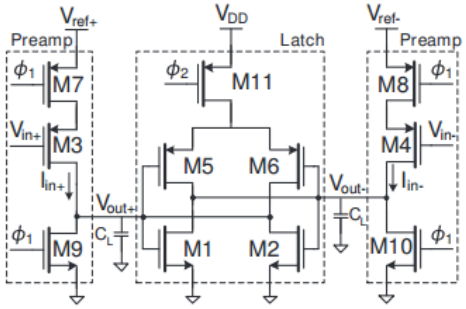

Fig 1. Differential dynamic comparator

The latch circuit only triggers when the preamplifier induces a sufficiently large differential voltage at the internal node of the latch. The offset due to the mismatch of cross coupled latch kicks in as soon as the amplifier begins to operate [8]. The trip point of the latch can be adjusted by sizing the input transistors [5], [6]. This dynamic comparator suffers from large kickback noise and moreover it generates a mismatch as soon as it's connected to other circuit as an input source which leads to improper operation of the Latch circuit.

III. PROPOSED COMPARATOR

A. *Circuit architecture*

Fig.2 shows the proposed comparator architecture. It consists of two stages. The first stage is comprised of a preamplifier stage and the second stage is a latch stage. The first two stages are fed with clock Clk1 and Clk2. The mismatch effect inside the latch circuit is being overcome by separating the input transistors [1]. At the first phase both Clk1 and Clk2 are high which discharges the output node to the ground. During the second phase the Clk1 goes low which turns on the transistor M_7 and M_8 and the current starts to flow and charges up the node capacitor till Clk2 goes low. As soon as Clk2 goes low transistor M_{12}

and M_{13} goes off which cuts the path from the input to the cross coupled latch. This separation helps to fight back the kickback noise which is generated at the latch during decision phase. The voltage difference between the input branches and the reference differential voltage gives rise to the current I_{in+} and I_{in-} . This process takes place during the amplification phase. During the third phase the

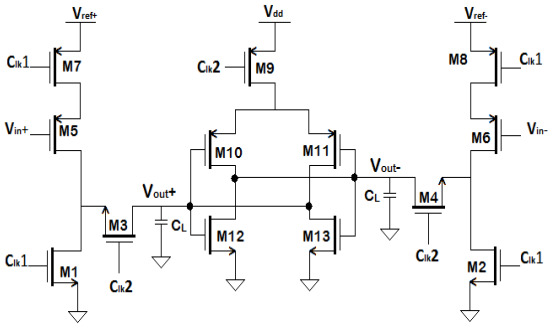

Fig 2:-schematic of the Proposed Comparator

Differential voltage is boosted in the regenerative loop of the cross coupled inverter.

B. *Time variant modelling of transistor*

During the power analysis of a dynamic comparator, the time variant model is used which emulates the operation of the transistor during dynamic operation. Existing model of MOSFET based on the separate expression for each operating region often suffers from inaccuracies near the boundaries between such regions. A single expression for drain current present in [7] is valid for all region of operation. The expression is given as follows

$i_{d=}i_z[\ln^2(1+e^{Vp-Vsb/2\phi t}) - \ln^2((1+e^{Vp-Vdb/2\phi t})]$

ϕ_t is the thermal voltage and V_p is the pinch off voltage. This model shows a good accuracy for low voltage operation in all regions.

IV. ANALYSIS

A. *Decision point*

A comparator compares the input differential voltage with reference differential voltage $V_{refdiff}$. The output nodes V_{out+} and V_{out-} are discharged to the ground at the beginning. The amplification starts as soon as the clock Clk1 goes low and Clk2 still remains high. The current charges the output capacitor C_L so the output rises linearly over time. The transistors M_7 and M_8 operate in linear region which acts as a resistor to the input transistor M_5 and M_6. At the beginning of the third phase the initial voltage at the output nodes are $V_{out+} = I_{in+}t_{amp}/c_L$, $V_{out-}=I_{in}-t_{amp}/c_L$. Once the comparator enters into the third phase the sign of the Vout+ and Vout- determines which way the comparator swings. The input currents are controlled by V_{in+}-V_{ref+} and Vin-V_{ref-} . Power is drawn only when the circuit is latched. The body terminals are shorted to their immediate sources to avoid body effect.

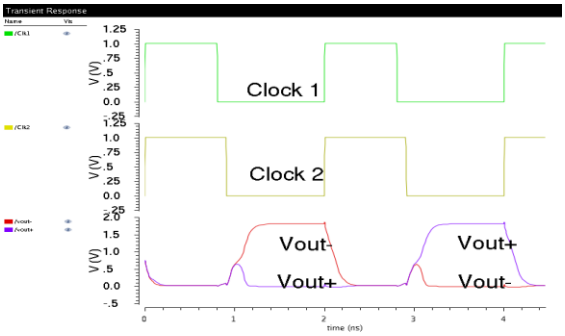

Fig. 3. Output waveform showing the swing of the proposed comparator

B. *Sensitivity analysis*

The offset of a comparator depends on different variables for that sensitivity analysis is required. The main variables for a comparator are transistor's length, width, threshold voltage, carrier mobility, input and reference voltage clock signal and different parasitic capacitances. Robustness is defined by the small sensitivity to these variables. The comparator offset will be zero if the comparator is symmetric with respect to all idealities.

Sensitivity of the comparator is defined as $S_x^{Vox}=V_{os}/\Delta X$ [4]; where ΔX is the amount of imbalance in the variable and where V_{os} is the offset voltage.

C. *Kickback noise*

The output voltage variation in CMOS latched comparators can spoil the input voltage as it is coupled to the input transistor in the circuit shown in Fig 1.The use of transistors M_3 and M_4 in the proposed circuit helps in the reduction of the kickback noise to further extent [9].

D. *Delay*

The delay shown in Fig. 4 can be defined as the time difference between the start of the amplification phase and the time where 50% of the final output of the latch is reached. The capacitance value used in this architecture is less than 1fF.

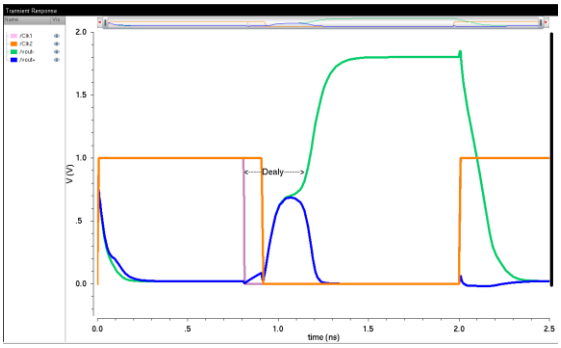

Fig. 4 delay of the comparator

E. *Power analysis*

During one period of comparison the average power of the supply voltage is obtained from the equation

$Power_{avg}=1/T\int_0^T Vdd.Isupply.dt=f_{clk.}V_{dd}\int_0^T Isupply.dt$ where I_{supply} is the current drawn from the supply voltage (V_{dd}) and f_{clk} is the comparator clock frequency. During the decision making phase when Clk2=V_{dd}, at first both the transistor M_{10} & M_{11} both are on. As time passes, when one

of the outputs is charged enough to turn on one of NMOS transistor (M_{12}/M_{13}) regeneration will commence. Assuming that the case where $V_{in+}<V_{in-}$, Out_+ charges and eventually turns on M_{11} which in turn charges node V_{out-} to V_{dd} during evaluation phase. A current is drawn from V_{dd} from one of PMOS transistor during a short time in the dynamic operation of the decision making phase. The difference voltage in latch output(V_{out+}-V_{out-}) changes in logarithmic manner as follows $\Delta V_{out}=V_{out+}-V_{out-}=\Delta V_o exp(G_m t/C_{load})$ where in this equation, G_m is the effective transconductance of the PMOS and NMOS transistors of the back to back latch inverters , C_{load} is the load capacitance at the comparators output and ΔV_o is the initial voltage difference [8].The most influential design parameters on power consumption of the comparators are based upon the clock frequency, size of the input transistor , supply voltage and the time during which comparison is made that is the time when the peak supply current is drawn. For instance there is a trade-off in the latch inverters while deciding the sizes of PMOS transistors. Parasitic capacitances increase leads to higher power dissipation if bigger transistors are used.

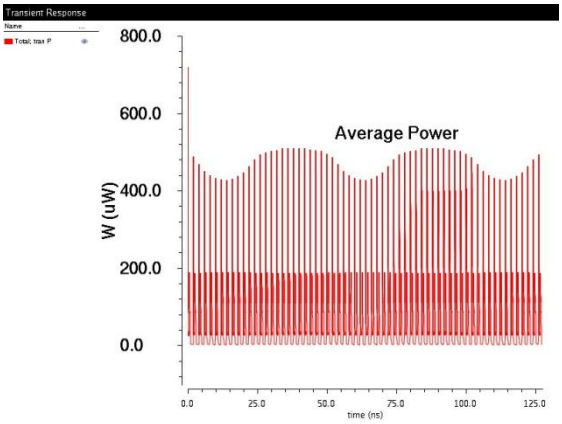

Fig.5 average power consumption of Proposed comparator

V. SIMULATION RESULT AND COMPARISON

The layout of the proposed comparator in 180nm technology is shown in Fig.6. The whole comparator takes an area of 185.26um^2. The proposed structure in Fig. 2 is designed in Cadence 0.18u process. In table 1 key value that are being used are shown. The amplification time for the proposed comparator was set to 100ps.The proposed comparator successfully detects a difference of 1mv.

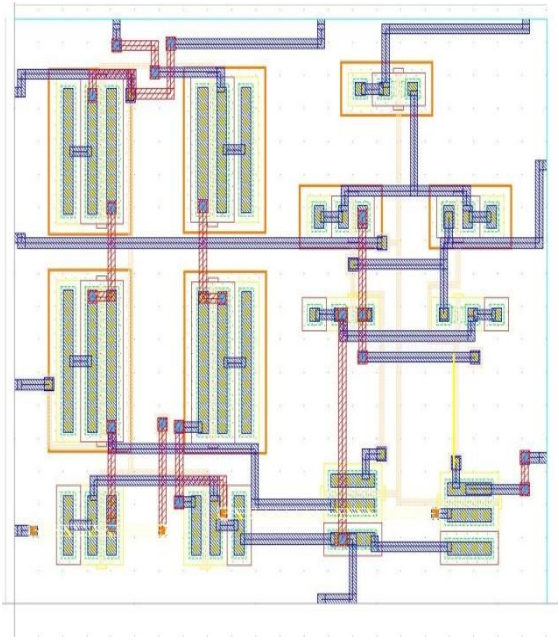

Fig.6 layout of the proposed comparator in 180nm.

Table 1. Key Values Used For Simulation At Same Clock Frequency

Technology	**180nm**	**45nm**
Power supply	1.8v	1v
MOSFET size	M7=M8=200/9 M5=M6=225/9 M3=M4=100/9 M1=M2=100/9 M10=M11=44/9 M12=M13=22/9	M7=M8=140/3 M5=M6=40/3 M3=M4=20/3 M1=M2=8/3 M12=M13=8/3
Clock Frequency	20G Hz	20G Hz
Input signal frequency	20M Hz	20M Hz

The proposed comparator is simulated in 180nm and 45nm CMOS technologies. The power consumption of the pre-layout and post layout simulation in 180nm are shown in table 3.Comparison of the previous architecture with the proposed architecture is shown in Table 2.

Table 2.

Comparators	Offset Voltage(Vos)	Power	Delay
Previous architecture[1]	39mv	72.95uw	168.04ps
Proposed architecture	20.98mv	32.06uw	160.81ps

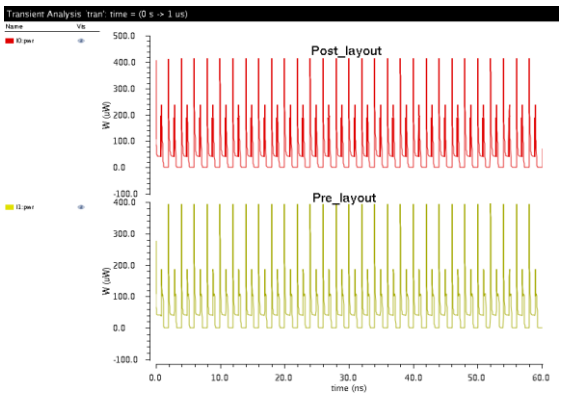

Fig. 7 showing the power graph of pre-layout and post layout simulation.

Table 3.

Pre-layout	average power=32.06uw	delay=160.81ps
Post-layout	average power=50.01uw	delay=197.18ps

The power consumption of the three sources V_{dd} , V_{ref+} and V_{ref-} are considered as power consumption in the proposed architecture. The offset voltage calculated in this architecture is around 20.98mv.The output waveform of the proposed comparator are shown in Fig. 8.

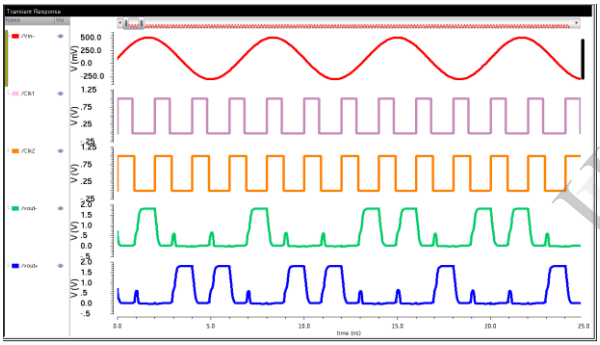

Fig. 8 output waveform of the proposed comparator.

Table 4.

Technology 180nm		
Supply Voltage	Power Dissipation	Delay
1.8v	32.06uw	160.81ps
1.6v	23.92uw	182.65ps
1.4v	18.97uw	218.38ps
1.2v	15.63uw	288.30ps
Technology 45nm		
Supply Voltage	Power Dissipation	Delay
1v	1.023uw	72.08ps
0.9v	0.796uw	406.5ps
0.8v	0.644uw	405.35ps
0.7v	0.508uw	265.80ps

From Table 4 it can be concluded that the comparator can work at a minimum supply voltage of 1.2v at 180nm process. Table 5 shows the variation of the power depending upon the input signal frequency. Fig. 9 shows the graph between power dissipation and the load capacitance from which it can be concluded that with the increase of the load capacitances the power dissipation increases and also at the same time the delay is increased. Table 5.a and 5.d gives the power dissipation verses input frequency in two different technologies.

Table 5.

180nm technology	
Input frequency	Power dissipation
20M HZ	32.06uW
40M HZ	32.14uW
60M HZ	32.08uW
80M HZ	32.07uW
100M HZ	32.28uW
45nm technology	
Input frequency	Power dissipation
5M HZ	1.031uW
10M HZ	1.024uW
50M HZ	1.009uW
100M HZ	0.995uW
150M HZ	0.985uW

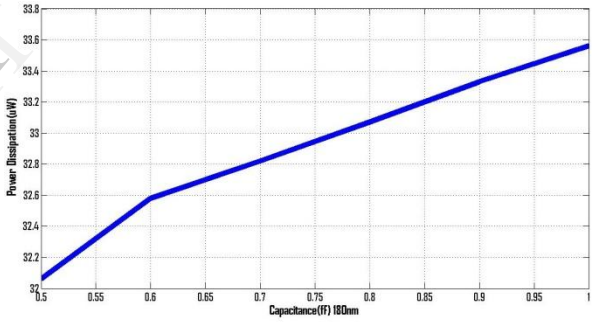

Fig. 9 Power dissipation vs capacitance curve in 180nm

VI. CONCLUSION

A new dynamic comparator with low power, high speed and low offset voltage has been proposed. The power dissipation of the comparator was calculated varying the supply voltage and the input frequency. The proposed comparator was simulated in 180nm and 45nm CMOS process and their results are shown in various table. The power consumption of the proposed comparator was 56% less than the previous architecture and the speed has been increased with further reduction of kickback noise and offset voltage. A post amplifier can be connected at the output when a full swing is required.

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REFERENCES

1. A low-power low-offset dynamic comparator for analog to digital converters Mohsen Hassanpourghadin , Milad Zamani, Mohammad Sharifkhani Department of Electrical Engineering, Sharif University of Technology, Tehran, Iran/Microelectronics Journal 45 (2014),pp. 256–262.
2. T. Cho, P. Gray, A 10 b, 20 msample/s, 35 mw pipeline a/d converter, IEEE J. Solid-State Circuits 30(3)(1995),pp.166-172
3. J. Yang, X. Cheng, Y. Guo, Z. Zhang, X. Zeng, A novel low-offset dynamic comparator for high-speed low-voltage pipeline adc, in: 2010 10th IEEE International Conference on Solid-State and Integrated Circuit Technology.
4. (ICSICT),2010,pp.548–550.
5. V. Katyal, R.L. Geiger, D.J. Chen, A new high precision low offset dynamic comparator for high resolution high speed adcs, in: IEEE Asia Pacific Conference on Circuits and Systems, 2006, APCCAS 2006, 2006, pp. 5–8.
6. L. Sumanen, M. Waltari, K. Halonen, "A Mismatch Insensitive CMOS Dynamic Comparator for Pipeline A/D Converters," IEEE ICECS, vol.1, pp. 32-35, Dec. 2000.
7. L. Sumanen, M. Waltari, V. Hakkarainen, K. Halonen, "CMOS Dynamic Comparators for Pipeline A/D Converters," IEEE ISCAS, vol.5, pp.157-160, May 2002.
8. Y. Tsividis, K.Suyama and K.vavelidis, “Simple reconciliation MOSFET model valid in all regions,” IEE Electronic. Lett. vol. 31 no. 6 pp. 506-508, March 1995.
9. J. He, S. Zhan, D. Chen, R. Geiger, Analyses of static and dynamic random offset voltages in dynamic comparators, IEEE Trans. Circuits Syst. I: Reg. Pap. 56 (5),pp-(2009)911-919,
10. P. Figueiredo, J. Vital, Kickback noise reduction techniques for cmos latched comparators, IEEE Trans. Circuits Syst. II: Express Briefs 53 (7) (2006) 541–545.
11. A. Nikoozadeh, B. Murmann, An analysis of latch comparator offset due to load capacitor mismatch, IEEE Trans. Circuits Syst. II: Express Briefs 53 (12) (2006),pp-1398-1402.