

Turbo Decoder for Wireless Communication System through VLSI Design

Konika Bhowmik

M.Tech (Vlsi) Student

Department of Electronics & Communication Engineering

Dr. C.V. Raman University Kota, Bilaspur

C.G., India

Ravish Gupta

Assistant Professor

Department Of Electronics & Communication Engineering

Dr. C.V. Raman University Kota, Bilaspur

C.G., India

Abstract— There is no indication of an interruption in the development of the wireless communication system, which requires ever-increasing data transfer rates. The demand for ever-increasing data rates from more and more mobile users has grown exponentially. To meet these data rate requirements, the wireless industry has already specified an increase in data rates up to the 3 Gbps level for next generation wireless communication systems. Thus, each of the communication blocks involved in a physical layer of a wireless communication system must support such higher data rates. Turbo codes are widely used in wireless communication systems to provide reliable information transfer and provide near-optimal error rate performance. However, the inherent iterative decoding process limits the decoder turbo to a higher data rate or higher rate. In this work the improvement of the flow and the energetic efficiency of a turbo-decoder is investigated, using the optimization on the architectural and algorithmic level.

A new ungrouped MAP decoding technique has resulted in a deep channel MAP decoder. We have also proposed an add-compare-select (ACS) architecture, which includes a standardization method for the status metric and has the shortest delay for the critical path. With these high speed MAP decoders, a fast and energy efficient parallel turbo decoder is developed that is compatible with 3GPP LTE and LTE-A for wireless communication. It was synthesized and simulated after layout in CMOS technology finally; the proposed turbo decoder design is implemented on FPGA and tested in a communications.

Keywords— Data Rate, wireless system, optimum error rate, MAP Decoder, LTE, GBPS, CMOS technology.

INTRODUCTION

1.1 Background

Evolution of such wireless connections Communication technologies from the second generation (2G) to the third generation (3G) has seen an increase in the speed of data transfer and predicted more than 3 Gbps for the next generation wireless communication standards. To, to Each communication block is associated with the physical layer of the wireless communication The system must process data at this speed.

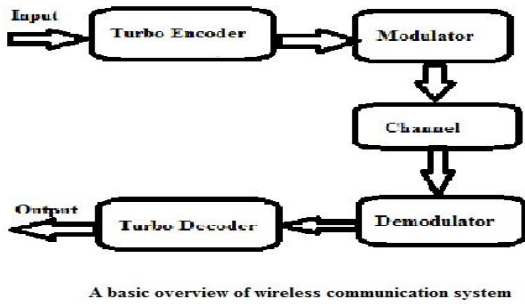
Wireless communication has always been in the field of communication The huge area, because it often faces great challenges. For example, how to recover data at high speed Transmission through wireless networks, delivery of audio and high definition video, Voice quality and the expansion of broadband data services. The channel decoder is an integral part of the wireless communication system and responds to it saber for reliable data communication.

A channel decoder for which turbo codes are used Error correction offers excellent bit error rate performance and has created this code Generally accepted by different wireless communication standards 3G data peak rates and the 4G wireless communication standards that include turbo codes for error correction are 3GPP-LTE (third generation partners).ship project - long-term evolution) the wireless standard has the highest peak data rate between 3G standards In a similar way to the ITUR specification (international telecommunication).

Communications Sector of the Communications Union) for 4G, 3GPP LTE-Advanced technology Supports a maximum data rate of 1 Gbps On the other hand, it is the inherent iteration the decoding process limits the turbo decoder to process data with a higher data rate. brilliant Much work is being done on the design of faster turbo transmitters or data through put implementations have achieved revenues of up to 2.2 Gbps However, the wireless industry has already focused on milestone performance of more than 3 Gbps the next generation of wireless communication standards. That is why our research goal It is based on the design of the turbo efficient decoder that can withstand such high performance for future wireless communication systems.

1.2 System Overview

The latest developments in DCS design are based on software algorithms instead of dedicated hardware. In a typical communication system, all processing is done in the digital domain. The digital transmission with analog transmission is not available for data processing and is not available. The main features of DCS provide a waveform of a set of possible finite waves over a fixed period of time, but waves can take any shape for an analog communication system. The purpose of the receiver is to define a waveguide waveform.



Here the diagram shows the upper block at the end of the tip end of the receiver, a signal transmitter in the courtyard. an analog system in the source data and the data processing system, an analog signal source compatibility between courses. It is difficult to get rid of the source data compression coding. Do not, however, it is entirely false, not upon any new users of encryption the secret of her message. Detection and correction of errors in the channel programming data bits are added to the case. The faith on the information taking into account increase the complexity of the decoder . There are many different approaches to the wide variety of sources; it is given to the source of the communication of the signals that they are fully to mix.

Carrier wave in that system that signal distorted for frequent shrill sound it produces. Very often, the pulse modulation block is typically included filtering to minimize the transmission bandwidth. Standards turned into binary code, and pulse modulation (PCM). The next step of great importance to give an address of Marcus applications for which is he that betrayed baseband modulation waveform frequency from the band pass of the thick, go to the toilet only on the upper is primarily associated with. He will take the signal processing steps, which are reversed transmitter to the receiver.

2. PROPOSE DESIGN

Basic transmitter and receiver schematic representations of the wireless communication device that's used for 3GPP-LTE/LTE-Advanced standards are shown in Fig.2. Practical blocks are divided as digital baseband module, analog-RF module and MIMO (multiple inputs multiple outputs) antennas. In digital baseband module of the transmitter, sequence of data bits United Kingdom eight $k = f1, 2, 3 \dots ng$ are processed by numerous sub-modules and are fed to the channel encoder. For each data bit of sequence Uk , a systematic bit xsk as well as parity bits.

$xp1k$ and $xp2k$ are generated by channel encoder using convolutional encoders (CEs) and QPP inter leaver (i). These Encoded bits are more processed by remaining sub modules; finally, the output- digital information from baseband are regenerate into quadrature and in-phase analog signals by DAC. Analog signals fed to multiple analog RF modules are up-converted to an RF frequency, amplified, band passed and transmitted via MIMO antennas, that transform RF signals into electromagnetic waves for transmission through wireless channel.

At the receiver, RF-signals provided by multiple antennas to analog-RF modules are band-pass filtered for extraction of desired band of signals. Then, they're low noise amplified and down converted into baseband signals. Later on, these signals are sampled by ADC of the digital baseband module where numerous sub modules process such samples and are fed to soft demodulator. It generates a-priori LLR values sk , $p1k$ and $p2k$ for the transmitted systematic and parity bits, respectively, and are fed to turbo decoder via serial-parallel convertor

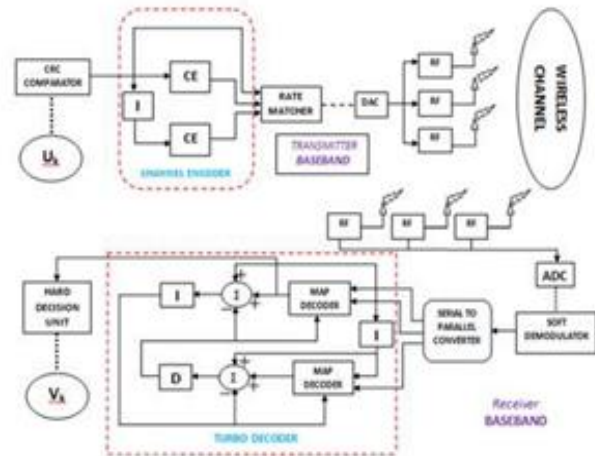


Fig : Basic block diagram of transmitter and receiver used for wirelessnetwork

3.1 TURBO CODE

The generic form of a turbo encoder consists of two encoders separated by the interleaved. The two encoders used are normally identical and the code is systematic, i.e., the output contains the input bits as well. Turbo codes are linear codes. Linear codes are codes for which the module sum of two valid code words is also a valid code word. A "good" linear code is one that has mostly high-weight code words. The weight or Hamming weight of a code word is the number of ones that it contains, e.g., the Hamming weight of code word '000' and '101' is 0 and 2 respectively. High-weight code words are desirable because it means that they are more distinct, and (thus the decoder will have an easier time distinguishing among them. While a few low-weight code words can be tolerated, the relative frequency of their occurrence should be minimized.

The choice of the interleaved is crucial in the code design. Interleave is used to scramble bits before being input to the second encoder. This makes the output of one encoder different from the other encoder. Thus, even if one of the encoders occasionally produces a low-weight, the probability of both the encoders producing a low-weight output is extremely small. This improvement is known as interleave gain. Another purpose of interleaving is to make the outputs of the two encoders uncorrelated from each other. Thus, the exchange of information between the two decoders while decoding yields more reliability. There are different types of interleaves.

3.2 Algorithm

The two main algorithms in the SISO component decoder, They are MAP decoding and SOVA decoding. The MAP decoding algorithm is a posteriori Opportunities (App). The SOVA decoding algorithm is based on ML probabilities. Both algorithms use an iterative technique to achieve the decoding performance. The MAP algorithm can Exceed SOVA decoding by 0.5 dB or more.

The MAP algorithm checks for many possible paths through Convolutional decoder grid, so it looks too complicated application in most systems. The MAP algorithm is complex because there are a large number of multiplied and exponential indicators. The log file MAP algorithm performs all calculations access. In recently the uses of the Max Log Map algorithm for decoding increase so much. Now the commercial operator the three algorithms MAP, LOG-MAP and MAX-LOG MAP algorithms were compared theoretical and practical and the best algorithm for high Debit is the preferred MAX-LOG MAP algorithm. Four Parameters are set to find the exact a posteriori probability for the received block. These are sectorial indicators, State metric before, metrics and probability of a logo.

3.3 The Wireless System

RF-based OFDM transmission systems both in-phase and quadrature components are transmitted; in optical systems it is not possible to relay phase information. The optical carrier is at THz frequency not allowing the signal demodulation due to technological restrictions. Because of this physical restriction, we had to apply a modification to the frequency spreading block of the overall system. An IFFT process performs the frequency spreading for the OFDM scheme generating I/Q components. The modification at the IFFT process is a generalized modification of the original function:

$$X(n) = X(n) = 1/N \sum_{k=0}^{N-1} X_k e^{j2\pi n k/N}$$

where $X(k)$ represents the amplitude and phase of the different signal components arriving from the BPSK/QPSK mapping block by parallelizing the complex components carried out from the mapping block (e.g., QPSK 16-QAM) we mirror them, introducing DC components for separation, by reversing the complex-conjugated symbols. As a result a stream of real-valued samples is generated, corresponding to an intensity modulation at the optical source allowing the fast and accurate demodulation of the transmitted signal.

$$X(k) = DC, a+bi, c+di, \dots, DC, \dots, c-di, a-bi, \\ Y(k) = A, B, C, \dots, S.$$

The orthogonal frequency division multiplexing is widely used in wireless RF communication systems and our goal is to adapt and investigate the performance of such a modulation scheme to the wireless optical physical layer. An optical test bed has been implemented in order to allow further evaluation of the simulated system in real conditions. For this reason, we have integrated optical components in an optical laboratory bench as an optical interface and furthermore we have

emulated the entire system with a vector signal generator from Agilent technologies.

The wireless optical system is designed to explore, mainly, the physical layer performance of the transmission rather than the actual protocol stack of a network. The evaluated system is presented. For the transmission part, a text file was chosen, broken-up in bits and mapped to subcarrier modulation schemes according to transmission requirements. The subcarriers modulation schemes can be BPSK, QPSK or 16-QAM in every number range from 4 to 512. After the mapping process, the symbols are driven to a serial-to-parallel block and introduced to the IFFT spreading process, The result of this process is amplitude modulation transmission as we are not able to have coherent schemes in wireless optical systems.

All this process is driven by custom software and the samples are downloaded to the Agilent vector signal generator where we can introduce the desired sampling rate and also further amplification if necessary. Once the samples are loaded to the generator, we are choosing the sampling rate, in our case 10MHz. The output of the signal generator is interfaced to a laser driver which biases the 650 nm laser diode. In order to stabilize the laser diode, we have used temperature controllers keeping the temperature at 25 degrees centigrade.

4. CONCLUSION

In this paper, turbo decoder has This paper focuses on the VLSI style side of high-speed MAP decoders that are the intrinsic building- blocks of parallel turbo decoders. For the LBCJR algorithm employed in MAP decoders, we've bestowed an ungrouped backward recursion technique for the computation of backward state metrics. Unlike the conventional decoder architectures, MAP decoder based on this system was extensively pipelined and retimed to attain higher clock frequency. In addition, the state metric normalization technique used within the suggested design of ACSU has achieved a reduced critical path delay.

5. REFERENCES

- [1] Rahul Shrestha and Roy Paily, Comparative Study of Simplified MAP Algorithms and an Implementation of Non-Parallel-Radix-2 Turbo Decoder," *Journal of Signal Processing Systems - Springer*, (DOI: 10.1007/s11265-014-0951-7, In Press - September-2014).
- [2] Rahul Shrestha and Roy Paily, High-Throughput Turbo Decoder with Parallel Architecture for LTE Wireless Communication Standards," *IEEE Transactions on and Systems I: Regular Papers*, Volume: 61, Issue: 9, pp. 2699-2710, September-2013
- [3] Rahul Shrestha and Roy Paily, \Performance and Throughput Analysis of Turbo Decoder for the Physical Layer of Digital Video Broadcasting - *Satellite-services to Handhelds (DVB-SH) Standard*," *Journals of IET Communications*, Volume: 7, Issue: 12, pp. 1211-1220, 2013.
- [4] Rahul Shrestha and Roy Paily, \Design and Implementation of a Linear Feedback Shift Register Interleaver for Turbo Decoding," *Springer Berlin/Heidelberg Lecture Notes in Computer Science*, Volume: 7373, pp. 30-39, 2012.
- [5] Shu Lin and Daniel J. Costello, Error Control Coding: Fundamentals and Applications, Prentice Hall, 1983.

- [6] D. Divsalar and F. Pollara, "Turbo codes for deep-space communications", *JPL TDA Progress Report 42-120*, Feb. 15, 1995
- [7] D. Divsalar and F. Pollara, "Turbo codes for PCS applications", *Proceedings of ICC 1995*, Seattle, Washington, pp. 54-59, June 1995.
- [8] S. Benedetto and G. Montorsi, "Unveiling turbo codes: some results on parallel concatenated coding schemes," *IEEE Transactions on Information Theory*, Vol. 42, No. 2, pp. 409-428, March 1996. J. G. Proakis, "Digital Communications", 3rd ed., New York, McGraw-Hill, 1995.
- [9] L. R. Bahl, J. Cocke, F. Jelinek, and J. Raviv. Optimal decoding of linear codes for minimizing symbol error rate. *IEEE Transactions on Information Theory*, IT-20:284-287, March 1974.
- [10] C. Berrou, P. Adde, E. Angui, and S. Faudeil. A low complexity soft-output viterbi decoder architecture. In *IEEE Proceedings of ICC '93*, pages 737-740, Geneva, May 1993.
- [11] C. Berrou, A. Glavieux, and P. Thitimajshima. Near shannon limit error-correcting coding and decoding: Turbo codes. In *IEEE Proceedings of ICC '93*, pages 1064-1070, May 1993. S. Crozier, Ken Gracie, and Andrew Hunt. Efficient turbo decoding techniques. Technical report, Communications research Centre, 3701 Carling Avenue, P.O. Box 11490, Station H Ottawa, Ontario, 1999.
- [12] E.A. de Kock, G. Essink, W.J.M. Smits, P. van der Wolf, J.-Y. Brunei, W.M. Kruijtzter, P. Lieverse, and K.A. Vissers. Yapi: Application modeling for signal processing systems. In *Proceedings 37th Design Automation Conference*, June 2000.
- [13] Dingninou, F. Raouafi, and C. Berrou. Organisation de la memoire dans un turbo decodeur utilisant l'algorithme SUB-MAP. In *Proceedings of GretsI*, pages 71-74, September 1999. France. M. P. C. Fossorier, F. Bukert, S. Lin, and J. Hagenauer. On the equivalence between SOVA and Maxlog- MAP decodings. *IEEE Communications Letters*, 2(5), May 1998.
- [14] W. J. Gross and P. G. Gulak. Simplified MAP algorithm suitable for implementation of turbo decoders. *IEEE Electronics Letters*, 34(16):1577-1578, August 1998.
- [15] J. Hagenauer and L. Papke. Decoding 'turbo'-codes with the soft output viterbi algorithm (SOVA). In *Proceedings of IEEE International Symposium on Information Theory (ISI T'94)*, page 164, Trondheim, Norway, June 1994.
- [16] J. Hagenauer, P. Robertson, and L. Papke. Iterative (turbo) decoding of systematic convolutional codes with the MAP and SOVA algorithms. *ITG Tagung, Codierung fur Quelle, Kanal und Ubertragung*, pages 21-29, October 1994.
- [17] Goo hyum Park, Suk hyun Yoon, Ik soo Jin, and Chang eon Kang. A block-wise MAP decoder using a probability ratio for branch metrics. In *IEEE 50th Vehicular Technology Conference*, volume 3, pages 1610-1614, September 1999.
- [18] Gibong Jeong and Dan Hsia. Optimal quantization for soft-decision turbo decoder. In *IEEE proceedings of 50th Vehicular Technology Conference*, volume 3, pages 1620-1624, September 1999.
- [19] C. G. Clark Jr and J.B. Cain. *Error correction coding for digital communications*. New York: Plenum Press, 1981.
- [20] H. Krau B. Complexity of a Max*-Log MAP decoder for use in a UMTS turbo decoder. 0.3d, Philips Semiconductors TCMC Nurnberg, July 1999.
- [21] C. Lin, C. Chen and A. Wu, Area-Efficient Scalable MAP Processor Design for High-Throughput Multistandard Convolutional Turbo Decoding," *IEEE Transactions on Very Large Scale Integrated (VLSI) Systems*, vol. 19, no. 2, pp. 305-318,2011
- [22] C. Berrou, A. Glavieux, and P. Thitimajshima, "Near Shannon Limit Error-Correcting Coding and Decoding: Turbo-Codes," in *Proc. 1993 International Conference on Communications (ICC '93)*, Geneva, Switzerland, May 1993, pp. 1064-1070.
- [23] Claude Berrou, Alain Glavieux and Punya Thitimajshima, "Near shannon limit error - correcting Coding and decoding : turbo-codes" *IEEE Transactions on Communications*, 44:1261 - 1271,Oct.1996.
- [24] Third Generation Partnership Project, "3GPP home page" www.3gpp.org. Vogt,J and Finger,A, "Improving the max-log-MAP turboDecoder," *Electron. Lett.*, vol. 36, no.23, pp.1937-1939, Nov 2000.
- [25] K. Loo, T. Alukaidey, and S. Jimaa, "High performance parallelised 3GPP turbo decoder," in *IEEE Personal Mobile Communications Conference*, April 2003, pp. 337-342.
- [26] A.J. Viterbi. An intuitive justification and a simplified implementation of the MAP decoder for convolutional codes. *IEEE J.Sel. Areas Commun.*, vol.16:pp.260-264, Feb.1998.
- [27] R. Dobkin, M.Peleg, and R.Ginosar. Parallel interleaver design and vlsi architecture for low-latency map turbo decoders. *IEEE Trans.VLSI Syst.*, 13(4):427-438, 2005.
- [28] Y.Sun, Y.Zhu, M.Goel, and J.R.Cavallaro. Configurable and Scalable High Throughput Turbo Decoder Architecture for Multiple 4G Wireless Standards. In *IEEE InternationalConference on Application-Specific Systems, Architectures and Processors(ASAP)*, pages 209-214, July2008.
- [29] J. Sun and O.Y.Takeshita. Interleavers for turbo codes using permutation polynomials over integer rings. *IEEE Trans.Inform.Theory*, vol.51:101- 119, Jan.2005.
- [30] O.Y.Takeshita.On maximum contention- free inter leaversandpermutation poly nomial sover integerrings. *IEEE Tran.Inform.Theory*, vol.52:1249-1253,Mar.2000