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Transistor Implementation of D Flip-Flop Using Reversible Logic Circuit

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***Abstract*—Reversible logic circuit is receiving attention of researchers for low power design. Flip Flop is the basic element for the sequential circuits, most of the part of the IC is built from sequential circuit, and hence it is needed to design low power flip-flop. The work is done on designing a reversible D – flip flop from a reversible Fredkin gate using GDI technique in 0.180um TSMC process, which can be used for low power design, and fault preventing circuit.**

Keyword —Reversible D flip-flop; GDI

I. INTRODUCTION

As the complexity of the circuit grows power dissipation becomes an important factor. A part of energy is dissipated during non-ideal switching of transistor. Landauer showed that amount of energy dissipated when a bit is lost is given by $KT\log_2 n$ where K is the Boltzmann's constant (1.3807X10-23 JK-1) and T is the temperature. For example, in room temperature (300 K), KT ln2 is approximately 2.8x10-21 J /transistor, which is not negligible for incoming multi-billion gate circuits. Bennet proposed that power not to be dissipated if circuit is implemented using reversible gates [1.] This solution promises the arbitrary small fraction of signal energy to be dissipated. Hence reversible logic circuit is getting attention of the researchers in many emerging fields such as nanotechnology, optical computing, and low power CMOS design. Section II gives the overview of reversible logic circuits, section III presents the circuit for d flip flop using reversible Fredkin gate, section IV presents transistor implementation of reversible D flip flop. Comparison with conventional flip-flop and conclusions are discussed in section V.

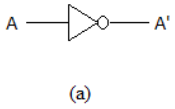
II. CONCEPT OF REVERSIBLE LOGIC CIRCUITS

A. Reversible Logic Function: A function is reversible if it satisfies following two criterions;

i. Number of inputs equal to the number of outputs
ii. Every output vector has a unique pre image

If I_v (I_1, I_2, I_3.....I_n) is the input vector and O_v (O_1, O_2, O_3 ...O_k) is the output vector then $I_v = O_v$.

B. Reversible Logic Gate: A reversible logic gate is (n x k) device where n is the number of input bits and k is the number of output bits with one to one mapping i.e. n = k



(a)

A	B
0	1
1	0

(b)

Fig.1 (a) NOT Gate (b) truth table of NOT gate

In conventional circuits NOT gate is the only reversible gate, as from output its input can be determined. While, AND OR and XOR gates are irreversible, as we can't determine input to gate from their output.

C. Quantum Cost: Every reversible gate has a cost associated with it known as quantum cost. Quantum cost of a reversible gate is the number of elementary operations required to implement its functionality, hence quantum cost defines the complexity of the circuit. Fig.1 shows a 1x1 simple NOT gate. All the reversible gates can be optimized by the NOT gate. If V is the root of NOT gate and V^+ is its Hermitian, then the quantum cost of the gate is calculated by counting the number or of V and V^+ in the gate.

The quantum gates has the following properties

$$V * V = NOT \quad (1)$$
$$V * V+ = V+ * V = I \quad (2)$$
$$V+ * V+ = NOT \quad (3)$$

D. Garbage output: This is the most important and prominent feature of reversible gate. The output of the gate which is not is used as the input to another gate is called garbage output.

A reversible gate is realized by three basic components:

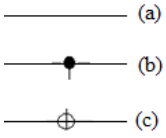


Fig.2 Components of reversible circuit (a) don't care line (b) control line (c) target line

The input on the don't care line is passed to output without change. Input at control line controls output on target line, if input to control line is '0' the input to target line will be passed as it is to its output and if input to control line is'1' the inverse of the input line is passed to its output. There have been many reversible gates synthesized [2, 3, 4], of which CNOT or Toffoli gate are used mostly to synthesize the reversible circuits. Any reversible circuit can be implemented using CNOT and TOFFOLI gate; hence these gates are called universal reversible gates.

E. NOT Gate: It is 1x1 reversible gate with zero quantum cost. The inputs get inverted at output, and hence we can determine the input to the gate, so it is the reversible gate present in conventional circuits.

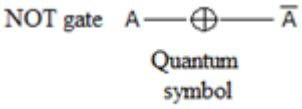


Fig.3 NOT Gate

F. Feynman/CNOT gate: It is 2x2 reversible gate with quantum cost of 1. The black dot in the circuit shown in fig 3.3 (b) is called control point. If A = 1, then inverse of B will be the output. As the NOT operation on B is controlled through control point by input A, the gate is called Controlled NOT.

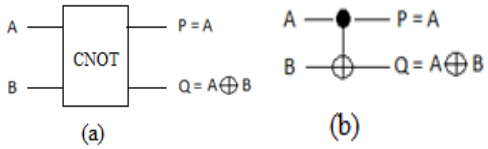


Fig.4 (a) CNOT Gate and (b) its Quantum realization

III. Design of reversible D flip-flop

To implement a flip flop we have equation,

$$Q+ = D.CLK + Q.\overline{CLK} \quad (4)$$

In literature Fredkin gate is a reversible gate whose output satisfies this equation. To make this gate to act like D-flip flop it is needed to have feedback. B is the data input; the output Q is the output of flip flop, which is feedback to input C as shown in figure 1.

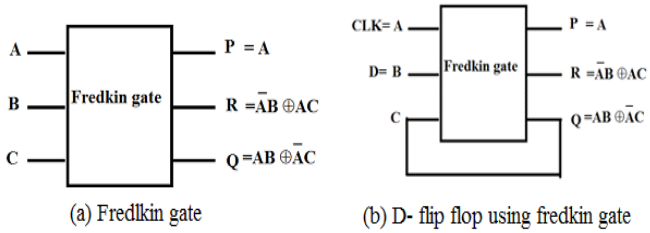


Figure.5 (a) Fredkin gate (b) D-flip flop using Fredkin gate

IV. TRANSISTOR IMPLEMENTATION OF REVERSIBLE D FLIP-FLOP

A. Gate diffusion input (GDI):

The GDI method uses a simple cell called GDI cell, shown in figure 6, it has three inputs the GDI cell contains three inputs: *G* (common gate input of both the nMOS and the pMOS), *P* (input to the source/drain of the pMOS), and *N* (input to the source/drain of the nMOS). Table I shows how a simple change to the input configuration of the simple GDI cell corresponds to a large variety of Boolean functions. Most of these functions are complex (6–12 transistors) in Static CMOS, as well as in standard PTL implementations, but very simple (only two transistors per function) in the GDI design method comparison shown in table II.

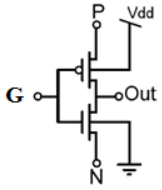


Fig.6 basic GDI cell

Similar to most of the PTL solutions, the GDI gates suffer from threshold voltage drops at their outputs. These drops affect the circuit operation in two ways: (1) performance degradation due to reduced current drive; (2) increase in the circuit's area, as cascaded regenerative inverters are required. But still the GDI technique is efficient than CMOS as it has low power dissipation [6, 7, 8].

TABLE I. BOOLEAN FUNCTION SYNTHESIS THROUGH INPUT CONFIGURATION OF GDI

N	*P*	*G*	*Out*	*Function*
0	B	A	$\bar{A}$B	F1
B	1	A	$\bar{A} + B$	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\bar{A}$B+AC	MUX
0	1	A	$\bar{A}$	NOT

TABLE II. COMPARISON OF NUMBER OF TRANSISTORS REQUIRED TO DESIGN GATES

Style	*AND*	*OR*	*XOR*
GDI	2	2	4
CMOS	6	6	12
TG	6	6	8
N-PG	4	4	6

B. Transistor implementation of reversible D flip-flop

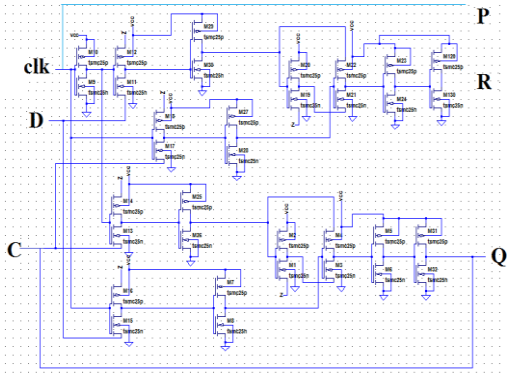


Fig.7 Implementation of Reversible D flip flop through GDI

From fig 5 implantation of the reversible D flip-flop is carried out through GDI shown in fig7. In this circuit the output R is same as clock input, so transistors forming output R are removed to reduce transistor count, which results in circuit shown in fig 8.

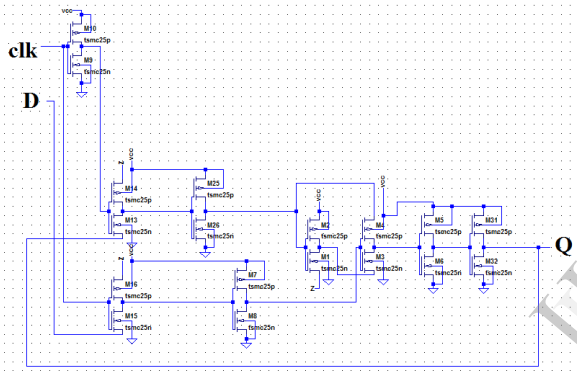


Fig.8 D flip-flop using Reversible logic circuit

C. Comparison of Reversible and Conventional D flip-flop

The conventional circuit for D flip-flop implemented through GDI is given in paper [9].

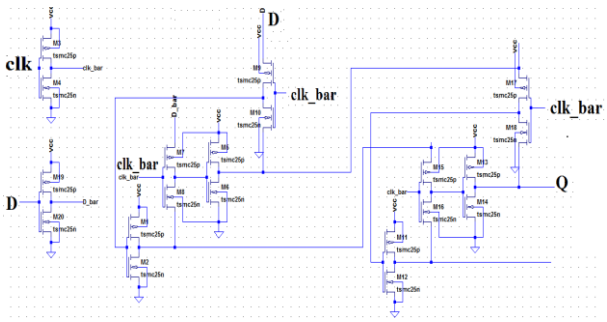


Fig.9 conventional GDI flip-flip

TABLE III. COMPARISON BETWEEN CONVENTIONAL AND REVERSIBLE FLIP FLOP

	Transistors	***Power (μW)***	***Delay (ps)***	***PDP (fs)***
Conventional circuit	20	916.91	347.10ps	333
Using Reversible logic circuit	18	426.17	66.77ps	28.45

CONCLUSION

In this paper transistor implementation of D flip-flop using Reversible logic circuit is carried out. The analysis is shown in table III, indicating that about 40% less power is dissipated than the conventional circuit. This circuit can be used to design registers and memories for ultra low power design.

REFERENCES

[1] Bennett, C.H., "Logical reversibility of Computation", IBM J.Research and Development 17: pp. 525-532, 1973.

[2] Prashant Yelekar, Introduction to Reversible Logic Gates & its Application, 2nd National Conference on Information and Communication Technology (NCICT) 2011 Proceedings published in International Journal of Computer Applications (IJCA).

[3] Raghava Garipelly, P.Madhu Kiran, A. Santhosh Kumar, Review on Reversible Logic Gates and their Implementation, IJETAE Volume 3, Issue 3, March 2013.

[4] Madhusmita Mahapatro, Sisira Kanta Panda, Design of Arithmetic Circuits Using Reversible Logic Gates and Power Dissipation Calculation, 2010 International Symposium on Electronic System Design, 2010 IEEE.

[5] Madhina Basha, V. N. Lakshmana Kumar, Transistor Implementation of Reversible Comparator Circuit Using Low Power Technique, International Journal of Computer Science and Information Technologies,Vol. 3, 2012.

[6] Morgenshtein, Idan Shwartz and Alexander Fish, Gate Diffusion Input (GDI) Logic in Standard CMOS Nanoscale Process, 26-th Convention of Electrical and Electronics Engineers in Israel. 2010 IEEE.

[7] Arkadiy Morgenshtein, Alexander Fish, Gate-Diffusion Input (GDI): A Power-Efficient Method for Digital Combinatorial Circuits, and Israel A. Wagner, IEEE transactions on very large scale integration (VLSI) systems, VOL. 10, NO. 5, OCTOBER 2002.

[8] Y. Syamala, K. Srilakshmi and N. Somasekhar Varma, design of low power cmos logic circuits using gate diffusion input (GDI) technique, International Journal of VLSI design & Communication Systems (VLSICS) Vol.4, No.5, October 2013.

[9] Arkadiy Morgenshtein, Alexander Fish and Israel A. Wagner, An efficient implementation of D-flip-flop using the GDI technique, ISCAS 2004 IEEE.