

Time Interval Measurement using Analog & Digital Methods - A Comparative Study

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Abstract—The paper is a comparative study of methods & techniques, especially Analog & Digital, used for time interval (TI) measurement in Nuclear Timing Spectroscopy Systems. The paper is a review of summarized results of Time-to-digital counter method with averaging and time-to-amplitude conversion followed by analog-to-digital conversion using single ADC and two tracking ADCs. Authors have designed, implemented these various methods and their performance is evaluated. All these methods are compared for their resolution, accuracy, temperature drift. Advantages offered by these methods are listed with respect to conventional nuclear timing spectroscopy system.

Keywords—Nuclear timing spectroscopy system, Time to Digital converter, Time Interval measurement, Time to Amplitude converter

I. INTRODUCTION

In many physics experiments, time-of-flight measurements and nuclear timing spectroscopy systems, a need arises to measure short time intervals (TIs) with pico-seconds (ps) resolution and good accuracy, refer [1], [2]. This paper summarizes the results obtained from various methods, designed and implemented for TI measurement by authors. Resolution offered by these methods is of the order of 106 ps in the measurement range of 3.5 μ s, although some methods can be easily adapted to extend the measurement range upto few tens to hundreds of ms.

The conventional nuclear timings spectroscopy system, as shown in Figure 1 comprises Time-to-Amplitude Converter (TAC) to convert TI between the START and STOP pulses into equivalent amplitude i.e. analog voltage. START and STOP pulses are generated by Time Pick-off circuit which are time-correlated with the pulses received from the detectors corresponding to one nuclear event. STOP pulse is delayed by fixed time period for proper operation of

Timing spectrum is developed using this digital code. Because of delay component, the spectrum is shifted in the time domain. To improve the resolution with the existing MCA which has limited number of channels, biased amplifier is used which removes the dc offset from the TAC output voltage. The conventional approach of measuring TI faces limitations because of performance issues of individual components like delay and biased amplifier. Also, the time-walk produced in the output pulses of time pick-off circuit adds to the jitter in the TI measurement. Non-linearity contributed by TAC in the conversion process also affects the accuracy of TI measurement. The conventional system components are sensitive to ambient temperature and the system has typically a longer conversion time of the order of 10 μ s. Authors have explored various methods of TI measurement, as explained below to overcome the limitations of conventional approach.

II. TI MEASUREMENT METHODS

A. Programmable Time to Digital Converter

This is digital method of TI measurement where input TI is stretched and then counted by counter method, refer [3]. Incoming TI between START and STOP pulse is converted into equivalent voltage V_1 , refer Figure 2. At the arrival of START pulse, positive slope generator starts building ramp as negative current I_1 is connected at the reference input. During time interval T_1 , ramp increases in positive direction. When STOP pulse is received, positive current I_2 is connected to negative slope generator, so ramp starts decreasing in the negative direction. Digital-to-Analog converters (DACs) are used to generate precise currents I_1 , I_2 in proportion to reference voltages provided at the input, -12V and 4.096V respectively. Current values are also proportional to the digital code applied to DACs which is same for both the DACs. Ratio of currents is maintained to $12/4.096 = 2.92$. Hence T_2 period is elongated compared to time period T_1 . Counter is enabled during period T_2 and counter digital output is proportional to T_2 . As the incoming TI increases, voltage V_1 reached during time period T_1 increases, in proportion to this time period, T_2 also increases. Therefore, counter output is proportional to the time period T_1 which is in proportion to the incoming TI.

Clock period of 50 ns is obtained using crystal controlled oscillator of 20 MHz frequency. As the time period T_2 is stretched, it helps to improve the resolution of the Time to Digital Converter (TDC) by stretching factor K , where

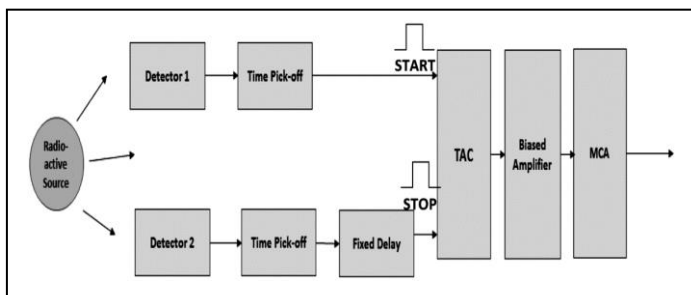


Figure 1 Nuclear Timing Spectroscopy System

TAC. TAC output voltage is digitized using Analog-to-Digital Converter (ADC) internal to Multi-channel Analyzer (MCA).

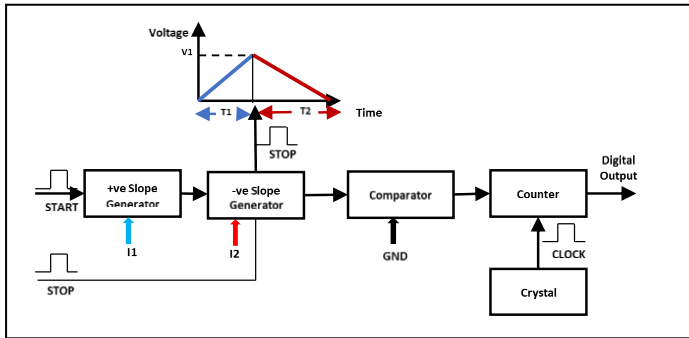


Figure 2 Programmable Time to Digital Converter

$$K = \frac{T2}{T1} \quad (1)$$

$$T2 = K * T1 = n * To \quad (2)$$

where 'To' is clock period and 'n' is decimal equivalent of binary count of the counter in (2).

$$T1 = \frac{(n * To)}{K} \quad (3)$$

Thus, resolution of TDC is improved by stretching factor K. Clock period is $n = 50$ ns, with $K = 2.92$, resolution obtained by this method is $50\text{ns} / 2.92 = 17.12$ ns. Resolution can be further improved by increasing value of K, but then large number of counter ICs are required to count time period T2. Also, conversion time of TDC increases in proportion to elongated time period T2. Therefore, value of K has to be optimum combination of range and resolution. The implemented design of TDC offers improved resolution compared to conventional counter method. Four 4 bit counter ICs are used, so the range of TDC is $(2^4 * 16) * 50\text{ns} = 3276.8$ μs . DAC output currents I1, I2 can be changed by controlling the digital code to DAC. Thus, slope of ramps can be controlled resulting into different ranges of time interval measurement. System components and hence currents I1, I2 may change because of temperature effect. But both the currents will change in similar manner, which will result in similar effect on time period T1 and T2. So, the final digital count corresponding to input TI remains largely unaffected because of temperature effects.

Performance of the system is evaluated initially using slow clock of 6.4 μs period for measurement of TI of 60 μs , refer Figure 3. T2 period is stretched to 140 μs approximately and counted by counter, refer Figure 4.

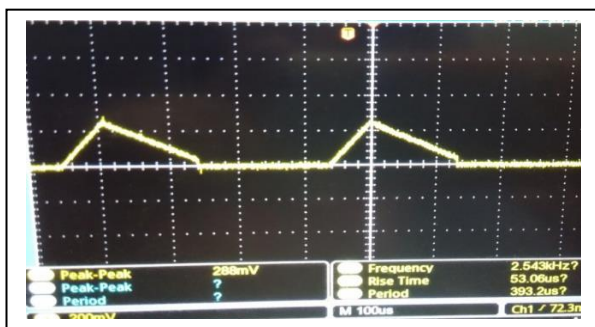


Figure 3 Time Interval TI of 60 μs

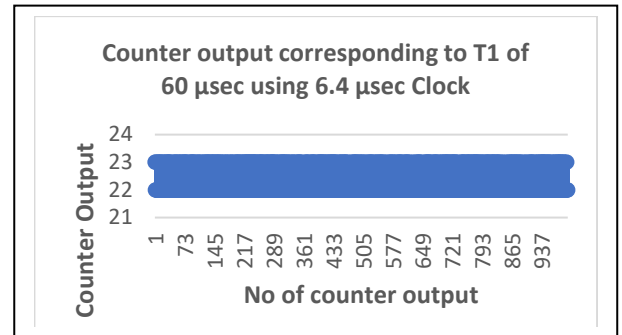


Figure 4 TDC Counter 1000 readings for TI T1 of 60 μs

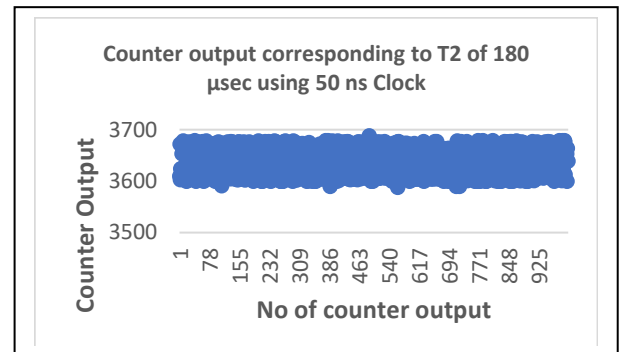


Figure 5 TDC Counter 1000 readings for TI T2 of 180 μs

Average of 1000 counter digital output is computed which is close to 22. So, with 6.4 μs clock period, $22 \text{ count} * 6.4$ $\mu\text{s} = 140$ μs .

TDC performance is further tested with 50ns clock period for time period T2 of 180 μs , counter 1000 readings are displayed, refer Figure 5. TDC resolution can be further improved by using crystal controlled oscillator of higher frequency.

B. Time to Amplitude Converter followed by single ADC

In this method, TAC produces ramp of fixed duration which is connected to ADC input, refer [4]. System design is tested for ramp of duration 25.6 μs . TAC starts building ramp at the arrival of START pulse, using integrator circuit as shown in

Figure 6. START pulse is generated using analog switch which governs the charging and discharging of capacitor in the integrator circuit. Ramp is also connected as input to comparator which is provided with reference voltage at the other input. When ramp crosses threshold voltage,

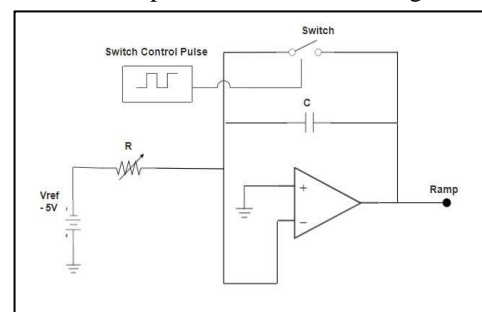


Figure 6 Ramp Generation Circuit

comparator output goes high, which is treated as STOP pulse. This is how STOP pulse can be shifted on the entire duration of ramp by varying reference voltage to the comparator. Further precise TIs of 5ns and 1 ns are obtained using 8 bit programmable delay generator (PDG) ICs. Comparator output is provided to the input of PDG and delayed output from PDG is used as STOP pulse. When STOP pulse arrives, ADC receives START conversion pulse. ADC digital output code is equivalent to time interval between START and STOP pulse. Successive Approximation (SAR) ADC of 16 bit is used which has conversion time of 1 μ s. The total dead time of the system can be reduced to 1 μ s using onboard memory to store ADC values. The dead time of this system is much lower compared to the conventional nuclear timing spectroscopy system which is of the order of 10 μ s. With this reduced dead time of the system, the system is capable of handling typical nuclear event rate of 100 KHz.

ADC code variation is observed for one particular TI using comparator output as STOP pulse, refer Figure 7. The code variation is observed because of jitter in analog switching time, noise in the input voltage to ADC, jitter in comparator output variation, nonlinearity error in ramp output, ADC nonlinearity. ADC code variation is also observed for one particular TI using PDG output as STOP pulse, refer Figure 8. Comparator output is connected to PDG and PDG code is set to give desired delay at the output. The delayed output of PDG is used as STOP pulse.

The designed system needs to make use of delay component to delay STOP pulse after START pulse. But biased amplifier is not required which is used in conventional system. SAR ADC used for to build this system offers 65K channels which are very large in number compared to 8K channels offered by MCA used in the conventional system.

C. Time to Amplitude Converter followed by Two Tracking ADCs

A totally new integrated system is proposed, designed, and implemented, as discussed in [5]. Free running ramp generation circuit produces periodic ramp of time period 25.6 μ s, as shown in Figure 9. Ramp is given as input to two tracking ADCs. At the arrival of START pulse at time instant

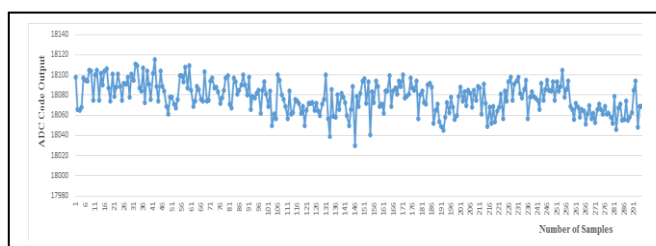


Figure 7 ADC code variation using comparator output as STOP pulse

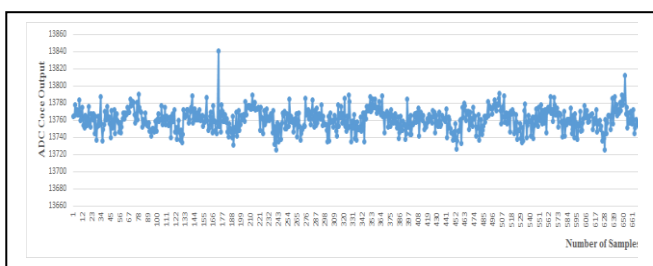


Figure 8 ADC code variation using PDG output as STOP Pulse

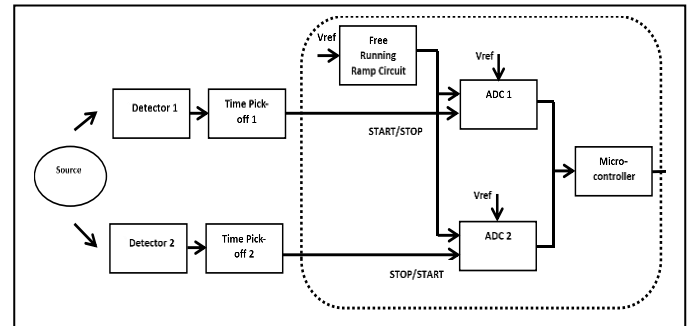


Figure 9 Integrated System with Two Tracking ADCs

T1, ADC1 receives start conversion pulse (SOC) and ADC1 digitizes ramp voltage corresponding to time instant T1 and produces code D1. At the arrival of STOP pulse, ADC2 receives SOC and ADC2 digitizes ramp voltage corresponding to time instant T2 and produces code D2. The difference in two ADCs code, (D2-D1) is computed which is proportional to time interval TI. If STOP pulse comes after START pulse, then ADC2 code will be greater than ADC1 code. However, the difference between the two codes remains the same and proportional to input TI. When timing spectrum is developed using digital code of ADC, the events corresponding to $D2 > D1$ are plotted on the right side of the time axis, whereas event corresponding to $D2 < D1$ are plotted on the left side of the time axis.

The system has provision of changing ramp duration from 100 ns to few hundreds of μ s. 16 bit SAR ADC is used in the system. So, by changing ramp period and with the existing 65K channels of ADC, TI measurement range and resolution can be governed. Much larger range (μ s) with ps resolution is attained by this method compared to conventional system range of ns with ps resolution. The integrated system doesn't require delay component, hence the need of biased amplifier is automatically eliminated. TI measurement is independent of input source voltage fluctuations, ramp slope variations. Dead time of system can be reduced to 1 μ s. Further the ramp generation and ADCs are made to track over the entire temperature range because of which the spectrum stabilization is easy. Also the ADCs used are SAR ADCs with very low acquisition jitter of few ps.

The performance of the system is tested with ramp of 3.5 μ s duration, refer Figure 10. Ramp is connected to two tracking ADCs input, as well as to the comparator input. Other input of comparator is provided with the reference voltage. When

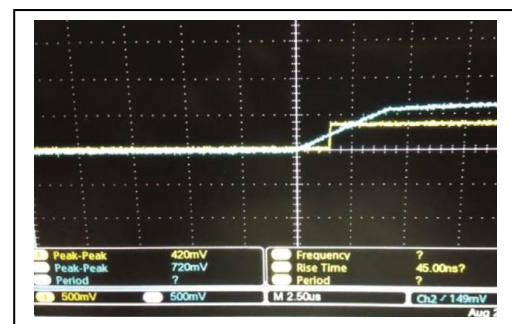


Figure 10 Two tracking ADCs System - Ramp of 3.5 μ s duration

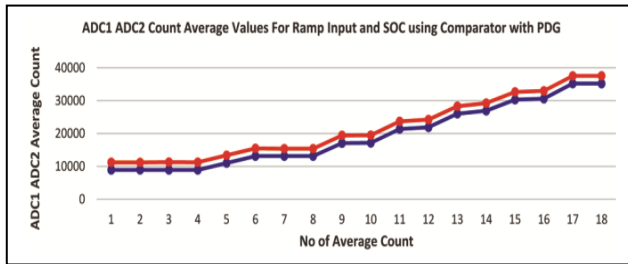


Figure 11 Two tracking ADCs system – Ramp Linearity

ramp crosses reference voltage, comparator output goes high. Comparator output pulse is connected to PDG, where the digital code of PDG is set to give 1 μ s delay at the output. PDG sources two types of output, one is reference output and the another one is delayed output. Reference output of PDG is used as SOC pulse for ADC1 and delayed output is used as SOC pulse for ADC2. Comparator output is shifted on the entire section of the ramp to test non-linearity of the ramp. In case of any jitter at the output of PDG, it will remain present in both SOC pulses used for ADCs, hence TI measurement should remain unaffected. The experiment has shown quite linear result. As shown in Figure 11, comparator reference is maintained at one value, 1000 readings are obtained from both the ADCs for this event of START and STOP pulses, average of 1000 readings computed and plotted in the graph. Then the comparator reference is changed for the next level on the ramp. This is a continuous experiment which is performed.

Also, the best possible resolution for the implemented system was measured and ADC code variation was observed because of all sources of noise which could be present in the system. With 16 bit ADC, the resolution expected for the system is $3.5 \mu\text{s} / 65536 = 53 \text{ ps}$. The ADC code offset variation is seen to be ± 2 counts about the offset average value, refer Figure 12. This shows that the offset variation for ramp input is of the order of $53 \text{ ps} * 2 = 106 \text{ ps}$. Hence TI resolution of the order of 100 ps can be precisely attained using this integrated system. Further experiment was conducted to measure individual ADCs nonlinearity error. For the given ramp at the input of two ADCs, SOC is provided to the two ADCs at the same time instant. Assuming extreme conditions, i.e. ADC1 code varies by $+0.5 \text{ LSB}$ and ADC2 code varies by -0.5 LSB , then the maximum error or spread in TI measurement would be 1 LSB. The ADCs code is obtained and the difference between the two ADCs code is computed. Further the variation of this difference is plotted using LabVIEW software. Figure 13 shows the developed spectrum and Full Width at Half Maximum (FWHM) is observed in the spectrum. It is found that the maximum spread in TI

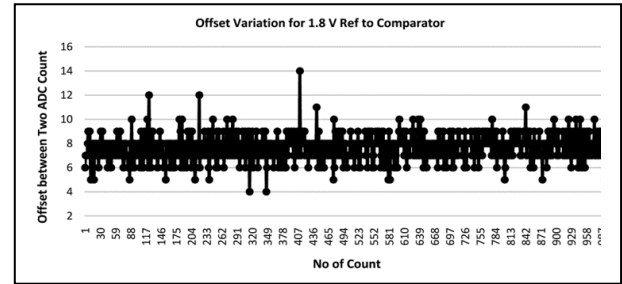


Figure 12 ADCs code offset variation

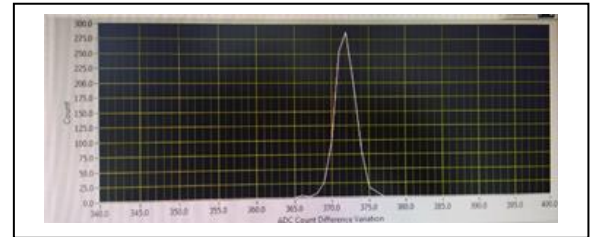


Figure 13 Spectrum Development

measurement, i.e. FWHM is $\text{LSB} * 2 \text{ counts}$ (i.e. $53 \text{ ps} * 2 = 106 \text{ ps}$), which includes all the errors and factors for the TI spread in the measurement system. This spread counts for ramp nonlinearity, ADCs nonlinearity, ADCs aperture jitter variation, comparator output jitter variation. Spectrum proves that the integrated system can be reliably used for ps TI measurement in nuclear timing spectroscopy systems. Further the spread can be reduced 1.5 ps by using ramp duration of 100 ns.

III. COMPARATIVE STUDY

The performance issues, analysis and a comparative of analog and digital methods implemented for TI measurement is discussed below

A. Resolution

In basic digital method, the resolution is decided by the basic clock period, T_0 . Hence to obtain better resolution, fast clock and therefore, high speed counter ICs are required. In the designed TDC method, time stretching is proposed, because of which the resolution is improved by a factor of K. But increasing K, result into increase of conversion time and dead time of the system. Also, the counter ICs required to count elongated time period T_2 , increases in number. Therefore, optimum value of K has to be used which gives best combination of resolution and conversion for the system.

In single ADC or two tracking ADCs method (Analog method), resolution of the system is governed by ramp duration and ADCs number of bits. So, with ramp of short duration like 600 ns, and 16 bit ADC, resolution $= 600 \text{ ns} / (2^{16}) = 10 \text{ ps}$ approximately. Very fine resolution of ps can be obtained using analog method. However, in conventional analog method, range is limited to few ns for obtaining ps resolution. This limitation is overcome in the designed integrated system by adapting to free running ramp technique.

B. Accuracy

TDC (Digital method) uses digital clock and counter to count the elongated time period T_2 which is proportional to T_1 at the input. Because of clock and START or STOP pulse misalignment, the error in the measurement can be maximum $\pm T_0$, where T_0 is the clock period. If the method makes use of 20 MHz clock, the time period is equal to 50 ns. Because of stretching factor K , the actual resolution is enhanced to 25 ns. But, the inaccuracy in the measurement can be of the order of 50 ns, which is almost 200% of the resolution offered by TDC. The inaccuracy in the measurement can be minimized by using averaging method, i.e. to take 1000 reading of the same event, and take the average. But this process can be time consuming, also not suitable for dynamic process.

In single ADC or two tracking ADCs method (Analog method), the resolution offered is ramp duration / Number of bits of ADC. e.g. in the implemented two tracking ADCs system, the system was tested for resolution of $600 \text{ ns} / 65536 = 10 \text{ ps}$. The factors which can affect the T_1 measurement accuracy are – ramp nonlinearity, comparator jitter, ADCs nonlinearity, ADCs acquisition jitter. Ramp nonlinearity would affect both the ADCs code in the similar manner, hence the T_1 measurement will remain unaffected. Comparator jitter appears in both START and STOP pulse, so the measurement should not get affected. However, ADCs individual nonlinearity may affect the measurement. So, the experiment was conducted to observe this effect on T_1 measurement, refer

Figure 13. The experiment shows that the spread in the spectrum is close to 2 counts, which is few ps. Therefore, it can be concluded that the analog method can be used for find resolution of ps with much better accuracy compared to digital method.

C. Dead Time

In TDC method, the total conversion time is time period T_1 + time period T_2 . Time period T_2 is stretched to increase the resolution of the system with the existing clock frequency and counter ICs speed. This elongation factor K increases the conversion time and hence dead time of the system. Also, the conversion time is proportional to the T_1 at the input, and increases with the T_1 .

In analog method, dead time is mainly decided by the conversion time of the ADC. 16 bit SAR ADC with conversion time of $1 \mu\text{s}$ is used. So the dead time of the system can be reduced to almost $1 \mu\text{s}$. This enables the system to digitize event rate of the order of 100 KHz which is typical event rate in nuclear timing spectroscopy applications. The conventional timing spectroscopy systems makes use of special nuclear ADCs which limits the conversion time to almost 10 μs . Also, the conventional systems make use of MCA which has limited number of channels, 8K. The proposed system offers much large number of channels which is 65 K.

D. Ramp Nonlinearity / Temperature Drift

Both analog and digital methods make use of integrator circuit to generate ramp. Since opamp based circuit is used, longer duration ramp can be generated. DAC is used to set the precise current in the integrator circuit. Therefore, ramp slope can be governed with fine precision. Nonlinearities may arise because of leakage current in the analog switches (refer

Figure 6), opamp input bias current, leakage current of charging capacitor. However, the nonlinearity contributed by all these factors is of the order of few nA, which is much less than the current equivalent to 1 LSB of the system (typically μA).

In TDC method, the input T_1 is converted into equivalent ramp of time period T_1 and this period is elongated to time period of T_2 . Because of resistors, capacitors sensitivity towards temperature, slope of ramp may vary. But if ramp slope decreases for T_1 period, then the ramp slope decreases in the same proportion for T_2 period. This has been proved in terms of mathematical equations in [3]. Hence it is shown that in TDC method, T_1 measurement is not affected because of ramp nonlinearity or temperature effect.

In analog method, if ramp slope changes because of temperature drift in resistor and capacitor values, since the same ramp is provided to the input of both the ADCs, the effect will be cancelled out in T_1 measurement.

E. Conversion/Digitization Nonlinearity

TDC method makes use of counter ICs to count time period T_2 . Digital counter ICs have proved to be precise and the T_1 measurement would be accurate except the jitter of $\pm T_0$, where T_0 is basic clock period. This jitter can be minimized by using averaging method, as explained earlier above in B.

In analog method, ADCs used for digitization process play crucial role in defining the nonlinearity of this conversion process. ADCs used in nuclear timing spectroscopy system are preferred to be the one which have low DNL error. INL error results into spectrum peak shift which doesn't affect the T_1 measurement. But DNL error can result into T_1 measurement inaccuracy. So conventionally ADCs like Wilkinson ADC is preferred for nuclear applications which has low DNL error, but it has large conversion time. Thus, the event rate gets limited for the system. Authors have proposed integrated system which makes use of SAR 16 bit ADC which has low conversion time of $1 \mu\text{s}$ and very low acquisition jitter of few ps. Though SAR ADCs offer low conversion time, which enables system to digitize high event rate, SAR ADCs do impose the limitations on the system because of wide DNL error. However, the proposed integrated system makes use of two ADCs which are tracking ADCs. So if one ADC' DNL error is $+0.5 \text{ LSB}$, and other ADC'

error is -0.5 LSB, this may result into total error of 1 LSB. But the TI events can take place over the entire ramp on any section, so automatically the nonlinearities in the channels of ADCs are compensated.

IV. CONCLUSION

Authors have explored digital method in TDC as well as analog method in integrated system. It is clear from the above III comparative study, where both the methods have been compared for resolution, linearity and accuracy. Also, the integrated system advantages have been stated over conventional nuclear timing spectroscopy system. It is observed that for large time interval range of few μ s to few ms,

digital counter methods are used and to obtain fine resolution of few ps, hybrid methods are used which combine digital counter method with analog ADC method. These hybrid methods suffer because of inaccuracies contributed by digital as well as analog methods. Also, the error code because of digital method doesn't match with the one of analog method. Hence the authors have proposed new integrated system of two tracking ADCs which has given performance results of the order of few ps resolution over extended TI range of few hundreds of μ s.

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