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Three Phase Asymmetric Multilevel Inverter with Reduced Number of Switches for Improved Harmonic Performance

Neeraj Seth
M.Tech. Student
Sardar Patel College of Engineering,
Andheri, Mumbai 400058

R. D. Kulkarni
Member, IEEE
Head, EFS, Reactor Engg. Division,
Bhabha Atomic Research Centre,
Trombay, Mumbai 400085

V. P Joshi
Head, Dept. of Electrical Engg.,
Sardar Patel College of Engineering,
Andheri, Mumbai 400058

***Abstract*—The paper introduces an Asymmetric topology of three phase Multi-Level (seven level) Inverter (MLI) with reduced number of switches. This topology facilitates reduction in Total Harmonic Distortion (THD) and number of switches. Amongst the conventional techniques e.g. Diode Clamp, Flying Capacitor and Cascaded Multilevel Inverter, Cascaded Multi-Level Inverter (CMLI) requires lesser number of components. In case of seven level, three phase multilevel inverter, conventional CMLI requires thirty six switches whereas the proposed topology needs only twelve switches for the generation of three phase seven level output voltage. The Multi-carrier Sinusoidal Pulse Width Modulation (MSPWM), the Carrier Disposition (CD) in particular, along with appropriate logical circuitry is used to generate the required gate pulses for triggering a designated switch. The proposed topology is successfully simulated and verified in simu-link selecting 1 kHz carrier frequency.**

Keywords— Asymmetric topology, Cascaded Multilevel Inverter, Total Harmonic Distortion, Multi-carrier Sinusoidal Pulse Width Modulation.

I. INTRODUCTION

Recently for medium and high-voltage, high-power industrial & research applications [1-4] multi-level Voltage Source Inverters (VSI) are extensively accepted. Inverters synthesize better output voltage and current waveforms with reduced harmonics [5] thus, providing unique solution for the desired applications. Various industrial applications where multilevel inverter technology is extensively used covers the areas such as speed control of single phase as well as three phase induction motors, hybrid active harmonic filters, reactive power compensation, renewable energy sector, traction, plug in hybrid electric vehicles and many more. However, they requires high number of components such as input DC sources and power electronic devices i.e. IGBTs, MOSFETs and the required gate driver circuitry. But, these limitations are overcome by their advantages such as low dv/dt, small output filter size as the dominant harmonics are significantly reduced, low electromagnetic interference and reduction in Total Harmonic Distortion (THD) in output voltages. A broad classification of different multilevel inverter topologies are classified into two main categories [6]: (1) Single dc-source inverters, for e.g. Neutral-Point-Clamped (NPC) multilevel inverter and Flying Capacitor multilevel inverters (2) Multi-DC sources inverters, for e.g. Cascaded H-Bridge (CHB) multilevel inverter [7-8]. Further, multi-DC source inverter is classified into symmetrical (equal DC source) and asymmetrical (unequal DC source) topologies. Fundamentally, asymmetrical topologies produce more voltage levels as compared to symmetrical topologies keeping same DC sources. Recently, asymmetrical topologies are becoming one of the most interested research areas [9-10] in the field of power electronics and applications. In the asymmetrical configurations, the magnitudes of input DC voltage sources are unequal. The size of these topologies is substantially reduced improving the overall reliability, since minimum number of power electronic components and DC sources are used. Considering the above mentioned types of multilevel inverters, there are three basic conventional multilevel inverter topologies: Diode Clamped Multi-Level Inverter (DCMLI), Flying Capacitor and Cascaded Multilevel Inverter. The DCMLI [11-12] basically uses the clamping diode to get the desired step in the output waveform of the inverter. It is a widely used topology that gives the output voltage levels with the help of clamping diodes. The key concept of DCMLI is the reduction of voltage stress in the power electronic devices with the help of diode. A typical n-level DCMLI needs (n-1) voltage sources, {2(n-1)} switching devices and {(n-1)(n-2)} diodes [13]. Fig.1 shows the structure of 7-level Diode clamped multilevel inverter.

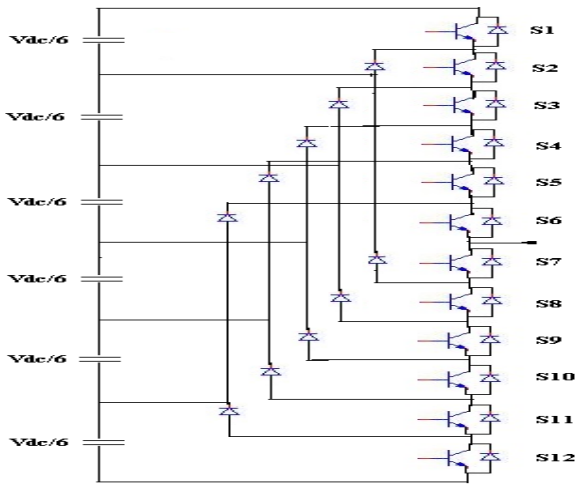

Fig.1 Seven level Diode Clamped Multilevel Inverter

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The second topology is the Flying Capacitor Multi-Level Inverter (FCMLI) [14], the structure of which is similar to that of DCMLI. Similarly, for an n-level FCMLI, it will require {(n-1)(n-2)/2} clamping capacitors per phase leg in addition to (n-1) main DC capacitors. The voltage stress across each power electronic switch has to be same and equal to {Vdc/(n-1)} for n level multilevel inverter, this is assured by the proper connection of capacitors of FCMLI. But, the major limitation of FCMLI is the number of capacitors involved comparative to other multilevel inverter topologies. Fig.2 shows the structure of five level FCMLI.

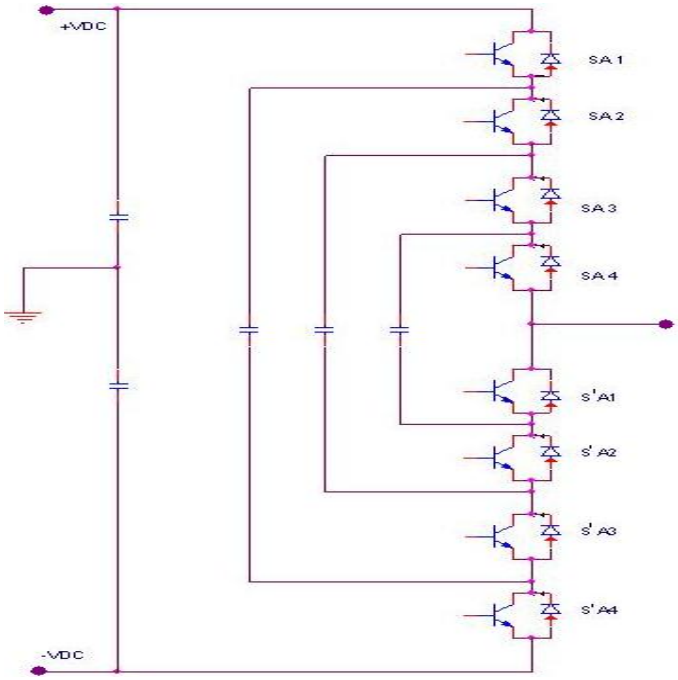

Fig.2 Five level Flying Capacitor Multilevel Inverter

The third topology is Cascaded Multi-cell Inverter topology which consists of number of power electronic switches connected in proper combination with series connected DC sources to give the various levels in the output voltage. Number of input DC sources (m) connected in series gives the number of output voltage level that can be written as (2m+1). CMLI has the least complex structure that requires lesser number of components compared to other types of multilevel topologies.

Besides, conventional two level inverter requires a large and expensive LC output filter and can only be used with the application that can withstand such stresses. The, conventional inverters have some more disadvantages when operating at high frequency, mainly due to higher switching losses and constraints of the device ratings. In view of the above discussions, the technical and economic aspects for the development of multilevel inverters are as follows.

1) Modular realization
2) High availability
3) Failure management and
4) Investment and life cycle cost.

A broad classification of DC-AC power conversion (Inverter) is shown in Fig.3.

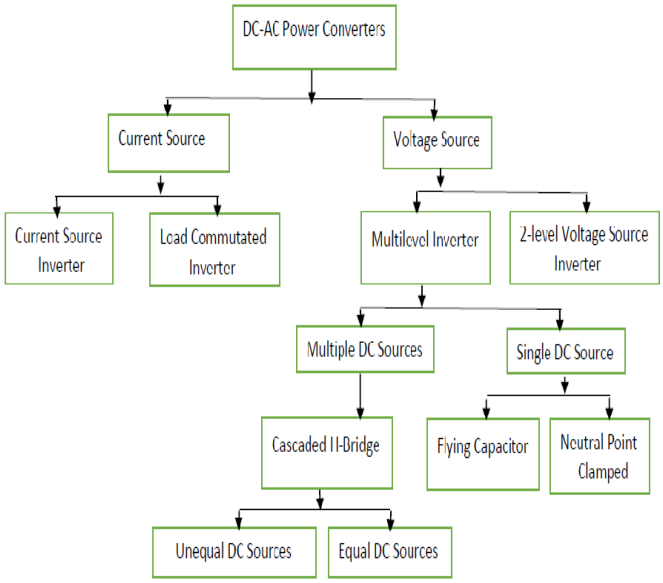

Fig.3 Classification of Multilevel Inverter

II. Conventional Cascaded H-Bridge Multilevel Inverter

It is composed of multiple units of single phase H-bridge power cells; each cell consists of two legs in parallel powered by isolated DC sources. Each leg consists of two series connected power electronics switches. The inverter input DC voltage is usually fixed, while its ac output voltage can be adjusted by different modulation schemes. For achieving the N level with symmetric CHB, it requires {(N-1)/2} number of cells per phase and {2(N-1)} number of switches per phase. Hence for three phase seven level output, it requires nine cells and thirty six switches. Fig. 4 shows the basic structure of single H bridge cell whereas Fig. 5 shows the three phase seven level CHB multilevel inverter.

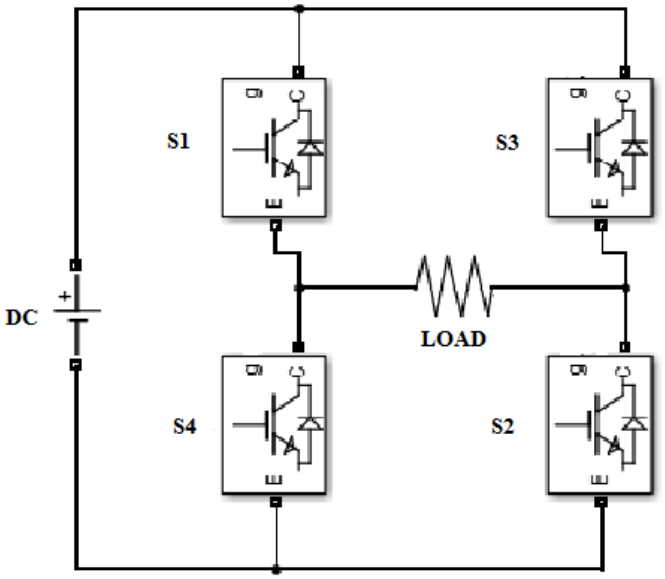

Fig.4 Structure of Single H bridge cell

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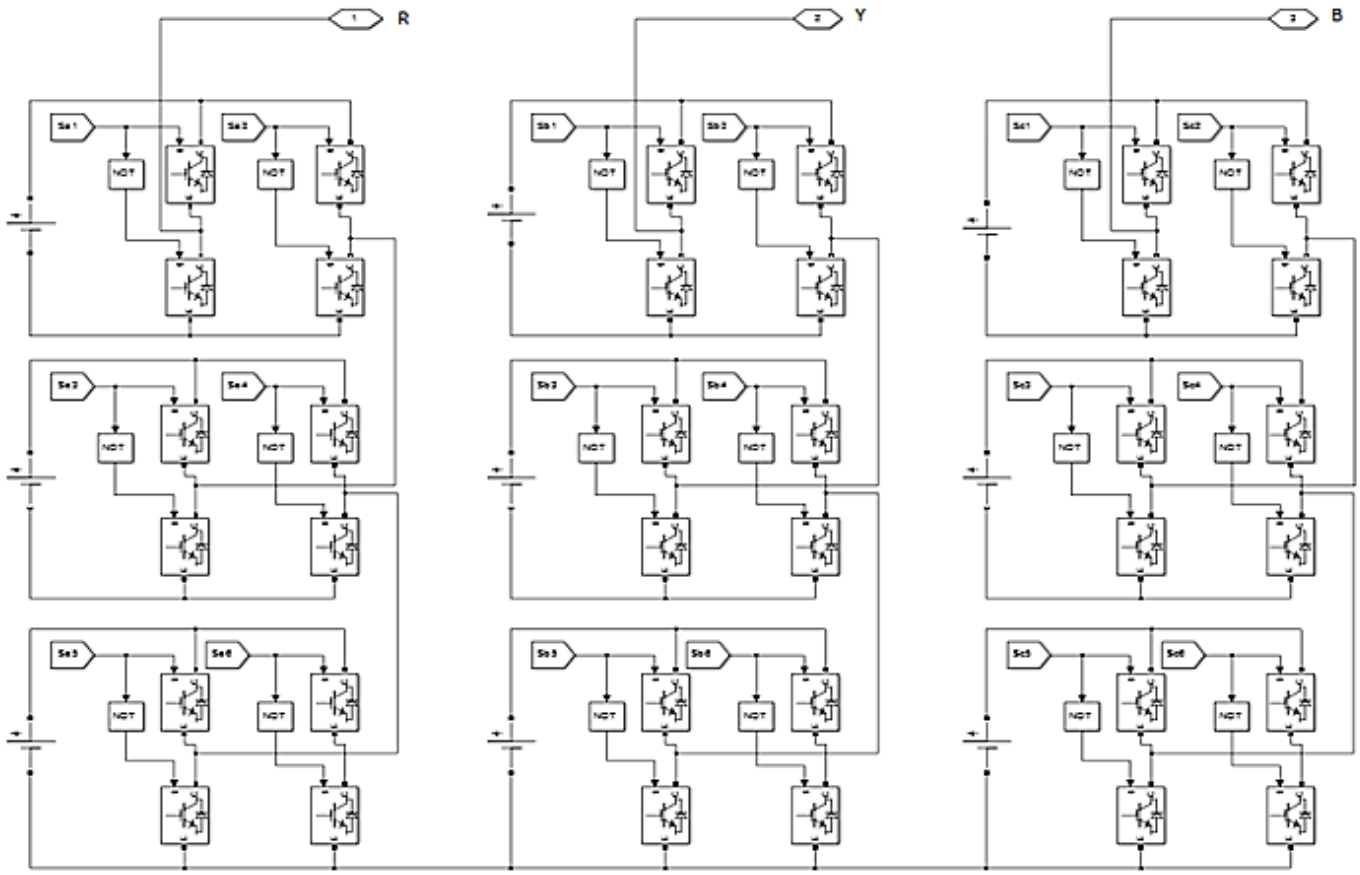

Fig.5 Conventional three-phase seven level Cascaded H-Bridge Multilevel Inverter

III. Proposed Assymetric Topology

This topology presents an asymmetric configuration (input DC sources are of unequal magnitude) for three phase seven level inverter with reduced number of switches. To generate three phase seven level output voltage, the proposed topology requires only twelve switches instead of thirty six switches which are needed in CHBMLI. Fig. 6 shows the simulation circuit of the proposed topology simulated in Simu-link. It contains three legs and each leg contains two cells. Each cell contains two switches and one DC source. For e.g. switches S1 and S2 are in same cell and the generated levels of output voltage waveform are: 0Vdc, ±1Vdc, ±2Vdc, ±3Vdc. As 1Vdc=150V and 2Vdc=300V, hence generated seven voltage levels are: 0V, ±150V, ±300V, ±450V. For achieving the desired output voltage levels, each phase requires four switches and two voltage sources having different magnitudes. Therefore, for three phase output, it requires three voltage sources having magnitude 1Vdc (150V) and three voltage sources having magnitude 2V (300V).

For achieving a desired level, the switches are triggered by a particular well defined pulse pattern. Switching strategy for the proposed topology is shown in Table I. It may be noted that one cycle of reference sine wave has eighteen modes of switching states. It can be clearly observed from the switching table that at any instant of time, six switches are ON and six switches are in OFF condition.

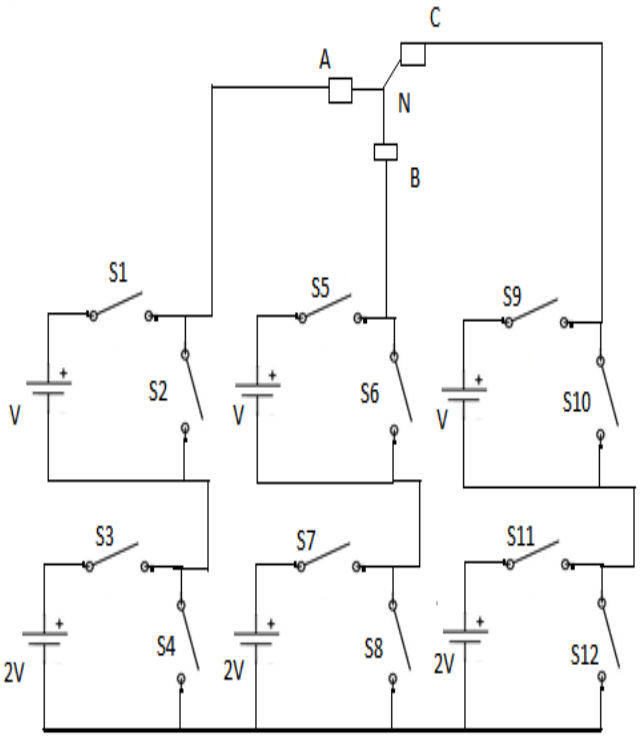

Fig.6 Block diagram of proposed asymmetric topology

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TABLE I. SWITCHING STRATEGY FOR PROPOSED ASSYMETRIC TOPOLOGY

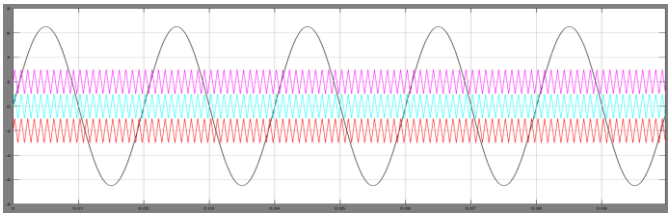
Mode	Switching states												Line voltages		
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	Vab	Vbc	Vca
1	OFF	ON	ON	OFF	OFF	ON	OFF	ON	ON	OFF	ON	OFF	2V	-3V	V
2	ON	OFF	ON	OFF	OFF	ON	OFF	ON	ON	OFF	ON	OFF	3V	-3V	0
3	ON	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	ON	ON	OFF	3V	-2V	-V
4	ON	OFF	ON	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	ON	3V	-V	-2V
5	ON	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	ON	3V	0	-3V
6	ON	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	ON	2V	V	-3V
7	ON	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	ON	V	2V	-3V
8	ON	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	ON	0	3V	-3V
9	OFF	ON	ON	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	ON	-V	3V	-2V
10	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	ON	-2V	3V	-V
11	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	ON	-3V	3V	0
12	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	ON	-3V	2V	V
13	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	ON	OFF	-3V	V	2V
14	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	ON	OFF	-3V	0	3V
15	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	ON	OFF	-2V	-V	3V
16	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	ON	OFF	-V	-2V	3V
17	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	ON	OFF	0	-3V	3V
18	ON	OFF	OFF	ON	OFF	ON	OFF	ON	ON	OFF	ON	OFF	V	-3V	2V

Basically switches S1, S2, S3, S4 are dedicated for R phase, switches S5, S6, S7, S8 for Y phase and switches S9, S10, S11, S12 are dedicated for B phase. For understanding the operation of proposed topology, let us consider Mode 1 where Vab is equals to 2V, Vbc equals to -3V and Vca equals to 1V. For obtaining mode 1, switches S2, S3, S6, S8, S9, S11 are in ON state whereas Switches S1, S4, S5, S7, S10, S12 are in OFF state. Similarly remaining modes can also be obtained by using the given switching pattern.

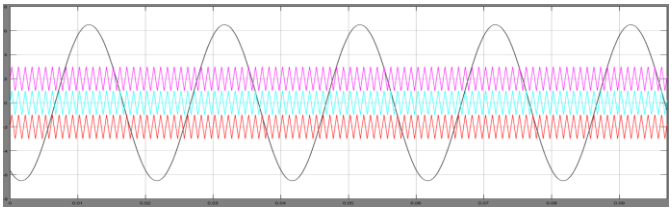
IV. CONTROL STRATEGY

In order to obtain desired switching pulse, level shifted multicarrier Pulse Width Modulation (PWM) technique is incorporated. Level shifted means all the carrier waves are displaced by DC offset value of desired magnitude. There are various methods of PWM techniques such as Phase Disposition (PD), Phase Opposition Disposition (POD), Alternate Phase Opposition Disposition (APOD) through which switching pulses can be obtained [15]. In PD technique, all the carrier waves are in same phase whereas in POD technique, carrier wave above zero has zero degree phase shift and carrier waves below zero are shifted by 180 degree. In APOD technique, adjacent carrier waves are phase shifted by 180 degree. In the proposed topology, level shifted PD technique is used which can be seen in Fig.7 (a), (b), (c). [16-17]

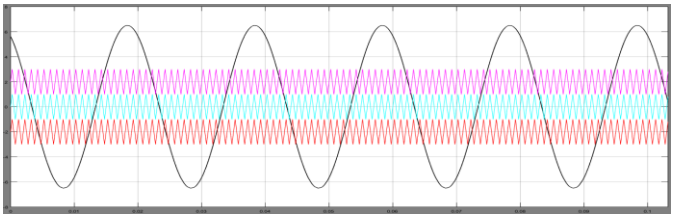
Here, the number of carrier waves can be calculated by using {(N-1)/2}, where N is the number of levels of output voltage waveform. For seven level output voltage waveform, only three carriers are required, whereas CHBMLI requires six carrier waves. Three reference sinusoidal waves are used which are shifted by 120 degrees to each other. By comparing sine wave with three carrier waves, three different pulse patterns are obtained. Now by using appropriate logic gate circuitry with these three pulses, final gate pulse for switches S1, S2, S3, S4 are generated for R phase. In the same way for Y phase i.e. for obtaining gate pulses for switches S5, S6, S7, S8, the same carrier waves are compared with second reference sine wave (120 degrees phase shifted). Similarly for B phase, it can be observed that the switches in each cell (S1 and S2) are complementary to each other. Similarly the pairs of switches S3 & S4, S5 & S6, S7 & S8, S9 & S10, S11 & S12 are complementary to each other.



(a) R phase



(b) Y phase



(c) B phase

Fig. 7 PD PWM techniques

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V. SIMULATION USING SIMU-LINK

The proposed topology is successfully simulated using Simu-link tool for no load, Resistive (R) load and Resistive-Inductive (RL) load using Metal Oxide Semiconductor Field Effect Transistor (MOSFET) as the switching device. Simulation circuit diagram for proposed topology is shown in Fig. 8, where R=10 ohm and L=15 mH has been chosen for simulation. Fig. 9 shows the three phase line to line output voltage waveform which is same for no load, R load and RL load conditions. Figs. 10 and 11 shows the three phase output current waveform for R load and RL Load respectively at 1 KHz carrier frequency.

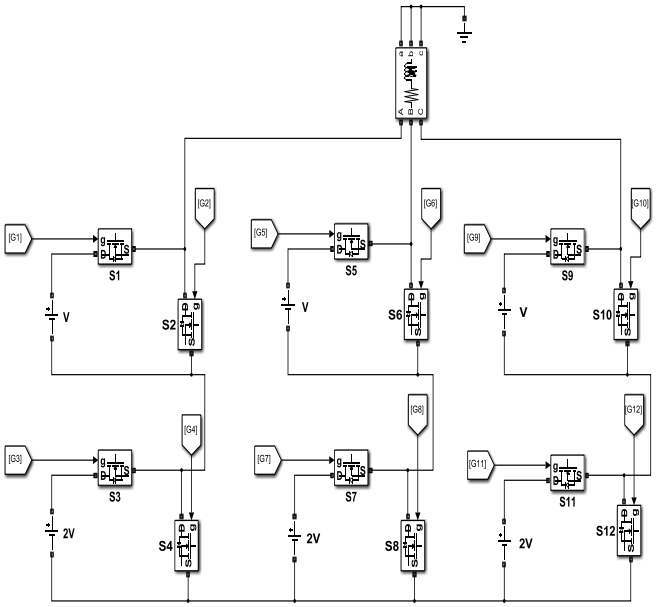

Fig. 8 Simulation circuit diagram for the proposed topology

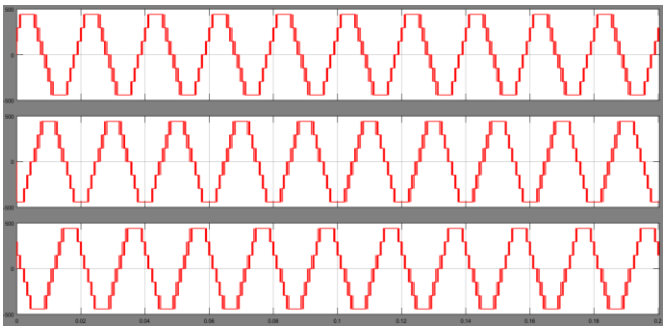

Fig. 9 Three phase output voltage waveforms (a) R phase (b) Y phase (c) B phase

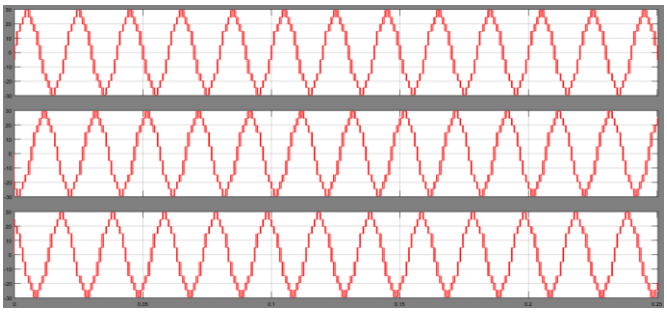

Fig.10 Three phase output current waveform for R Load

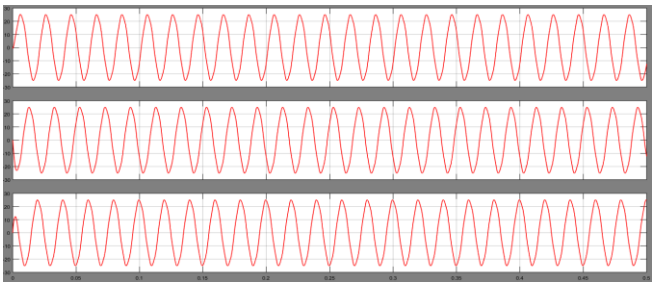

Fig.11 Three phase output current waveform for RL Load

VI. SIMULATION RESULTS

It can be observed from Fig. 12 that THD at 1 KHz carrier frequency for the voltage waveform at No load, R load and RL load is 15.11% whereas the THD for current waveform obtained is 4.64 (RL load) as shown in Fig.13. The comparison between CHBMLI and the proposed topology is shown in Table II.

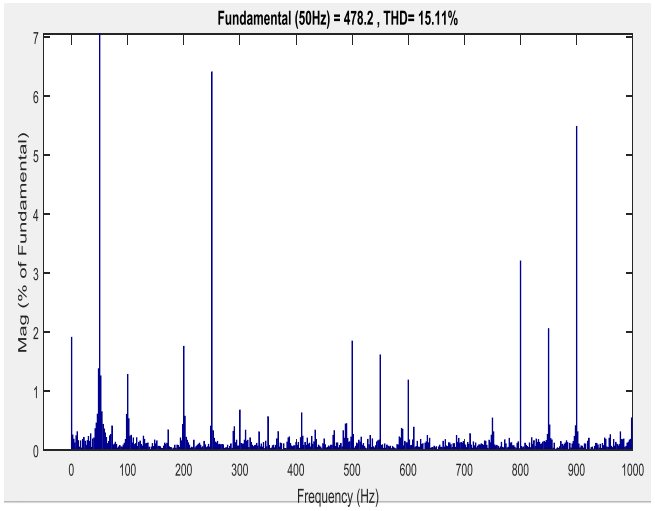

Fig.12 THD for voltage waveform at 1 KHz carrier frequency

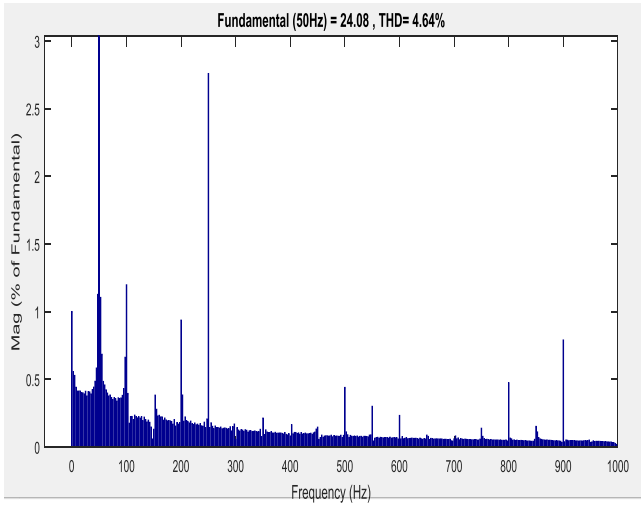

Fig.13 THD for Current waveform at 1 KHz carrier frequency

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TABLE II. COMPARISION BETWEEN CONVENTIONAL CHBMLI AND PROPOSED TOPOLOGY

Parameters	Conventional CHBMLI	Proposed Topology
No. of switches	36	12
No. of DC Sources	9	6
PWM Technique	PD	PD
THD in Voltage waveform (Any type of load)	18.28%	15.11%
THD in Current waveform (R-Load)	18.25%	15.33%
THD in Current waveform (RL-Load)	5.85%	4.64%
No. of carrier wave Required	6	3

VII. CONCLUSIONS

An asymmetric topology of three-phase Cascaded Multilevel Inverter has been developed with reduced number of switches and the associated gate driver circuits. With less number of switches and input DC sources, the proposed topology results in reduced installation area. Level shifted Phase Disposition PWM technique is successfully employed for different load conditions. The results with minimum THD in voltage waveform (any type of load) obtained was 15.11% at 1 KHz carrier frequency and minimum THD in current waveform (RL load) obtained was 4.64% at 1 KHz carrier frequency. Since only two DC sources are required per phase, hence, solar PV panels can also be used as input DC source in the proposed topology for the integration with renewable energy. Hence, the proposed topology poses great industrial, research and commercial applications with lesser harmonic content and better results. Furthermore, different modulation control strategies can also be implemented for opening new challenges in the field of multilevel inverter technology.

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