Thin Film Fabrication And Characterization Of Inkjet Printed Nano Silver (AG) Interconnects

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ABSTRACT:

This work has resulted a promising replacement element, nano silver to overcome the present day interconnect issue and to meet the future requirements of circuit fabrication. Initially precursor Solution, Silver Nitrate ($AgNO_3$), an environment friendly reducing agent tannic acid ($C_{76}H_{52}O_{46}$), and chemicals Carboxy Methyl Cellulose Sodium Salt ($C_8H_{16}NaO_8$), Sodium carbonate(Na_2CO_3) were all dissolved in appropriate volume of deionized water and these solutions were stirred for one hour protecting away from sunlight .The prepared solution was used as a conductive ink in a inkjet printer to draw interconnect pattern on the substrate. A thin film of nano silver Pattern remained on the substrate. SEM images and XRD analysis of thin film nano silver pattern were carried out and these patterns were characterized to prove its identity to find application as interconnect in ULSI technology.

Key words: Ag interconnects; Inkjet Printing; Moore's Law; Thin Film; ULSI.

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1. INTRODUCTION

In the world of digital fabrication, the race still continues between human expectation for better circuit performance and circuit scaling. To satisfy Moore's prediction law and work it for the future, fabrication technology has evolved from Small Scale Integration (SSI) to Ultra Large Scale Integration (ULSI).Yet after all these evolutions interconnect issues remain a crippling factor limiting the overall performance of the circuit. Present day VLSI fabrication technology uses copper element as interconnect which struggle to find a place in for the future scaling technologies. Interconnect, as the name describes is a medium to inter-connect two or more devices on a chip. The function of an interconnect is to distribute clock and other signals to the various functional blocks of a CMOS integrated circuit and is utilized like a metronome to coordinate actions of circuits [1,2].

These clock signals are particularly affected by technology scaling (Moore's law), in that long global interconnect lines become significantly more resistive as line dimensions are decreased. Finally, the control of any differences and uncertainty in the arrival times of the clock signals can severely limit the maximum performance of the entire system and create catastrophic race conditions in which an incorrect data signal may latch within a register. Novel structures are currently under development to ameliorate these issues and provide effective solutions [3-5].

Table No.1: shows the resistivity and conductivity of several materials.
The values are correct at 20 degrees Celsius.

Material	ρ (Ωm) at 20 °C Resistivity	σ (S/m) at 20 °C Conductivity
Silver	1.59×10^{-8}	6.30×10^{7}
Copper	1.68×10^{-8}	5.96×10^{7}
Gold	2.44×10^{-8}	4.10×10^{7}
Aluminum	2.82×10^{-8}	3.5×10^{7}
Zinc	5.90×10^{-8}	1.69×10^{7}
Nickel	6.99×10^{-8}	1.43×10^{7}
Iron	1.0×10^{-7}	1.00×10^{7}
Lead	2.2×10^{-7}	4.55×10^{6}

1.2 INTERCONNECT SOLUTION:

The 2012 reports from IRTS concludes that Cu and low-κ interconnects will probably represent the final "conventional" interconnect technology. And also concluded there are no metals with significantly lower resistivity than Cu. But it is eminent that Ag has significantly lower resistivity than Cu.

The most Critical Challenges faced at nanometer scaling and their respective issues is given in Table No.2.

Table No.2: Critical challenges and issues with interconnect design for future [6].

MOST CRITICAL CHALLENGES AT NANOMETER SCALING	SUMMARY OF ISSUES
Material Introduction of new materials to meet conductivity requirements	The rapid introductions of new materials/processes that are necessary to meet conductivity requirements create integration and material characterization challenges.
Manufacturable Integration Engineering manufacturable interconnect structures, processes and new materials	Integration complexity, CMP damage, resists poisoning, dielectric constant degradation. Lack of interconnect/packaging architecture design optimization tool
Reliability Achieving necessary reliability	New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling, and control of failure mechanisms will be key.
Cost & Yield for Manufacturability Manufacturability and defect management that meet overall cost/performance requirements	As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.

2. Materials and Experimentals:

2.1. Chemicals Used:

1. Silver nitrate ($AgNO_3$)
2. Tannic acid ($C_{76}H_{52}O_{46}$) and
3. Carboxy Methyl Cellulose Sodium Salt ($C_8H_{16}NaO_8$)
4. Sodium carbonate (Na_2CO_3)

2.2. Experimental procedure

Silver nano-particles were synthesized by reducing its precursor silver nitrate solution. 0.17% of Sliver nitrate ($AgNO_3$) solution dissolved in100ml of deionized water was mixed along with 0.1% of tannic acid dissolved 10ml of deionized water, similarly 0.1% of Carboxy Methyl Cellulose Sodium Salt dissolved in 10ml of deionized water, and 0.1% of Sodium carbonate dissolved in 10ml of de-ionized water. The mixture solution was stirred for one hour keeping it away from sunlight.

2.3. Printing and Pattern:

The prepared solution was used as an conductive ink and an interconnect pattern was drawn on the substrate using EPSON inkjet printer. The graphical structure of Interconnect patterns is shown below:

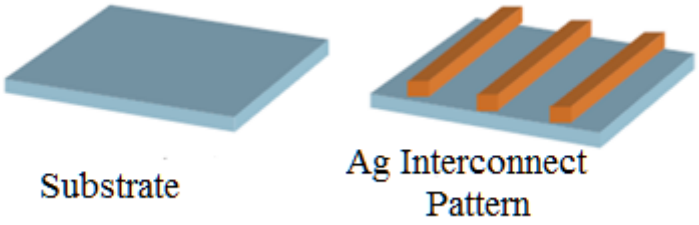

Figure No.1: Proposed Structure of Silver Interconnect Patterns on Flexible Substrate

3. RESULTS AND DISCUSSIONS:

3.1 SEM & XRD Analysis:

The SEM images of prepared silver nano-particles is shown below:

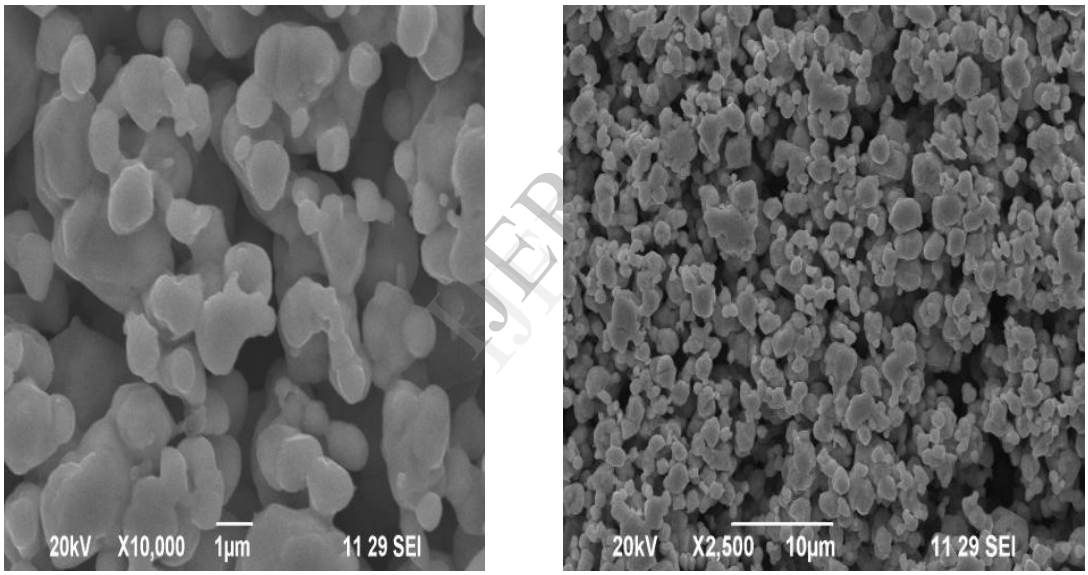

Figure No. 2: SEM image of Nano Silver

Silver Nano ink prepared was filtered using a filter paper dried and then the dried samples were analyzed using XRD analysis. The results of XRD confirm the formation of silver nanoparticles (Ag).

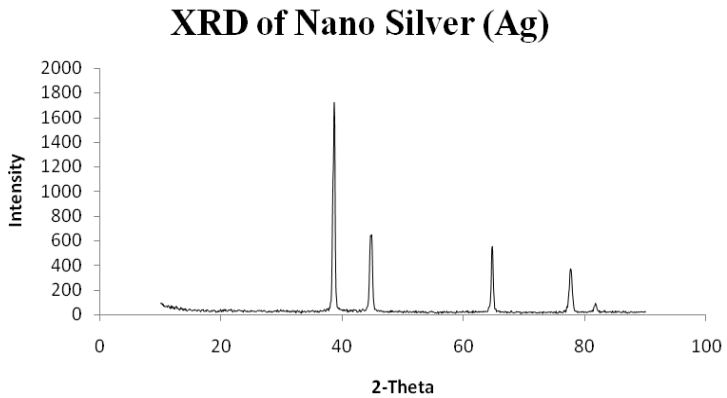

Figure No. 3: XRD plot of Nano Silver

The particle size (D) of the prepared Nano Silver was calculated using Scherrer's Formula and found to be in the range of 16nm to 28nm.

3.2 Characterization of Nano Silver Interconnects:

The VI characteristics of the interconnect lines are drawn with the help of NI Labview discrete components measurements.

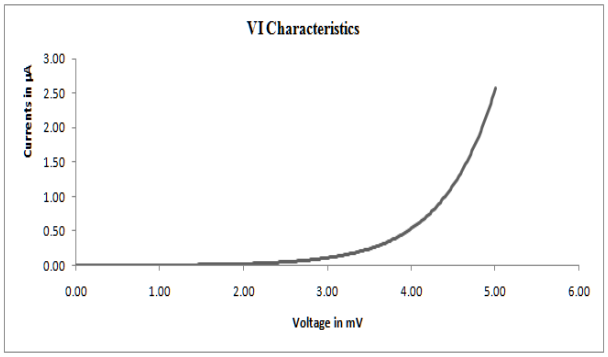

Figure No.4: VI characteristics of Nano Silver Interconnects

4. Conclusions:

The resistivity of the drawn Nano silver Interconnects, whose length is 1cm and width is 10µm, is found to be 0.0785µΩ.m at room temperature (30°C), which is proved to be much more conducting compared to an ordinary silver at 20°C. Hence, nano silver based interconnects can be used in IC chip replacing conventional Copper interconnects.

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