Thermal Aware Energy Efficient Content Addressable Memory Design on FPGA

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Abstract—In this work, we are going to integrate the thermalaware and energy efficient design approach in content addressable memories. During implementation on FPGA, we are going to test the thermal stability by operating this CAM design with different ambient temperature 25^0C, 35^0C, 45^0C, 55^0C, and 65^0C. We have shown the compatibility of our device with wireless network by operating it on different frequency ranges: 1GHz, 2.4 GHz, 3.6 GHz, 4.9 GHz, 5 GHz, 5.9 GHz, 60 GHz bands of WLAN channels. There is 69.38%, reduction in leakage power, when we scale down ambient temperature from 65^0C to 55^0 C, 45^0 C, 35^0 C, 25^0 C at 1 GHz. In this work, we are using 28nm technology based Kintex-7 FPGA and Verilog Hardware Description Language.

Keywords—Thermal Aware, Energy Efficient, FPGA, Content Addressable Memory.

I.   INTRODUCTION

Content Addressable Memory (CAM) is an application specific memory which allows us to search the content in the single clock cycle [1]. Content addressable memory is also known by the name associative memory, associative array [7] or associative storage [2]. Unlike the other computer memories that uses memory address for the reference of data word [6] stored at that particular address, Content addressable memory (CAM) is a special type of computer memory used in a very high speed searching applications in which user supply the data word and CAM searches the complete memory in order to find the data word in the memory.
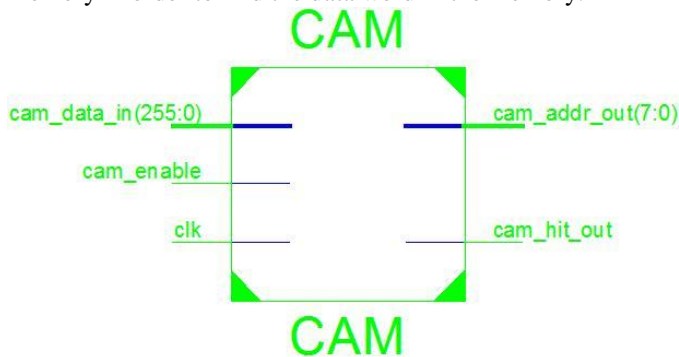

Fig. 1: Top Level Schematic of CAM

In Figure1, this CAM has three inputs and two outputs. If data word is found successfully, then CAM returns the complete list of addresses (Storage addresses) where the data word   was

found. Content Addressable Memory (CAM) was mainly designed to search the entire memory in single operation due to which it is much faster than the other memories (mainly RAM) used [2]. Kintex-7 is 28nm technology based FPGA.

Fig. 2: 28nm Technology Based Kintex-7 FPGA

Kintex-7 FPGA has maximum number of logic cells in compare to other 90nm technology based Virtex-4 FPGA, 65nm technology based Virtex-5 FPGA and 45nm technology based Spartan-6 FPGA. Kintex-7 FPGA has Block RAM, DSP Slices, PCI Gen2 Blocks, GTX Transceivers, I/O Pins as shown in Table 1. Random Access Memory (RAM) uses simple storage cells, On other hand CAM have its individual comparison circuit in order to identify a match between the i/p(input) bit and the stored bit. Also matched o/p (output) from individual cell in the data word should be combined to produce a complete data word match signal. Due to this extra circuitry area of Content addressable memory chip increases making manufacturing cost high .The parallel nature of CAM for searching in which huge amount of circuitry is active on every cycle make it more power consumptive [11].

TABLE 1: DEVICE RESOURCE AVAILABLE IN KINTEX- 7 FPGA

	XC7K70T	XC7K160T	XC7K325T
Logic Cells	65,600	126,240	326,080
BlockRAM (Kb)	4,860	11,700	16,020
DSP Slices	240	600	840
PCIe® Gen2 Blocks	1	1	1
GTX Transceivers (12.5 Gb/s Max Rate)	8	8	16
I/O Pins	300	400	500

Because of these disadvantages, CAM is only used in some special applications where the slow speed is not tolerable. Two types of CAM mainly used are Binary CAM and Ternary CAM [1]. Binary CAM simply uses data search words that contains 1s and 0s to perform the exact match, But in Ternary CAM there exists a third state known as ' Don't Care' or 'X' which make our searching more flexible. For e.g. Ternary CAM can have a stored word "X010X" which will match any of these words "10101", "10100", "00101", "00100". It makes our came more flexible but also increases the cost of it. Content addressable memory frequently in computer networking device (CND)[3]. For example, when a switchinghub (also known as network switch) receives data frame (DF) from any of the ports , internal table is updated with the DF's source MAC address [4] and port it was received on, it then looks for the destination's MAC address in the table to determine what port the frame needs to be forwarded to, and send it out on that port. MAC address table is mainly implemented using binary CAM (BCAM) so destination port can be found very quickly Ternary Cam (TCAM) are mainly used in routers [5].
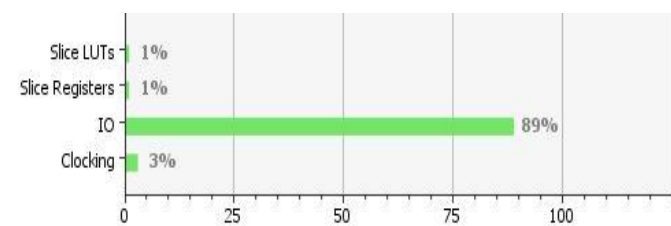

Fig. 3: Resource Utilization (%) of CAM on FPGA

When we are implementing CAM on Kintex-7 FPGA, then CAM is using 1% of slice LUTs, 1% of Slice Registers, 89% of IO and 3% of clocking available on Kintex-7 FPGA. With the use of TCAM in routing table, lookup process becomes very efficient [8]. The use of "don't care" to store the addresses for the host part of address make it easy and quick to look up the destination address in CAM for immediate retrieval of the correct routing entry; both comparison and masking are done by the Content addressable memory hardware [2]. Thermal aware is the demand of time, so we are operating CAM on different ambient temperatures: 25^0 C, 35^0C, 45^0C, 55^0C, and 65^0C. The design we are representing is compatible with Wireless network channels using IEEE 802.11 protocols at different frequency range from 2.4GHz to 60 GHz. W are using 298.15K in place of 25^0C and similarlywe are increasing degree Celsius by 273.15 and convert into Kelvin for thermal analysis.

TABLE 2: LIST OF WLAN 802.11 CHANNELS

WLAN Channels	Frequency (GHz)	Range and Specification
802.11b/g/n	2.4 GHz	2412-2484MHz
802.11y	3.6 GHz	3657.5-3692.5MHz
802.11a/h/j/n/ac	5 GHz	4915-5825MHz
802.11p	5.9 GHz	5850-5925MHz
802.11ad	60 GHz	WiGig

II. THERMAL ANALYSIS OF CAM

A. When CAM is Operating at 1 GHz Frequency

TABLE 3: POWER DISSIPATION AT DIFFERENT TEMPERATURE

Temperature→ Power↓	25^0 C	35^0 C	45^0 C	55^0 C	65^0 C
Clock	0.008	0.008	0.008	0.008	0.008
Logic	0.005	0.005	0.005	0.005	0.005
Signal	0.024	0.024	0.024	0.024	0.024
IO	0.028	0.028	0.028	0.028	0.028
Leakage	0.045	0.057	0.076	0.104	0.147
Total	0.11	0.122	0.141	0.169	0.211

There is 69.38%, reduction in leakage power, when we scale down ambient temperature from 65^0C to 55^0 C, 45^0 C, 35^0 C, 25^0 C at 1 GHz as shown in Figure 4 and Table 3.
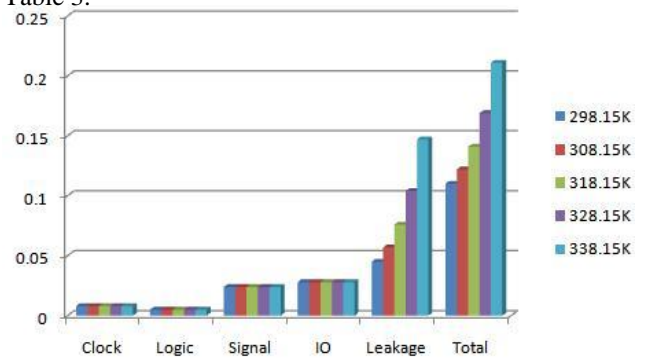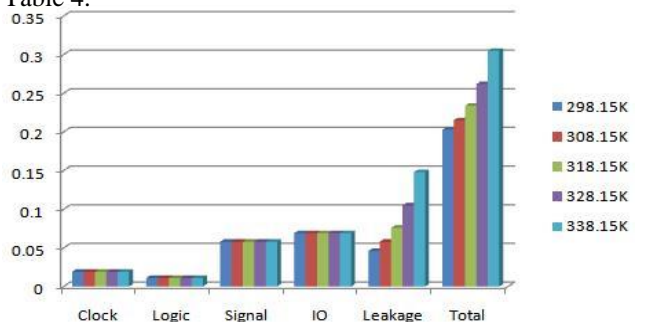

Fig. 4: Power Dissipation at 1GHz Frequency and Different Temperature

B. When CAM is Operating at 2.4 GHz Frequency

TABLE 4: POWER DISSIPATION AT DIFFERENT TEMPERATURE

Temperature→ Power↓	25^0 C	35^0 C	45^0 C	55^0 C	65^0 C
Clock	0.019	0.019	0.019	0.019	0.019
Logic	0.011	0.011	0.011	0.011	0.011
Signal	0.058	0.058	0.058	0.058	0.058
IO	0.069	0.069	0.069	0.069	0.069
Leakage	0.046	0.058	0.076	0.105	0.148
Total	0.203	0.215	0.234	0.262	0.305

There is 68.91%, reduction in leakage power, when we scale down ambient temperature from 65^0C to 55^0 C, 45^0 C, 35^0 C, 25^0 C at 2.4 GHz as shown in Figure 5 and Table 4.

Fig. 5: Power Dissipation at 2.4GHz Frequency and Different Temperature

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C. When CAM is Operating at 3.6 GHz Frequency

TABLE 5: POWER DISSIPATION AT DIFFERENT TEMPERATURE

Temperature→ Power↓	25^0 C	35^0 C	45^0 C	55^0 C	65^0 C
Clock	0.029	0.029	0.029	0.029	0.029
Logic	0.017	0.017	0.017	0.017	0.017
Signal	0.087	0.087	0.087	0.087	0.087
IO	0.104	0.104	0.104	0.104	0.104
Leakage	0.046	0.058	0.077	0.106	0.148
Total	0.283	0.295	0.314	0.343	0.385

There is 68.91%, reduction in leakage power, when we scale down ambient temperature from 65^0C to 55^0 C, 45^0 C, 35^0 C, 25^0 C at 3.6 GHz as shown in Figure 6 and Table 5.
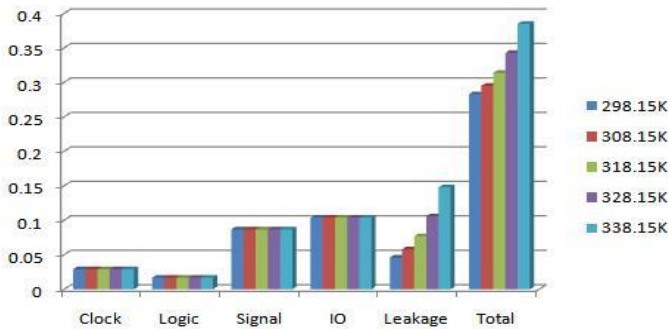

Fig, 6: Power Dissipation at 3.6GHz Frequency and Different Temperature

D. When CAM is Operating at 4.9 GHz Frequency

TABLE 6: POWER DISSIPATION AT DIFFERENT TEMPERATURE

Temperature→ Power↓	25^0 C	35^0 C	45^0 C	55^0 C	65^0 C
Clock	0.039	0.039	0.039	0.039	0.039
Logic	0.023	0.023	0.023	0.023	0.023
Signal	0.119	0.119	0.119	0.119	0.119
IO	0.142	0.142	0.142	0.142	0.142
Leakage	0.046	0.058	0.077	0.106	0.149
Total	0.369	0.381	0.400	0.429	0.473

There is 69.12%, reduction in leakage power, when we scale down ambient temperature from 65^0C to 55^0 C, 45^0 C, 35^0 C, 25^0 C at 4.9 GHz as shown in Figure 7 and Table 6.
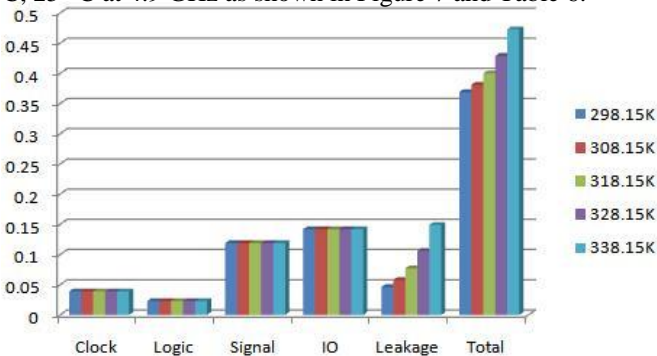

Fig. 7: Power Dissipation at 4.9GHz Frequency and Different Temperature

E. When CAM is Operating at 5 GHz Frequency.

TABLE 7: POWER DISSIPATION AT DIFFERENT TEMPERATURE

Temperature→ Power↓	25^0 C	35^0 C	45^0 C	55^0 C	65^0 C
Clock	0.040	0.040	0.040	0.040	0.040
Logic	0.023	0.023	0.023	0.023	0.023
Signal	0.121	0.121	0.121	0.121	0.121
IO	0.145	0.145	0.145	0.145	0.145
Leakage	0.046	0.058	0.077	0.106	0.149
Total	0.376	0.388	0.407	0.436	0.479

There is 69.12% reduction in leakage power, when we scale down ambient temperature from 65^0C to 55^0 C, 45^0 C, 35^0 C, 25^0 C at 5 GHz as shown in Figure 8 and Table 7.
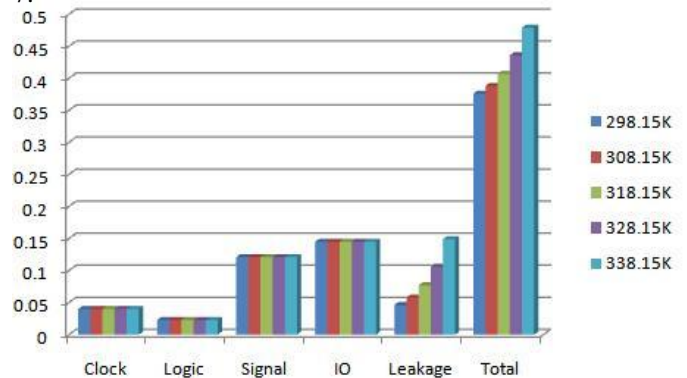

Fig. 8: Power Dissipation at 5GHz Frequency and Different Temperature

F. When CAM is Operating at 5.9 GHz Frequency

TABLE 8: POWER DISSIPATION AT DIFFERENT TEMPERATURE

Temperature→ Power↓	25^0 C	35^0 C	45^0 C	55^0 C	65^0 C
Clock	0.047	0.047	0.047	0.047	0.047
Logic	0.028	0.028	0.028	0.028	0.028
Signal	0.143	0.143	0.143	0.143	0.143
IO	0.172	0.172	0.172	0.172	0.172
Leakage	0.046	0.058	0.078	0.107	0.150
Total	0.436	0.448	0.467	0.496	0.540

There is 69.33%, reduction in leakage power, when we scale down ambient temperature from 65^0C to 55^0 C, 45^0 C, 35^0 C, 25^0 C at 5.9 GHz as shown in Figure 9 and Table 8.
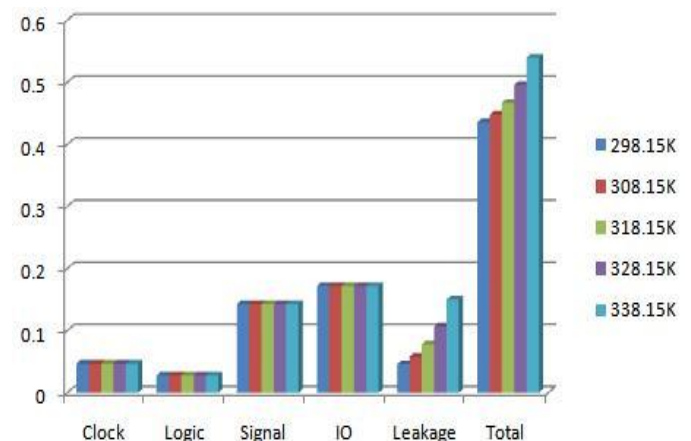

Fig. 9: Power dissipation at 5.9GHz Frequency and Different Temperature

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G. When CAM is operating at 60 GHz Frequency

TABLE 9: POWER DISSIPATION AT DIFFERENT TEMPERATURE

Temperature→ Power↓	25^0 C	35^0 C	45^0 C	55^0 C	65^0 C
Clock	0.482	0.482	0.482	0.482	0.482
Logic	0.111	0.111	0.111	0.111	0.111
Signal	1.325	1.325	1.325	1.325	1.325
IO	1.777	1.777	1.777	1.777	1.777
Leakage	0.054	0.070	0.096	0.134	0.190
Total	3.749	3.765	3.791	3.829	3.885

There is 71.57%, reduction in leakage power, when we scale down ambient temperature from 65^0C to 55^0 C, 45^0 C, 35^0 C, 25^0 C at 60 GHz as shown in Figure 10 and Table 9.
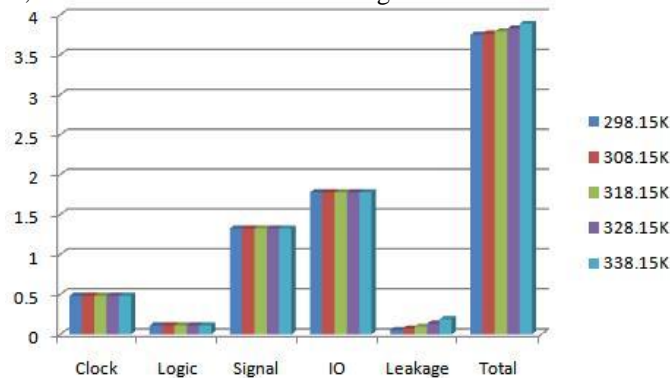

Fig. 10: Power Dissipation at 60GHz Frequency and Different Temperature

III.   CONCLUSION

We have achieved thermal aware energy efficient Content addressable memory on FPGA. We operated our device on different ambient temperatures and check for its working with Wireless network channels using IEEE 802.11 protocols at different frequency range from 1 GHz to 60 GHz. We have achieved an energy efficient CAM as we are getting 71-68% reduction in leakage power, when we scale down ambient temperature from 65^0C to 55^0 C, 45^0 C, 35^0 C, 25^0 C. Leakage power is directly proportional to temperature. Although, there is no reduction in Clock power, Logic power, Signal power, IO power but there is reduction in Total power.

IV.   FUTURE SCOPE

In future we will use content addressable memory with the concept of pervasive computing. We have used 2D IC in this paper but we will implement the design in future using 3D, 4D IC. We have implemented this CAM using 28 nm FPGA, but there is a large scope of implementing CAM on 14nm, 20nm, 32nm, 40nm, 90nm and large scale FPGA. This design is energy efficient but we can make it High Performance also. This design is implemented using Verilog. In future, we can also go for VHDL, System C, Embedded C, and C++ for high level synthesis.

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