International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 2 Issue 2, February- 2013

The Seventeen And Nineteen Level Asymmetrical Cascaded H-Bridge MLI With Minimum Number Of Switches As Their Input Of Photovoltaic Arrays With Grid Connection

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Abstract: **Nowadays, the non renewable energy sources are used compared with renewable energy sources, because day by day the non renewable energy sources are reduces. The main energy supplier of the worldwide economy is fossil fuel. This however has led to many problems such as global warming and air pollution. Therefore, with regard to the worldwide trend of green energy, solar power technology has become one of the most promising energy resources. The PV arrays produces DC voltage. But all electrical equipments operating with AC supply. The basic Inverter converts DC voltage to AC voltage. Inverter produces symmetrical square wave. The square wave contains infinite number of odd harmonics. So, these inverter output is used to electrical equipments, life of the electrical equipments reduces. Multilevel inverter produces various output voltage levels in a cycle. Multilevel inverter produces increase the voltage levels in the output voltage and corresponding THD value decreases in their increase output voltage levels. The PV arrays are connected to the as their input voltage of the Multilevel inverters. Multilevel inverters are two types of Cascaded H-bridge MLI. They are symmetrical and Asymmetrical cascaded H-bridge MLI. The existing system of symmetrical and asymmetrical Cascaded H-bridge MLI produces five, seven, nine level with 8 switches only and produces nine, eleven, thirteen, fifteen levels only operate with 12switches of asymmetrical Cascaded H-bridge MLI. The symmetrical and asymmetrical multilevel inverters are simulated with PV arrays in matlab/simulink. The THD analysis observed in the 5level to 15level of symmetrical asymmetrical multilevel inverters. The 17 level and 19 level output voltage produces with 32 and 36 switches in the symmetrical cascaded H-bridge configuration. But the proposed topology 17level and 19 level asymmetrical multilevel inverter operate with only 12 switches with PV arrays as their input sources with grid connection. The THD analysis observed in the17 level 19 level asymmetrical multilevel inverters.**

***Key words*: Multi level inverters, photovoltaic cells, harmonic analysis, Total Harmonic Distortion (THD).**

I.INTRODUCTION

A renewable energy application such as photovoltaic (PV) system has been widely used for a few decades since PV energy is free, abundant and distributed throughout the earth[1-3]. As a short introduction on the general development and forecast of world market in the photovoltaic's (PV) are presented. The general classification introduces grid connected, stand alone, large scale and roof-top PV-systems [4]. The core of presentation concentrates on the Development and trends of converters for grid connected PV-systems. The renewable energy sources are consists of fuel cell, photovoltaic cells, wind turbines, micro turbines and so on etc. but photovoltaic cells are most popularly used [5-9]. So the photo voltaic cells are producing the dc source. These dc source give to inverter. The inverter converts dc to ac power. But the inverter produces square wave ac. The square wave contains infinite number of harmonics are presented. The multilevel inverter means the level refers to the various voltage values in a cycle. The multilevel inverter output levels increase near to the sine wave shape formed. Then the number of harmonic content reduced in the output of the multilevel inverter output. The multilevel inverter are three types. They are

1.Diode clamped multilevel inverter
2.Flying capacitor multilevel inverter
3.Cascaded H-bridge multilevel inverter

The objective of this paper cascaded H-bridge inverter are symmetrical and asymmetrical multilevel inverters are used with Photovoltaic arrays in matlab/simulink. The asymmetrical multilevel inverters are used the number of switches are reduced, cost reduces, complexity, place requirement reduces compared with symmetrical multilevel inverters. The asymmetrical multilevel inverters have 5level to 15 level THD analysis are observed with photovoltaic arrays are given. The 17 level and 19 level output voltage produced only from 12 switches. The 17 and 19 level asymmetrical multilevel inverter (MLI) with grid connection.

II. PHOTO VOLTAIC SYSTEMS

A photovoltaic system directly converts sunlight into electricity. The basic device of a PV system is the PV cell. Cells may be grouped to from panels or arrays. The voltage and current available at the terminals of a PV device may directly feed small loads such as lighting systems and DC motors. A photovoltaic cell is basically a semiconductor diode whose p-n junction is exposed to light. Photovoltaic cells are made of several types of semiconductors using different manufacturing processes. The incidence of light on the cell generates charge carriers that originate an electric current if the cell is short-circuited.

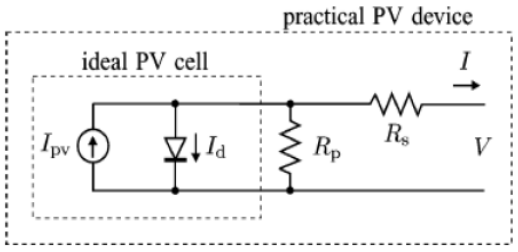

Fig.1 Equivalent cirucuit of a PV device including the Series and Parallel Resistances.

The equivalent circuit of PV cell is shown in Figure 1. In the above diagram the PV cell is represented by a current source in parallel with diode. $R_s$andR_p represent series and parallel resistance respectively. The output current and voltage from PV cell are represented by I and V.

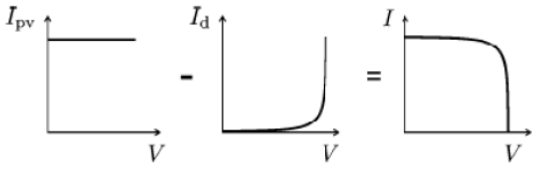

Fig.2 Characteristic I-V curve of the PV cell

The I-V characteristics of PV cell[7] is shown in Figure 2. The net cell current I is composed of the light-generated current $I_{PV}$and diode current I_d.

$$I = I_{PV} - I_d \qquad (1)$$

Where

$I_d = I_0 \exp(qV/akT)$

I_0 = leakage current of the diode

q=electron charge

k=Bolzmann constant

T=temperature of pn junction

a=diode ideality constant

The basic equation (1) of PV cell does not represent the *I-V*characteristic of a practical PV array. Practical array are composed of several connected PV cells and the observation of the characteristics at the terminals of the PV array requires the inclusion of additional parameters to the basic equation.

$$I = I_{PV} - \left[exp\left(V + \frac{R_s I}{V_t a}\right) - 1\right] - \frac{V + R_s I}{R_p} \qquad (2)$$

Where

$V_t = N_s kT/q$s is the thermal voltage of the array with N_s cells connected in series. Cells connected in parallel increase the current and cells connected in series provide greater output voltages. The I-V characteristics of a practical PV cell with maximum power point (MPP), short circuit current (Isc) and open circuit voltage (Voc) is shown in Figure 3. The MPP represents the point at which maximum power is obtained.

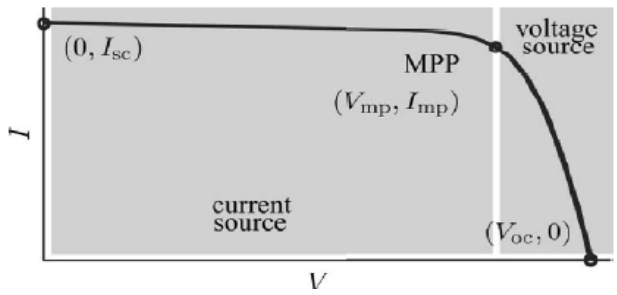

Fig.3 I-V Characteristic of the practical PV cell

Vmp and Imp are voltage and current at MPP respectively. The output from PV cell is not the same throughout the day; it varies with varying temperature and insolation (amount of radiation). Hence with varying teperature and insolation maximum power shourld be tracked so as to achieve the efficient operation of PV system.

III. CASACADED H BRIDGE INVERTER

3.1 Symmetrical Cascaded H Bridge (CHB) Inverter :

The Cascaded H Bridge (CHB) multilevel converters are simply a number of conventional two-level bridges, whose AC terminals are simply connected in series to synthesize the output waveforms. Figure 5 shows the power circuit for a symmetrical five-level inverter with two cascaded cells. The CHB inverter needs several independent DC sources which may be obtained from batteries, PV arrays or fuel cells. Through different combinations of the four switches of each cell, each converter level can generate three different voltage outputs, +Vdc,0,-Vdc. The AC output is the sum of the individual converter outputs. The number of output phase voltage levels is defined by n=2N+1, where N is the number of DC sources. For instance the output phase voltage swings from -2Vdc to +2Vdc with five levels.

$$I = I_{PV} - I_d$$

3.2 Asymmetrical Cascaded H Bridge (CHB) Inverter:

The above discussed H Bridge inverter topology is known as symmetrical CHB inverter topology is known as symmetric CHB inverter in which H bridges are fed by separate DC sources having same magnitude. An asymmetrical multilevel inverter shown in Figure 5 can be defined as a multilevel converter fed by a set of DC voltage source where at least one of them is different to the other one. The main advantage of asymmetrical multi level converter is, it uses less number of semiconductor switches compared with symmetrical topology. One interest of the asymmetrical configurations is that the number of levels is higher with the same number of cells. The number of levels is higher with the same number of cells in the symmetrical case, whereas it grows exponentially, in the asymmetrical case, the asymmetrical topology requires only twelve switches to obtain 7,9,11,13,15 level output voltage. whereas in case of symmetrical topology 12,16,20,24,28 switches are needed.

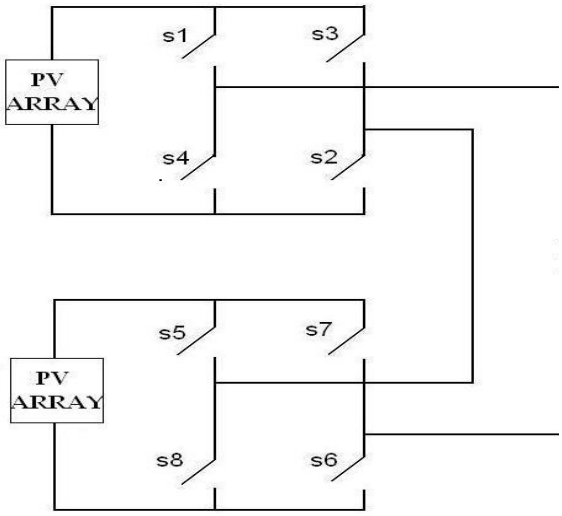

Fig. 4 Symmetrical Cascaded H-bridge multilevel inverter to get five level output voltage and Asymmetric Cascaded H-bridge inverter with seven, nine level with PV arrays as their input source

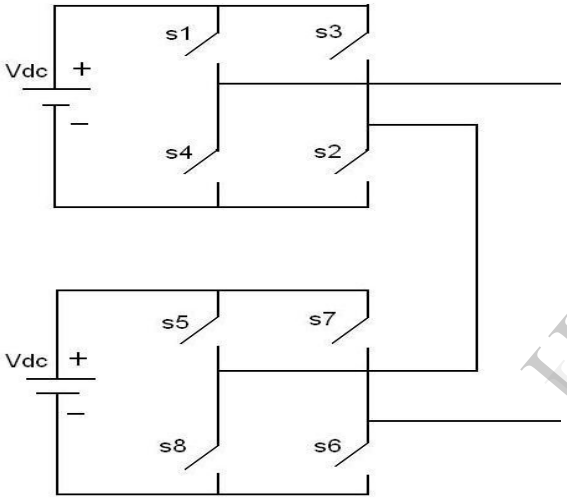

Fig. 5Symmetrical Cascaded H-bridge multilevel inverter to get five level output voltage and Asymmetric Cascaded H-bridge inverter with seven, nine level with DC sources as their input source

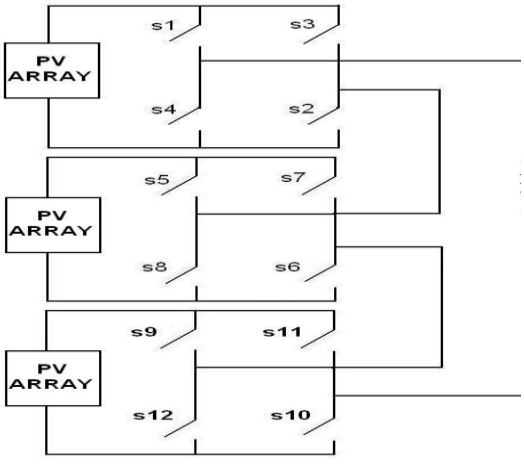

Fig. 6Asymmetrical Cascaded H-bridge multilevel inverter to get seven, nine, eleven, thirteen, fifteen level output voltage with PV arrays as their input source

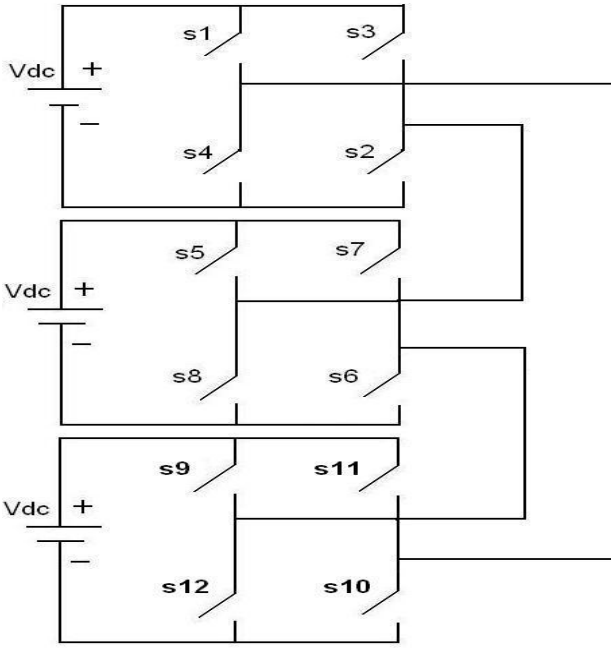

Fig.7Symmetrical Cascaded H-bridge multilevel inverter to get seven level and Asymmetric Cascaded H-bridge multilevel inverter to get nine, eleven, thirteen, fifteen level output voltage with DC sources as their input source

3.3 Proposed topology of single phase 17 and 19 level Asymmetrical Cascaded H Bridge (CHB) Inverter:

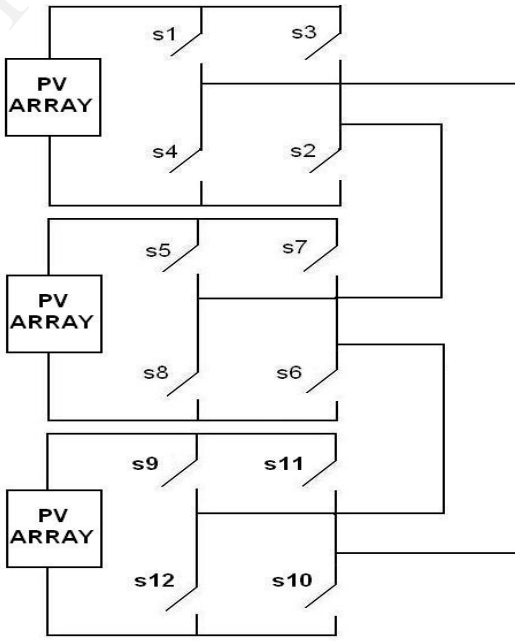

Fig.8Asymmetrical Cascaded H-bridge inverter to get seventeen, nineteen level output voltage

The proposed topology of single phase 17 and 19 level output voltage produced from 12 switches only. The other proposed topology is three phase 17 level and 19 level asymmetrical multilevel inverter

IV.MATLAB/SIMULATION RESULTS

4.1Symmetrical Cascaded H-bridge five level and Asymmetrical Cascaded H-bridge seven, nine level multilevel inverter:

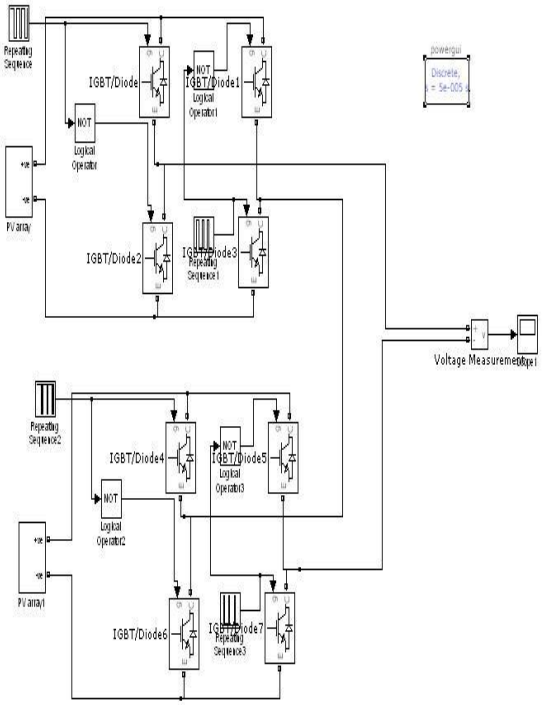

Fig. 10 Symmetrical Cascaded H-brige five level and Asymmetrical seven, nine level multilevel inverter simultation diagram

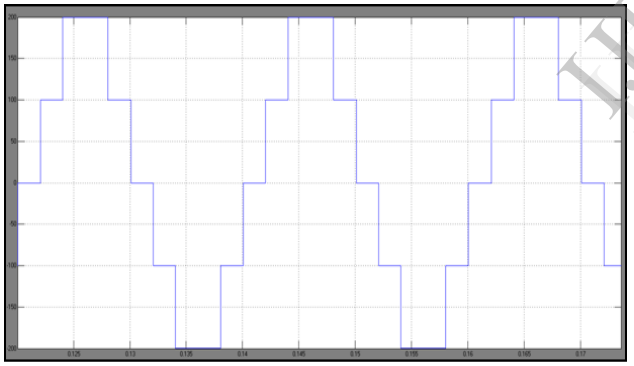

Fig.11 shows the symmetrical cascaded H-bridge five level multilevel inverter output voltage

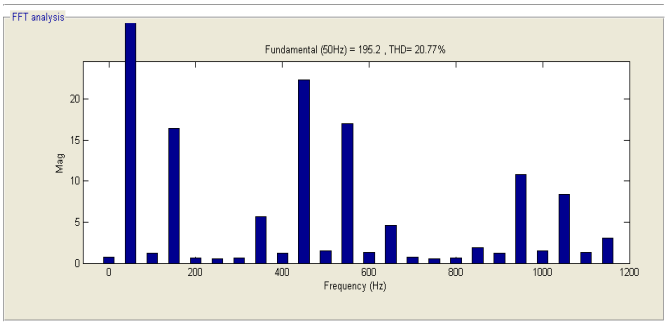

Fig.12 THD value of the symmetrical cascaded H-bridge five level multilevel inverter using FFT analysis

4.2Asymmetrical Cascaded H-bridge seven level multilevel inverter:

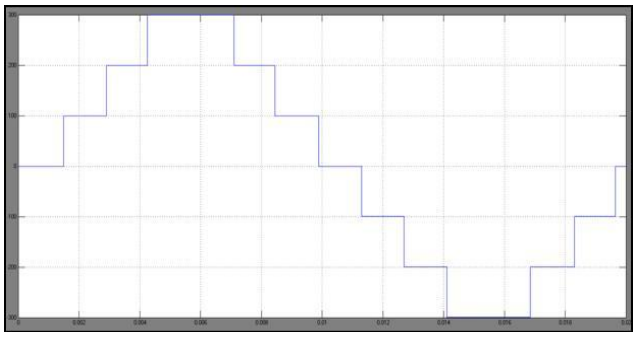

Fig.13 seven level mulitlevel Inverter output voltage

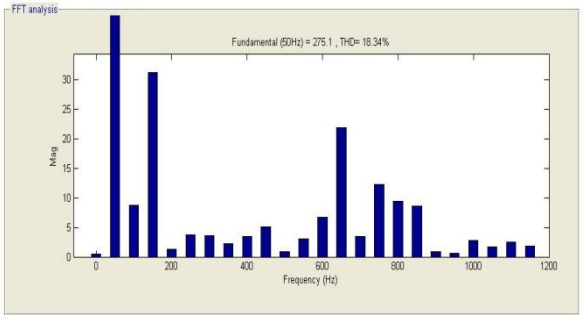

Fig.14 THD value of the seven level Asymmetrical cascaded H-bridge multilevel inverter using FFT analysis

4.3 Symmetrical cascaded H-bridge seven level and Asymmetrical Cascaded H-bridge nine, eleven, thirteen level multilevel inverter:

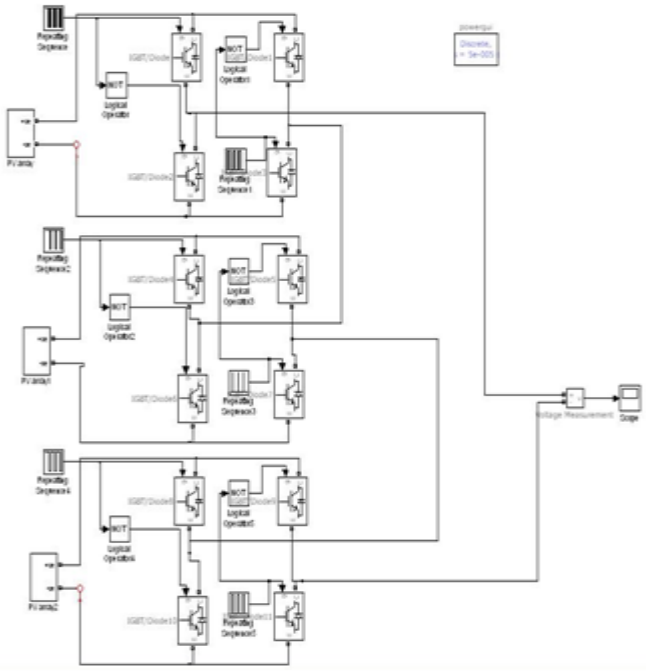

Fig.15 Symmetircal Cascaded H-bridge seven and Asymmetrical Cascaded H-brige multilevel inverter to get nine,eleven,thirteen,fifteen level multilevel inverter simultaiton diagram

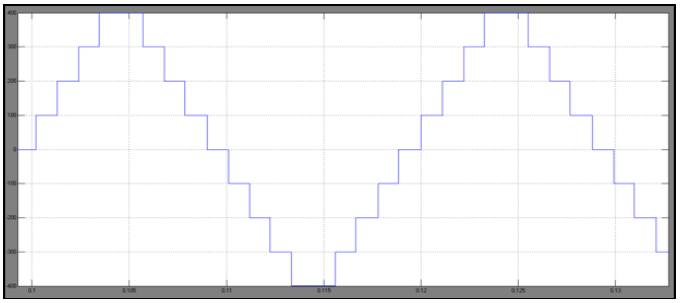

Fig.16 shows the Asymmetrical cascaded H-bridge nine level multilevel inverter output voltage

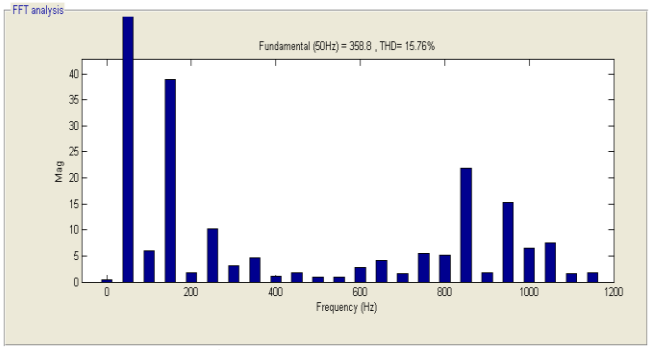

Fig.17 THD value of the nine level asymmetrical cascaded H-bridge multilevel inverter using FFT analysis

4.4 Asymmetrical Cascaded H-bridge eleven level multilevel inverter:

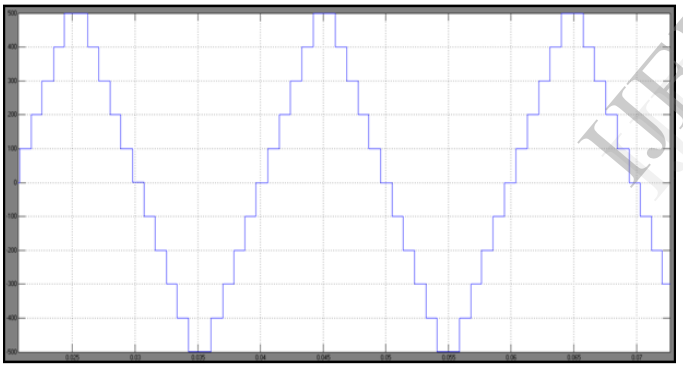

Fig.18 shows the asymmetrical cascaded H-bridge eleven level multilevel inverter output voltage

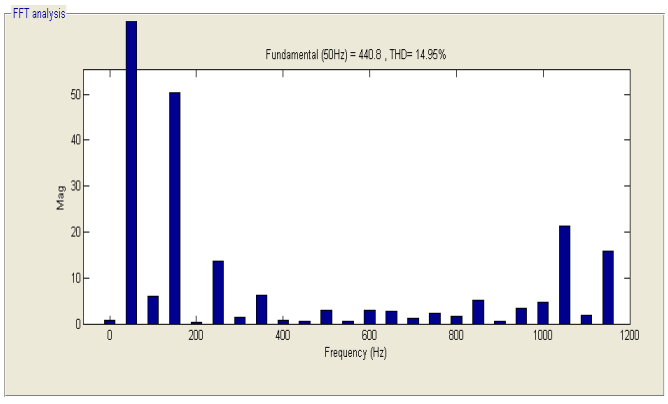

Fig.19 THD value of the eleven level asymmetrical cascaded H-bridge multilevel inverter using FFT analysis

4.4 Asymmetrical Cascaded H-bridge thirteen level multilevel inverter:

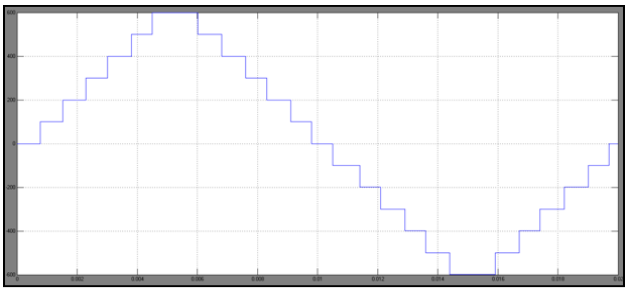

Fig.20 shows the asymmetrical cascaded H-bridge thirteen level multilevel inverter output voltage

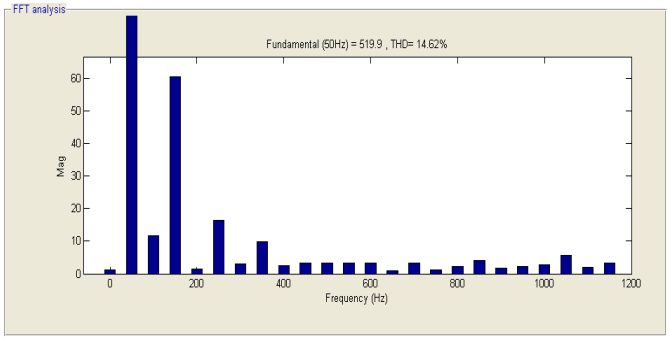

Fig.21 THD value of the thirteen level asymmetrical cascaded H-bridge multilevel inverter using FFT analysis

4.5 Asymmetrical Cascaded H-bridge fifteen level multilevel inverter:

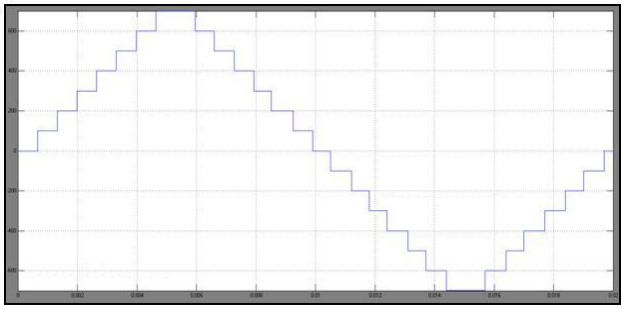

Fig.22 shows the asymmetrical cascaded H-bridge fifteen level multilevel inverter output voltage

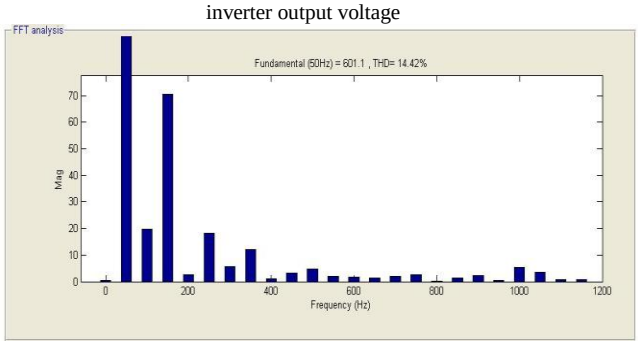

Fig.23 THD value of the fifteen level asymmetrical cascaded H-bridge multilevel inverter using FFT analysis

TABLE-I
PERFORMANCE COMPARSION OF DIFFEERNT LEVELS OF CHB INVERTER

Levels		DC1 Vin1	DC2 Vin2	DC3 Vin3	Output Voltage in Volts	No. of switches
5		Vin1	Vin1	-	2Vin1	8
7		Vin1	2Vin1	-	3Vin1	8
9	Type1	Vin1	3Vin1	-	4Vin1	8
	Type2	Vin1	Vin1	2Vin1	4Vin1	12
11	Type1	Vin1	Vin1	3Vin1	5Vin1	12
	Type2	Vin1	2Vin1	2Vin1	5Vin1	12
13	Type1	Vin1	Vin1	4Vin1	6Vin1	12
	Type2	Vin1	2Vin1	3Vin1	6Vin1	12
15	Type1	Vin1	Vin1	5Vin1	7Vin1	12
	Type2	Vin1	2Vin1	4Vin1	7Vin1	12

TABLE-II
HARMONICS IN VARIOUS SYMMETRICAL AND ASYMMETRICAL CASCADED H-BRIDGE MULTILEVEL INVERTERS

F1 & Harmonic Content	Number of levels					
	5level	7level	9level	11level	13level	15level
F1	195.2	275.05	358.75	440.08	520.96	601.09
3^{rd}	16.21	31.31	13.99	50.46	61.05	70.63
5^{th}	0.50	3.59	10.21	13.72	17.24	18.22
7^{th}	5.70	2.21	4.65	6.31	9.78	12.18
9^{th}	22.38	5.11	1.86	0.65	2.36	3.26
11^{th}	16.98	2.99	0.99	0.57	3.11	2.05
13^{th}	4.48	21.92	4.22	2.74	0.76	1.45
15^{th}	0.50	12.21	5.49	2.37	1.89	2.52
THD(%)	20.77	18.34	15.76	14.95	14.68	14.42

The various level output voltage levels consists of 5level to 15 level of symmetrical and asymmetrical multilevel inverter. The 5level to 15 level output voltage level contains harmonic content table as shown below table-II.

The Asymmetrical cascaded H-bridge MLI produces seven, nine, eleven, thirteen, fifteen level output voltage with twelve switches only. The THD value reduces according to the increase the output voltage levels from five, seven, nine, eleven, thirteen and fifteen levels. So we used in the asymmetrical configuration the reduced number of switches and cost of switches, area required and complexity reduces.

4.6 Proposed topology Asymmetrical Cascaded H-bridge Seventeen and Nineteen level multilevel inverter with grid connection:

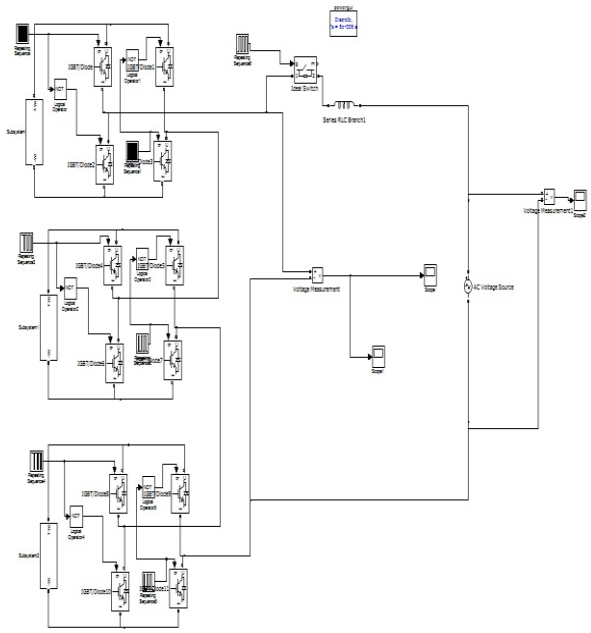

Fig.25Asymmetircal Cascaded H-bridge seventeen and ninteen level multilevel inverter with grid connecion of simultaiton diagram

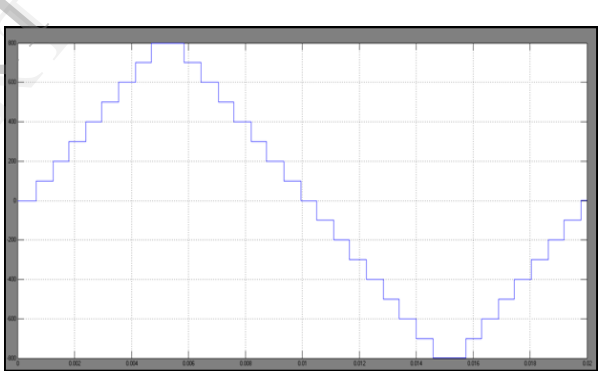

Fig.26 shows the asymmetrical cascaded H-bridge seventeen level multilevel inverter output voltage

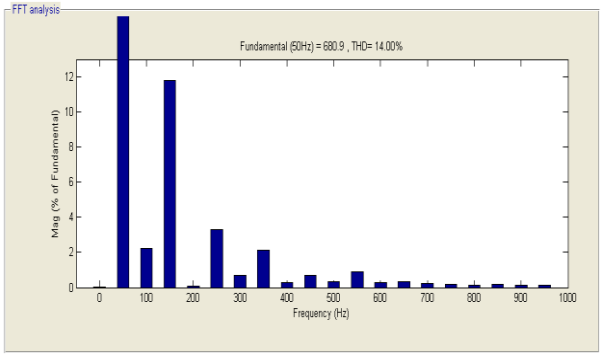

Fig.27 THD value of the seventeen level asymmetrical cascaded H-bridge multilevel inverter using FFT analysis

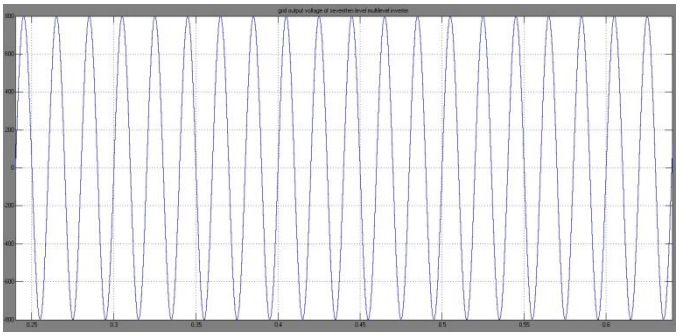

Fig.28 shows the asymmetrical cascaded H-bridge seventeen level multilevel inverter with grid connected of pure sine wave output voltage

4.7 Proposed topology of Asymmetrical Cascaded H-bridge nineteen level multilevel inverter:

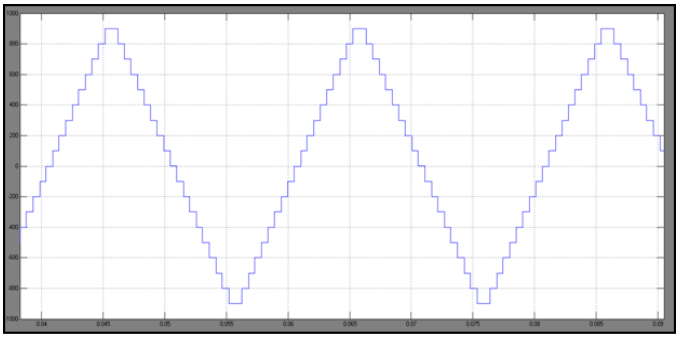

Fig.29 shows the asymmetrical Cascaded H-bridge nineteen level multilevel inverter output voltage

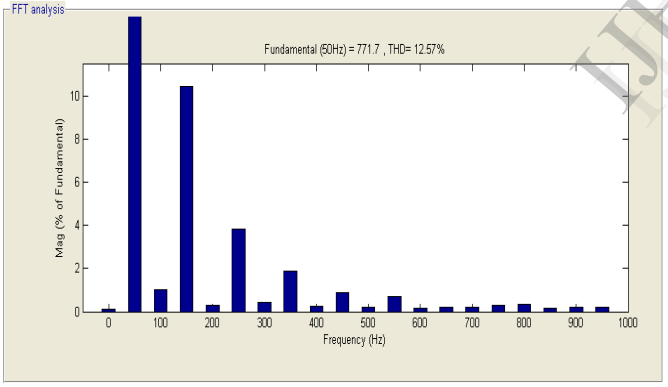

Fig.30 THD value of the nineteen level asymmetrical cascaded H-bridge multilevel inverter using FFT analysis

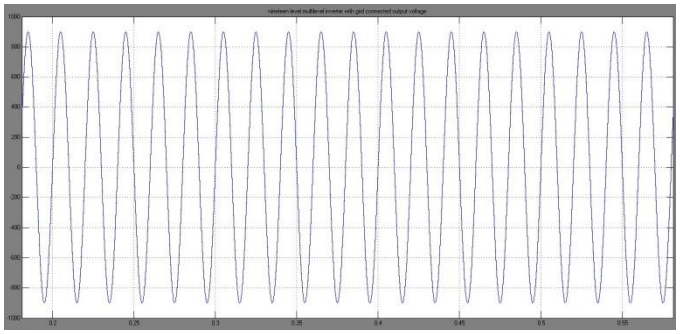

Fig.31 shows the asymmetrical cascaded H-bridge nineteen level multilevel inverter with grid connected of pure sine wave output voltage

TABLE-III
PERFORMANCE COMPARSION OF DIFFEERNT LEVELS OF CHB INVERTER

Levels	DC1 Vin1	DC2 Vin2	DC3 Vin3	Output Voltage in Volts	No. of swtiches
17	Vin1	3Vin1	4Vin1	8Vin1	12
19	Vin1	3Vin1	5Vin1	9Vin1	12

TABLE-IV
HARMONICS IN VARIOUS SYMMETRICAL AND ASYMMETRICAL CASCADED H-BRIDGE MULTILEVEL INVERTERS

F1 and harmonic content	Number of levels	
	17level	19level
Fundamental (F1)	680.89	771.87
3rd	80.4	80.90
5th	22.58	29.64
7th	14.54	14.39
9th	4.86	6.66
11th	6.01	5.59
13th	2.13	1.59
15th	1.27	2.19
THD(%)	14.00	12.57

The proposed topology of seventeen and nineteen level output voltage levels with 12 switches only in the asymmetrical configuration compared to symmetrical configuration of 32 and 36 switches produces seventeen and nineteen level output voltage. So, reduced number of switches, cost of switches and area required and also complexity reduces. In Table III, the input voltages as their input of seventeen and nineteen level multilevel inverters. The seventeen and nineteen asymmetrical multilevel inverter output voltage have THD as shown in Table-IV. The seventeen and nineteen level asymmetrical multilevel inverter with grid connection. The asymmetrical multilevel inverter to reduce the number of switches and cost also reduces. The complexity and place requirement and control circuit reduces and also switching losses also reduces compared to the symmetrical cascaded H-bridge multilevel inverters.

V.CONCLUSION

The Symmetrical MLIs are increases the number of voltage levels and corresponding number of switches increases. So, the cost of switches, area required, control circuit and complexity increases. In the asymmetrical configuration is seven, nine, eleven, thirteen, fifteen level output voltage operated with `12switches only. The proposed topology is seventeen and nineteen level output voltage with 12 switches only in the asymmetrical configuration. The seventeen and nineteen level asymmetrical multilevel inverter is connected with grid connection. Totally the asymmetrical cascaded H-bridge multilevel inverters to get the 7level to 19 level output voltage. The THD decreases to increase the number of levels, some lower or higher harmonic contents remain dominant in each level. These will be more dangerous induction drives. Hence the future work may be focus on implementing closed loop control with suitable harmonic

elimination technique to achieve better performance of the converter. The future scope is to determine the pwm techniques of asymmetrical multilevel inverters then to reduce the harmonic content in the output voltage of the asymmetrical multilevel inverters.

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