The design of high performance Barrel Integer Adder

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Abstract: **This paper presents the design of high performance barrel integer adder with less area and high speed with the help of parallel integer addition algorithm on the basis of researching the structure of half adder and D-flip-flops.It also elaborates the principle and structure of barrel integer addition algorithm, analyses the time and the degree of complexity in the area of the algorithm and at the same time compares it with the traditional integer addition algorithm. We realized that the 16-bit barrel integer adder using Verilog HDL and verifies comprehensively in the Altera device.The result shows that the speed of the barrelinteger adder designed in this paper improvesthe multiplier performance.**

I INTRODUCTION

Arithmetic Logic Unit (ALU), a very important part of microprocessor chip, can not only complete the arithmetic operation but also the logic operation . However, all the basic arithmetic operations (subtraction, multiplication, division) can eventually be reduced to the addition operation, so the realization of the addition operation is particularly important. In order to reduce the time of binary transmission and improve the speed of computing, people have designed various types of adders and raised a lot of methods to achieve adders, such as ripple carry adders, fast ripple carry adders, super-head carry adders, etc. The adders mentioned above are all of the parallel ones. In addition, there is also a kind of serial adder, which on the one hand has the advantages of less resources and flexible designs, etc; on the other hand, affects the speed of serial carry adder because of the gradual carry.

II.HALF ADDER

The half adder adds two one-bit binary numbers A and B. It has two outputs, S and C (the value theoretically carried on to the next addition); the final sum is 2C+ S. The simplest half-adder design, pictured on the right, incorporates an XOR gate for S and an AND gate for C. With the addition of an OR gate to combine their carry outputs, two half adders can be combined to make a full adder

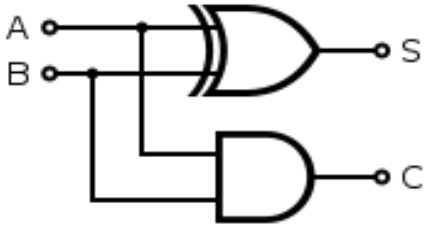

Figure 1: Half adder

Equations:

S=A^B

C=A&B

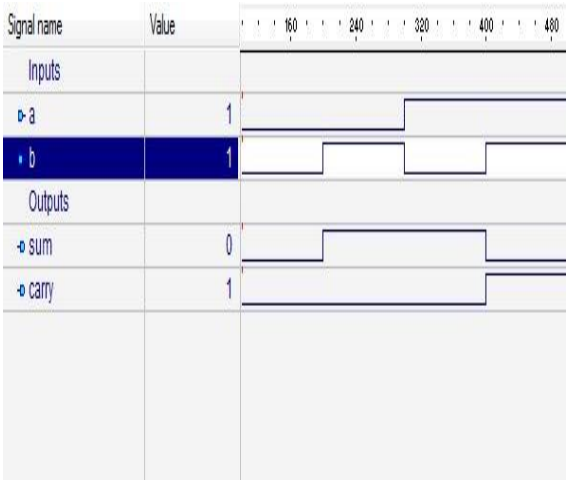

Figure 2: half adder wave form

III.D-FLIP-FLOP

The flip-flop above made of two NAND-gates is a very simple one. In time manufacturers have made more sophisticated ones. An example is the 7474, a so called D-flip-flop.

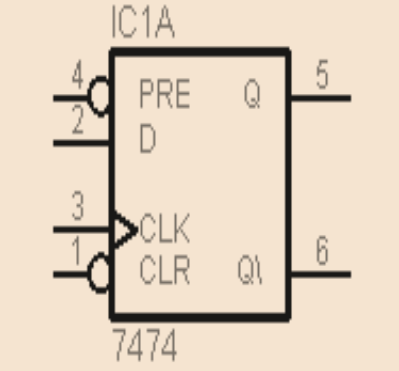

Figure 3: D_flip-flop

D (for Data) is an input. The moment the level on input CLK (for CLocK) goes from (L) to (H), ">" means "positive edge", the value of Data is copied to output Q. Output Q\ (another way to write Q with a "_" on top) becomes the opposite of Q. Changing the Data has no further influence on the outputs as long as Clock does not go from (L)to(H).Negating Preset causes Q to go (H) and Q\ to go (L) at any time. Negating Reset causes Q to go (L) and Q\ to go (H) at any time.Negating both these inputs causes unpredictable results.

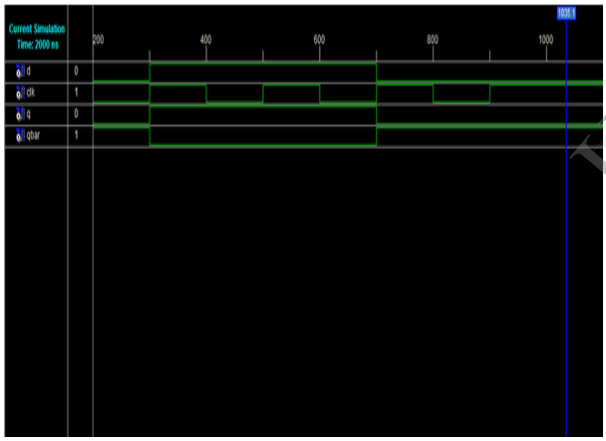

Figure 4: waveforms of D-flip flop

IV .THE PRINCIPLE OF BARREL INTEGER ADDITION ALGORITHM

Barrel Integer Addition Algorithm is a kind of parallel one based on the half-adder, of which basic principles are as follows: Suppose addend A and summand B are two binary numbers with n bits, using superscripts for time variables and subscripts for binary bits, while *Ak*□*Bk* are considered as the completion of the *k* meeting of iteration by A and B, that is:

$$A^k = A^k_{n+1} A^k_n A^k_{n-1} \cdots A^k_i \cdots A^k_3 A^k_2 A^k_1 ,$$

$$B^k = B^k_{n+1} B^k_n B^k_{n-1} \cdots B^k_i \cdots B^k_3 B^k_2 B^k_1 ,$$

k=0, 1, 2……..

The highest A^k_{n+1}, B^k_{n+1} are the carry bits added to the carries, there are $A^0_{n+1}=0$, $\mathbf{B}^0_{n+1}=0$. Obviously:

$$A = A^0 = A^0_{n+1} A^0_n A^0_{n-1} \cdots A^0_i \cdots A^0_3 A^0_2 A^0_1 ,$$

$$B = B^0 = B^0_{n+1} B^0_n B^0_{n-1} \cdots B^0_i \cdots B^0_3 B^0_2 B^0_1$$

are the initial number of iteration. The iterative formula of half-adder is defined as:

$$S^k_i = A^{k-1}_i \oplus B^{k-1}_i ,$$

$$C^k_i = A^{k-1}_i \cdot B^{k-1}_i ,$$

$$i = 1,2,3,\cdots,n+1 ; \quad k = 1,2,\cdots .$$

the equation (1) is the addition, while equation (2) is the carry; order

$$A^k_i = S^k_i ,$$

$$B^k_1 = C^k_{n+1}, B^k_i = C^k_{i-}$$

i=1,2,3⋯⋯n;k=1,2,3⋯

a new set of summands and additions can be obtained.

$$A^k = A^k_{n+1} A^k_n A^k_{n-1} \cdots A^k_i \cdots A^k_3 A^k_2 A^k_1$$

$$B^k = B^k_{n+1} B^k_n B^k_{n-1} \cdots B^k_i \cdots B^k_3 B^k_2 B^k_1$$

$$k = 1,2,\cdots .$$

It can prove that $C^k=0$, then

$$A + B = A^k = S .$$

The structure of Barrel Integer Adder is shown in Figure 5, where HA represents the half-adder, D the flip-flop, *i C* the control terminal of flip-flop. The Barrel adder is referred to CBA (Carry Barrel Adder) for short.

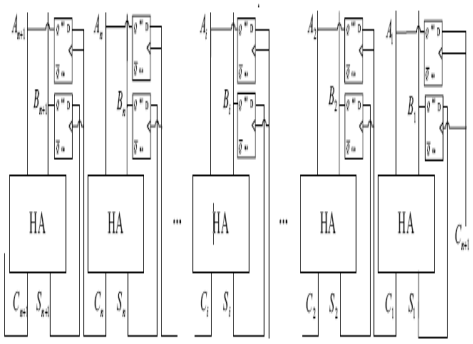

Figure 5: The structure of Barrel Integer Adder

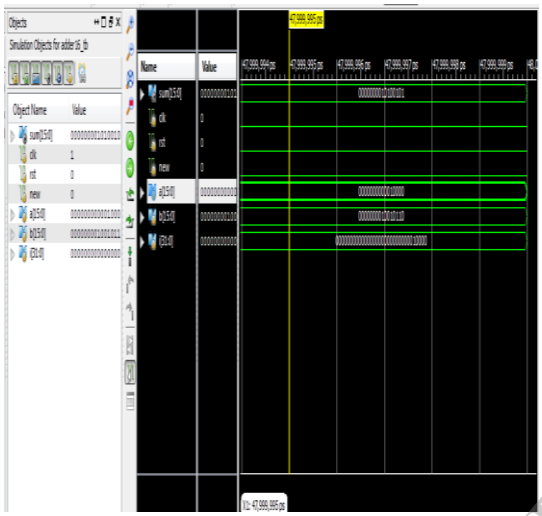

Figure 6: wave forms of barrel integer adder

V.CONCLUSION

The barrel integer adder is designed in this project improved the speed of integer addition algorithm.The speed of 106 bits barrel integer adder reached 151.03Mhz. Barrel integer adder has a good foundation for the improvement ofthe multiplier performance.

VI.FUTURE SCOPE

By reducing the number of iterations we can increase the speed of addition and reduce the power consumption .

VII . REFERENCES

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