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The Active Voltage Quality Regulator with the DC-Link Capacitor Boosting Circuit

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***Abstract*—Voltage sags have always been a huge threat to sensitive industrial and commercial electrical consumers; and deep sags with long duration time are usually more intolerable. In this paper, a new topology of series-connected compensator is presented to mitigate long duration deep sags, and the compensation ability is highly improved with a unique shunt converter structure acting as a DC-Link capacitor boosting circuit that has been theoretically analyzed. Additionally, the proposed active voltage equality regulator is a cost effective solution for long duration sags that are lower than 50% of the nominal voltage as it is compared with the traditional dynamic voltage restorer. High operation efficiency is ensured by applying the dc-link voltage adaptive control method. Analysis, along with simulation and experimental results, is presented to verify the feasibility and effectiveness of the proposed topology.**

***Keywords*—Dynamic voltage restorer (DVR), dynamic sag correction, long duration deep sag, DC-Link capacitor boost circuit, seriesconnect compensator.**

I. INTRODUCTION

The Power quality (PQ) problems have obtained increasing attentions as they can affect lots of sensitive end-users including industrial and commercial electrical consumers. Studies indicate that voltage sags, transients, and momentary interruptions constitute 92% of all the PQ problems occurring in the distribution power system. In fact, voltage sags have always been a huge threat to the industry, and even 0.25 s voltage sag is long enough to interrupt a manufacture process resulting in enormous financial losses. Voltage sags are generally classified according to its depth and duration time. Typical sag can be a drop to between 10% and 90% of the rated RMS voltage and has the duration time of 0.5 cycles to 1 min. The majority of the sags recorded are of depth no less than 50%, but deeper sags with long duration time obviously cannot be ignored as they are more intolerable than shallow and short-duration sags to the sensitive electrical consumers. More characteristics about voltage sags are described in many customer power devices have been proposed to mitigate such voltage sags for sensitive loads.

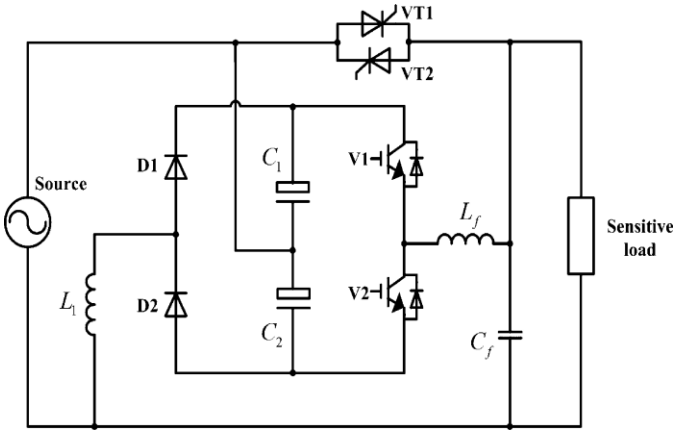

Fig. 1. Single-phase DySC configuration.

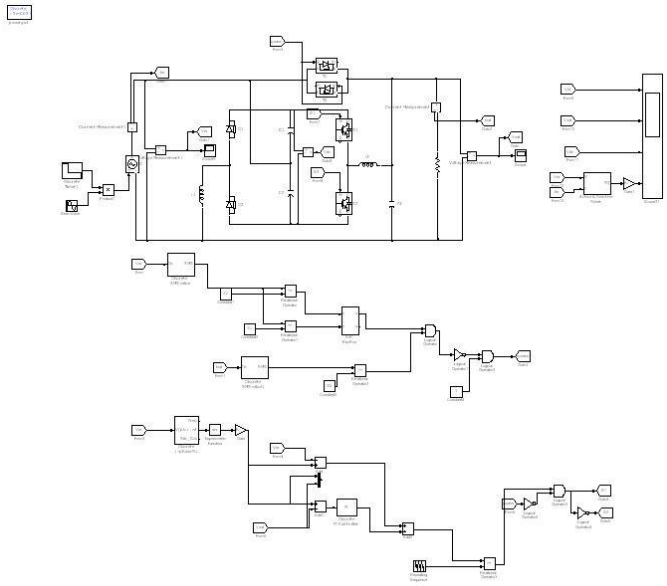

Fig. 1.1 SIMULATED DySC

The most studied voltage regulator topologies can generally categorized into two groups: the inverter-based regulator and direct ac–ac converters. Several ac–ac converter-based regulators are introduced. Series-connected devices (SD) are voltage-source inverter-based regulators and an SD compensate for voltage sags by injecting a missing voltage in series with the grid. There are lots of SD topologies, and key

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Vol. 6 Issue 07, July - 2017

features related to the evaluation of a certain SD topology are the cost, complexity, and compensation ability. Dynamic voltage restorer (DVR) is a commonly used SD and has been widely studied. The overall evaluation has shown that DVR with no storage and load-side-connected shunt converter ranks the highest as it can compensate for long-duration deep sags at a relatively low complexity and cost.

However, the aforementioned DVR topology is still not a cost effective solution for long duration deep sags as it regularly contains a series transformer that is heavy, bulky, and costly operating at the line frequency. This drawback is obviously non ignorable especially in low-power applications. A type of transformer less SD topology known as dynamic sag corrector (DySC) is proposed, and it is a low cost, small size, Light weight, and highly effective system for sag mitigation as the series transformer is no longer needed. There are several circuit structures of the DySC Fig. 1 illustrates another possible configuration. When the grid voltage differs from its desired waveform, a missing voltage will be injected and filtered by the DySC through its half-bridge series converter (V1, V2) and output filter（L_f, C_f） to maintain the load voltage at its rated value. During this period of time, the energy needed for the compensation is provided by the residual supply via a passive shunt converter (D1, D2, L_1) and stored in the dc-link capacitors（C_1, C_2 ）. So, the dc-link voltage should always be lower than the peak value of the supply voltage, and it means that the DySC can only compensate for voltage sags no deeper than 50% since the largest injection voltage of the DySC is solely determined by its dc-link voltage. The ride-through time of the DySC in deeper voltage sags is limited by the dc-link energy storage, and it is inadequate to provide reliable protection for sensitive loads. So, although the DySC is an excellent solution for sags in many cases, it is invalid for long-duration deep sags as its compensation ability is limited by the passive rectifier, either PWM rectifier or backup grid is adopted to increase the energy provided during voltage sags. But the compensation ability is greatly enhanced at the expense of significantly increasing the complexity and cost. In this paper, position of the shunt converter and series converter in the DySC is changed according to the structure differences between the DVR with the load-side-connected shunt converter and the DVR with the supply-side-connected shunt converter. As a result, the shunt converter together with the series converter formed a boost charging circuit and the dc-link voltage will be charged to exceed the peak value of the supply voltage. This obtained novel topology is called the transformer less active voltage quality regulator with the parasitic boost circuit (PB-AVQR), and it is capable of mitigating long duration deep voltage sags without increasing the cost, volume, and complexity compared with the traditional DySC topology. The dc-link voltage adaptive control method is also applied in the PB-AVQR to improve its operation efficiency. This paper starts with introducing the operating mode and working principles of the proposed configuration. Then, the parasitic boost circuit model is provided followed by the theoretical analysis to calculate its dc-link voltage. At last, the simulation results using MATLAB and experimental results on a 220 V-2kWprototype are given to verify the feasibility and effectiveness of the PB-AVQR topology.

II. TOPOLOGY AND PRINCIPLE

As shown in Fig. 2, the PB-AVQR topology is mainly consists of five parts, including a static bypass switch (VT1, VT2),a half-bridge inverter (V1, V2), a shunt converter (VT3, VT4),a storage module（C_1, C_2 ）, and a low-pass filter（L_f, C_f ）. The operating mode and applied control strategies are similar to what have been described in [25]. Under normal operating conditions, the static bypass switch is controlled to switch on and the normal grid voltage is delivered directly to

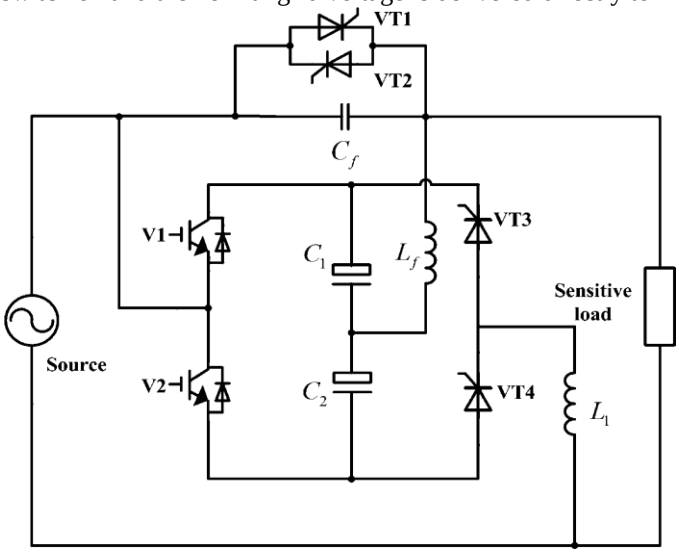

Fig. 2. Proposed PB-AVQR topology.

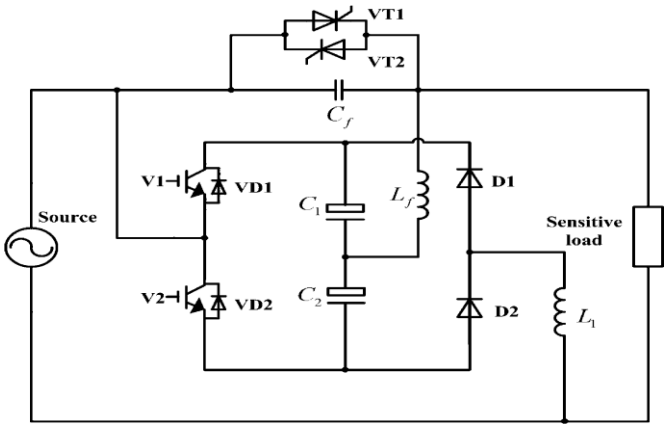

Fig. 3. SPB-AVQR topology.

International Journal of Engineering Research & Technology (IJERT)
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Vol. 6 Issue 07, July - 2017

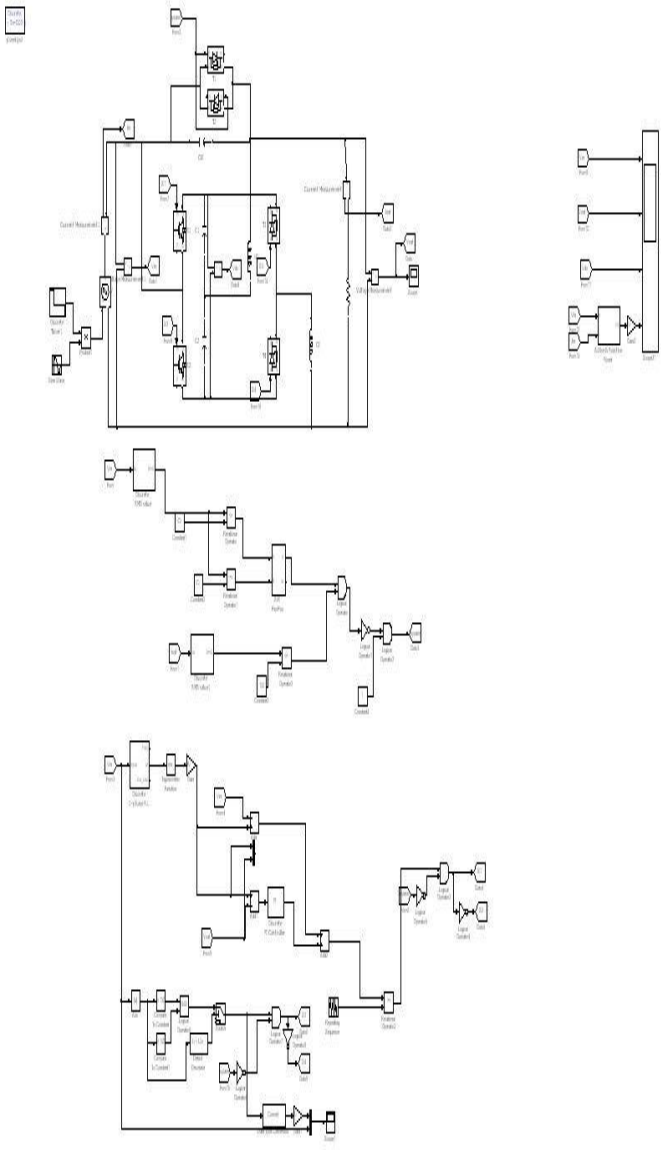


Fig. 3.1 SIMULATED PBAVQR

the load side via this bypass switch. When an abnormal condition is detected, the static bypass switch will be switched OFF and the inverter will be controlled to inject a desired missing voltage in series with the supply voltage to ensure the power supply of sensitive loads. There are totally two different kinds of control strategies in the proposed PB-AVQR system. When the grid voltage is lower than the rated voltage, an in-phase control strategy will be adopted and a phase-shift control strategy will be applied when the supply voltage is higher than the nominal voltage. Working principle of the PB-AVQR is different compared with that of the DySC due to its unique shunt converter structure. When the proposed configuration is analyzed, both the operating states of the switches (V1, V2) and the trigger angles of the thyristors (VT1,VT2) should be taken into consideration. So, a simplified PB-AVQR (SPB-AVQR) circuit shown in Fig.3, where two thyristors (VT3, VT4) in the proposed PB-AVQR are replaced by two diodes (D1, D2), is firstly introduced to better explain its working principles. The following analysis will be based on the SPB-AVQR which can be regarded as a special type of PB-AVQR. The only difference between these two configurations is that the shunt converter of the PB-AVQR is controllable while the shunt converter of the SPB-AVQR is uncontrollable. That is to say, the dc-link voltage of the SPBAVQR represents the upper limit of the dc-link voltage in the PB-AVQR structure. So, theoretical conclusions drawn with the SPB-AVQR are basically applicable to the PB-AVQR.

As shown in Fig. 3, switches V1 and V2 are now also parts of the parallel circuit, which means that the dc-link voltage will be affected by the on/off status of the switches. So, the turn on and turn off conditions of the compensation process should be considered to understand the working principles about the parasitic boost circuit of the SPB-AVQR. Figs. 4 and 5 illustrate four different operating conditions of the SPB-AVQR within one switching cycle during the positive and negative half-cycle of the sinusoidal supply voltage separately. Both the compensation process and charging process can be explained based on these operating conditions. In Figs. 4 and 5, the solid line means that there is current flowing through and arrows depict directions. Operating conditions during the positive half-cycle are illustrated in Fig. 4. When V2 is switched on, as shown in Fig. 4(a), the grid charges the inductor L_1 via the diode D2 and the capacitorC_2 discharges to maintain the load voltage. When V2is switched off, as shown in Fig. 4(b), the energy stored in the inductor during previous period is released to dc-link capacitorsC_1 and C_2 through VD1 which is the antiparallel diode of V1.Operating conditions during the negative half-cycle are given in Fig. 5. When V1 is switched on, as shown in Fig. 5(a), the inductor L_1 is charged via the diode D1, and the load is compensated by the capacitor C_1. When V1 is switched off, as shown in Fig. 5(b), the energy stored in L_1 is released through VD2, which is the antiparallel diode of V2, to capacitors C_1 and C_2 .So, in each half-cycle of the grid, one capacitor of the dc-link discharges to provide the energy needed for the compensation, and this energy is actually obtained from the supply source via the charging process described earlier.

Apparently, the charging circuit of the proposed configuration works exactly like a boost circuit and the dc-link voltage in this situation is controlled by the duty ratio of the two switches. So, the compensation ability of the SPB-AVQR is theoretically unlimited as long as the grid is strong enough to provide the needed power. However, as the boost circuit is parasitic on the series inverter, and the two switches are actually controlled according to the missing voltage, there still exist some restrictions. The relationships between the dc-link voltage and other system parameters will be discussed in the next section. In Figs. 4 and 5, two endpoints of the inverter are marked as *a* and *b*. Parts of the waveforms obtained at the inverter side and load side under four operating conditions are

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 07, July - 2017

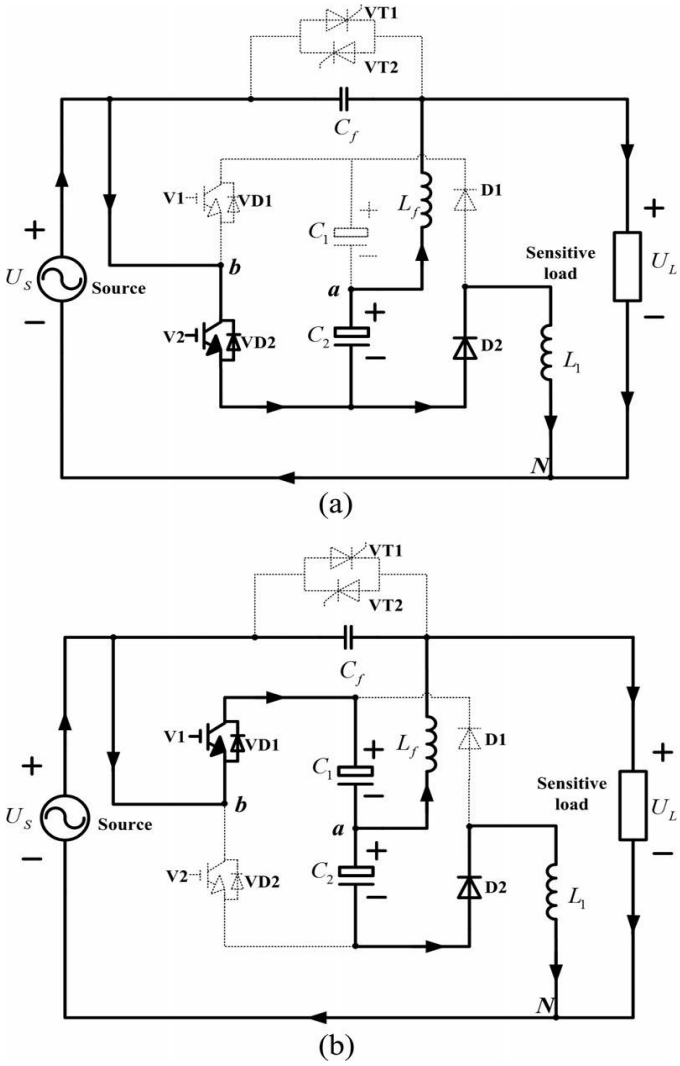
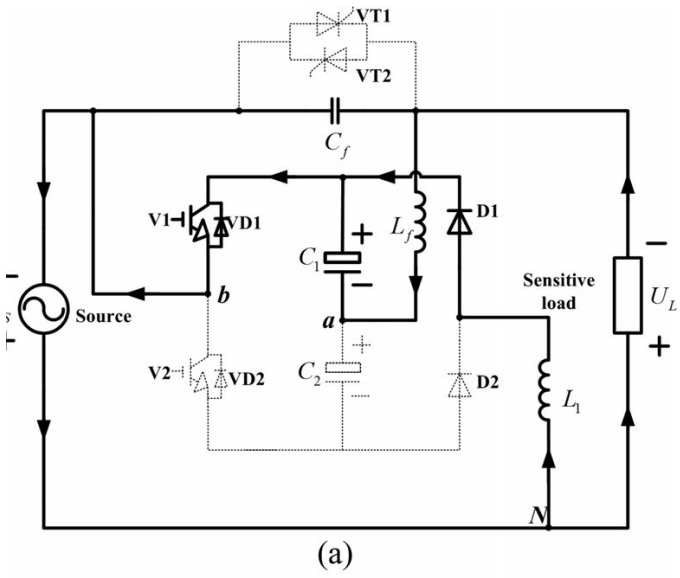


Fig. 4. Operating conditions during positive half-cycle. (a) V2 switched on.(b) V2 switched off.



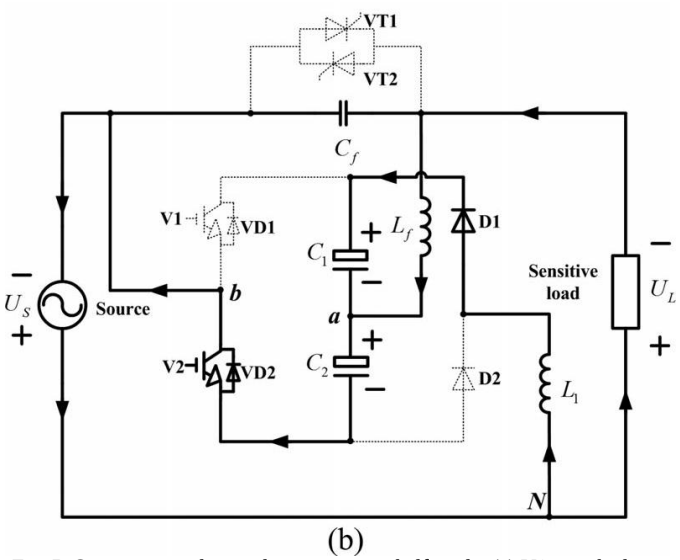


Fig. 5. Operating conditions during negative half-cycle. (a) V1 switched on. (b) V1 switched off.

Schematically shown in Fig. 6, where U_{aN} represents the voltage between *a* and *N*. As shown in Fig. 6, when V1/V2 is switched on/off, the dc-link voltage will be added/subtracted to the supply voltage to get a switching pulse voltage U_{aN} and the switching harmonics of U_{aN} will be filtered by L_f and C_f to get a smooth load voltage. So, the load voltage will be maintained at its rated value if the inverter is properly controlled according to the required missing voltage during sags.

III. MODELING AND THEORETICAL ANALYSIS

DC-link voltage is a key parameter to evaluate the compensation ability about a series compensation device since

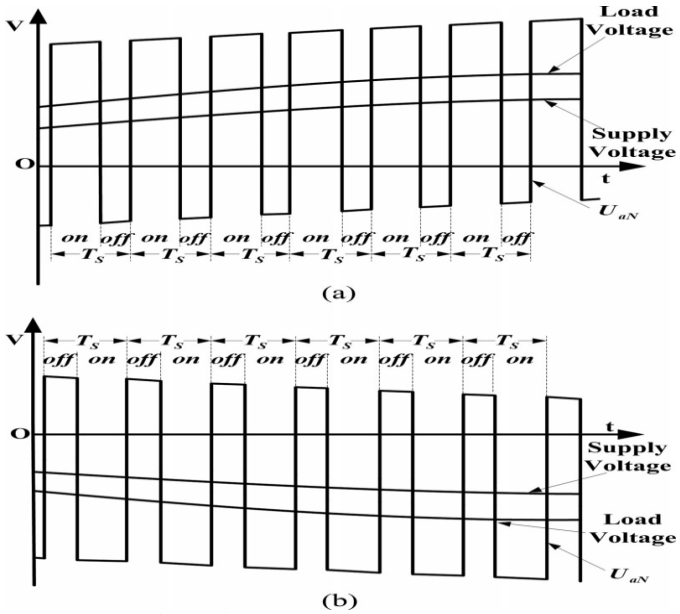


Fig. 6. Waveforms of supply voltage, load voltage, and *UaN*. (a) V2 on/off.(b) V1 on/off

it decides the maximum value of the injected compensation voltage. In this section, in order to evaluate the compensation ability of the proposed topology and verify its feasibility in

International Journal of Engineering Research & Technology (IJERT)
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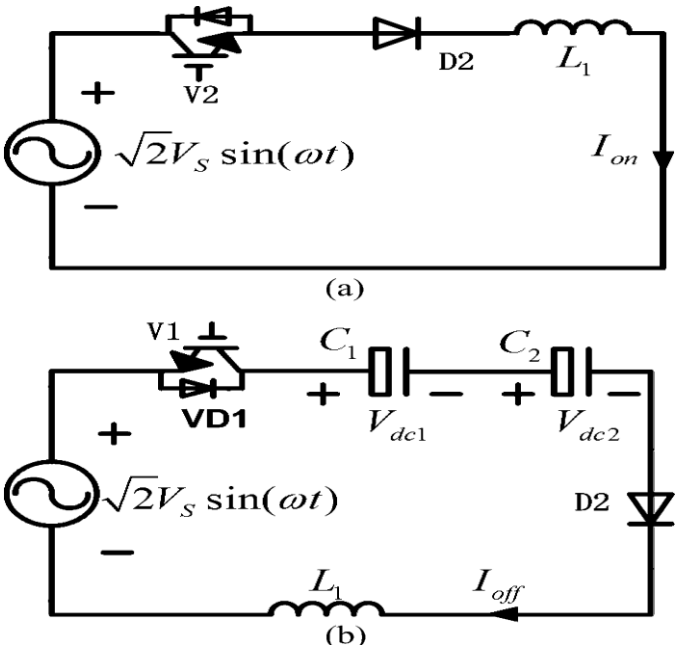
Vol. 6 Issue 07, July - 2017

mitigating long duration deep sags, relationships between the dc-link voltage and other system parameters will be derived based on the circuit model of the aforementioned operating conditions. As can be seen from Figs. 4 and 5, working principles during the positive and negative half-cycle of the supply voltage are the same, so the following analysis will be focused on the situation in the positive half-cycle. The control strategy applied for voltage sags is in-phase compensation, so the energy needed to maintain the load voltage in one half-cycle can be expressed as below equation

$$E_0 = \frac{T_0 \Delta V}{2V_{\text{ref}}} P_0 \qquad (1)$$

WhereT_0 is the grid voltage period time, V_{ref} is the rated rms Value of the load voltage, P_0 is the rated load power, and ΔV is the rms value of the missing voltage. In steady-state compensation, the energy needed for the compensation should completely be provided by the residential grid which is also the charging energy through the parasitic boost circuit in this case. So the charging energy provided during T_0 /2 referred to
as E_1 equals to E_0. E_0 can be easily obtained according to (1), but the calculation of E_1 involves with the operating conditions shown in Fig. 4. The simplified circuit model of Fig. 4 is illustrated in Fig. 7, where compensation loop including the filter and the load is ignored and only the charging circuit is considered.



In Fig. 7, V_S is the rms value of the supply voltage. Two state equations can be obtained based on Fig. 7 and written in the equation (2)

$$\begin{cases} L_1 \dfrac{dI_{\text{on}}}{dt} = \sqrt{2}V_S \sin(\omega t) \\ L_1 \dfrac{dI_{\text{off}}}{dt} = \sqrt{2}V_S \sin(\omega t) - V_{\text{dc1}} - V_{\text{dc2}}. \end{cases} \qquad (2)$$

the analysis will be significantly simplified if some realistic approximations are carried out. Then(2) can be discredited into (3) based on two following assumptions:$C1$ and $C2$ are well designed so that Vdc1 and Vdc2 can be regarded equal without considering their ripple voltages; the switching frequency is much higher than the line frequency that the supply voltage in the nth switching cycle can be treated as a constant value

$$\begin{cases} L_1 \Delta I_{\text{on}n} = \sqrt{2}V_S \sin(\omega n T_s) t_{\text{on}n} \\ L_1 \Delta I_{\text{off}n} = [\sqrt{2}V_S \sin(\omega n T_s) - 2V_{\text{dc}}] t_{\text{off}n} \end{cases} \qquad (3)$$

where $t$on$n$ and $t$off n are, respectively, the turn-on and turn-off time ofV2 in the nth switching cycle, T_s is the switching period, Vdc is the steady-state dc-link voltage, and ΔIon$n$ or ΔIoff n represents the variation amount in charging current during $t$on$n$or $t$off n . As the analysis is within the positive half-cycle of the grid, there exists a constraint: $n \leq T0$ /2T_s. Apparently, $t$on and $t$off n here are actually the inverter's duty cycle and they can be expressed as (4) when two-level symmetric regular-sampled PWM method is adopted

$$\begin{cases} t_{\text{on}n} = \dfrac{T_s}{2}\left[1 + \dfrac{\sqrt{2}\Delta V \sin(\omega n T_s)}{V_{\text{dc}}}\right] \\ t_{\text{off}n} = \dfrac{T_s}{2}\left[1 - \dfrac{\sqrt{2}\Delta V \sin(\omega n T_s)}{V_{\text{dc}}}\right]. \end{cases} \qquad (4)$$

The recursion formula of the charging current at the end of the nth switching cycle can be obtained by combining (3) and (4)

$$I_{\text{off}n} = I_{\text{off}(n-1)} + \frac{T_s}{L_1}[\sqrt{2}V_{\text{ref}} \sin(\omega n T_s) - V_{\text{dc}}] \qquad (5)$$

Where Ioff n represents the charging current instantaneous value at the end of the nth switching cycle and ΔIon$n$ can be derived at the same time

$$\Delta I_{\text{on}n} = \frac{\sqrt{2}T_s V_S \sin(\omega n T_s)}{2L_1}\left[1 + \frac{\sqrt{2}\Delta V \sin(\omega n T_s)}{V_{\text{dc}}}\right]. \qquad (6)$$

The energy stored in an inductor is related to the current that flows through it, so the charging energy provided by the grid via the parasitic boost circuit in the nth switching cycle can be
expressed and then rearranged as equation (7)

$$E_{\text{in}n} = \frac{1}{2}L_1 \Delta I_{\text{on}n}^2 + L_1 I_{\text{off}(n-1)} \Delta I_{\text{on}n}. \qquad (7)$$

Ioff $(n-1)$ in (7) can be superimposed according to the recursion formula shown in (5). Before the expression is given, there are some features about the charging current

International Journal of Engineering Research & Technology (IJERT)
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Vol. 6 Issue 07, July - 2017

should be clarified:1) the value of the charging current cannot be lower than zero as the current flowing through a diode is unidirectional; 2)the value of the charging current can either be zero or nonzero and its value always decreases after increasing in one half-cycle of the sinusoidal grid voltage. Then, the nonzero terms of the charging current can be derived as follows:

$$I_{\text{off}(n-1)} = \sum_{k=n_0}^{n-1} \frac{T_s}{L_1}\left[\sqrt{2}V_{\text{ref}}\sin(\omega k T_s) - V_{\text{dc}}\right] \quad (8)$$

where $n0$ is the initial superposition instant and Ioff n is always equal to zero when n is smaller than $n0$. So, $n0$ can be calculated according to (5) and expressed as follows:

$$n_0 = \text{ceil}\left(\frac{T_0 \arcsin\frac{V_{\text{dc}}}{V_{\text{ref}}}}{2\pi T_s}\right) \quad (9)$$

Where ceil (•) represents the rounded up function and the arcsine function here ranges from 0 to $\pi/2$. Furthermore, when the charging current calculated by (8) decreases to the value no more than zero, n will reach its upper limit denoted by ne. Substituting (6), (8), and (9) into (7), the energy provided by the supply in the nth switching cycle can be written as follows:

$$E_{\text{inn}} = \frac{T_s^2 V_S^2 A^2}{4L_1}(1+\sqrt{2}BA)^2 + \frac{\sqrt{2}T_S^2 V_S A}{2L_1 V_{\text{dc}}} \times (V_{\text{dc}} + \sqrt{2}\Delta V A)\sum_{k=n_0}^{n-1}(\sqrt{2}V_{\text{ref}}C - V_{\text{dc}}) \quad (10)$$

where

$$A = \sin\omega n T_s$$
$$B = \frac{\Delta V}{V_{\text{dc}}}$$
$$C = \sin\omega k T_s.$$

$E1$ now can be obtained if (10) is added with n ranging from1 to $T0$ /2Ts . So, the overall energy balance equation can be written as follows:

$$E_1 = \frac{T_s^2 V_S^2}{4L_1}\left(\sum_{n=1}^{\frac{T_0}{2T_s}} A^2 + 2\sqrt{2}B\sum_{n=1}^{\frac{T_0}{2T_s}} A^3 + 2B^2\sum_{n=1}^{\frac{T_0}{2T_s}} A^4\right) + \frac{T_s^2\sqrt{2}V_S}{2L_1}\sum_{n=n_0}^{n_e}\left[(A+\sqrt{2}BA^2)\sum_{k=n_0}^{n-1}(\sqrt{2}V_{\text{ref}}C - V_{\text{dc}})\right] = \frac{T_0\Delta V}{2V_{\text{ref}}}P_0 = E_0. \quad (11)$$

The charging current peak value Imax is considered to arise at the switching cycle after the value of (8) reaches its upper limit. So Imax is expressed as follows:

$$I_{\max} = \frac{\sqrt{2}T_s V_S \sin(\omega n_{\max} T_s)}{2L_1}[1+\sqrt{2}B\sin(\omega n_{\max} T_s)] + \sum_{n=n_0}^{n_{\max}}\frac{T_s}{L_1}(\sqrt{2}V_{\text{ref}}C - V_{\text{dc}}) \quad (12)$$

where $n$max is the switching cycle when Ioff n reaches its maximum value and $n$max can be written as follows:

$$n_{\max} = \text{ceil}\left[\frac{T_0\left(\pi - \arcsin\frac{V_{\text{dc}}}{V_{\text{ref}}}\right)}{2\pi T_s}\right]. \quad (13)$$

So far, the main features of the SPB-AVQR topology can be described by (11) and (12). As shown in (11), the dc-link voltage is not only related to the supply voltage, but also associated with the charging inductance, load active power, and switching frequency. However, the dc-link voltage cannot be obtained directly from (11) as $n0$ and ne cannot be computed with unknown dc-link voltage. So, an iterative algorithm is applied to estimate the dc-link voltage, where Ts, VS , $T0$, Vref, $L1$, and $P0$ are all treated as constants. A flow chart of the adopted calculating method is illustrated in Fig. 8, where Vdc0 is the initial value for Vdc and ΔVdc is the iterative step. The algorithm is terminated if the error between $E0$ and $E1$ is smaller than the error tolerance ε. Moreover, the charging current can be calculated by (12) and(13) as long as Vdc is obtained .Fig. 9 shows the relationships between the steady-state dc-link voltage and the supply voltage with different inductance values obtained according to (11). Other system parameters are listed as follows: $P0$ = 2 kW, Ts = (1/15000)s, $T0$ = 0.02 s, Vref= 220 V. The black solid line in Fig. 9 is the Vdc−VS curve of the DySC topology. As can be seen in Fig. 9, the steady-state dc-link voltage of the SPB-AVQR under different supply voltage is much higher than that of the DySC topology and it decreases lightly with the falling of the supply. Additionally, when the supply voltage is lower than 50% of its rated value, the dc-link voltage of the SPB-AVQR is still maintained high enough for the compensation while that of the DySC is too low to mitigating the deep sag. Fig. 9 also indicates that the dc-link voltage of the SPB-AVQR becomes higher with a lower inductance under the same circumstance. Fig. 10 gives the Imax−VS curve under the same condition. It presents that the steady-state charging current peak value increases with the decreasing of the supply voltage and it can be suppressed by increasing the charging inductance.

International Journal of Engineering Research & Technology (IJERT)
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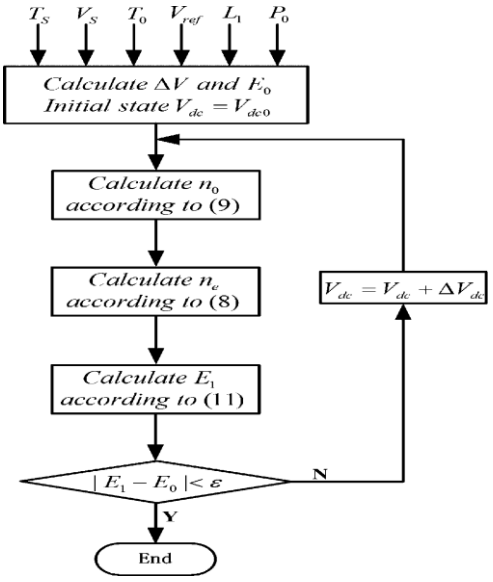


Fig. 8. Flow chart for calculating *V*dc.

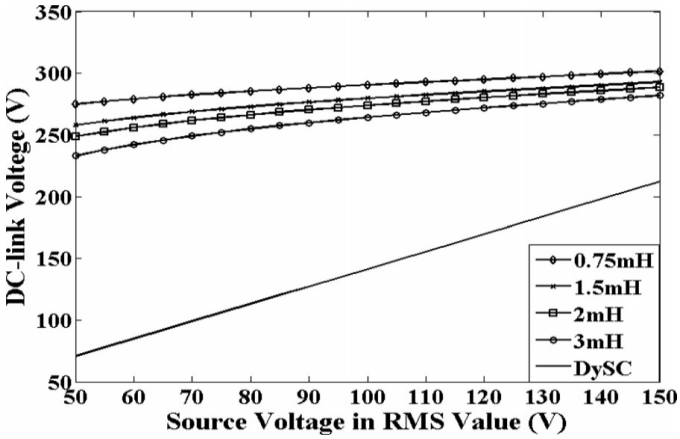


Fig. 9. Vdc−VS curve of the SPB-AVQR with different inductances.

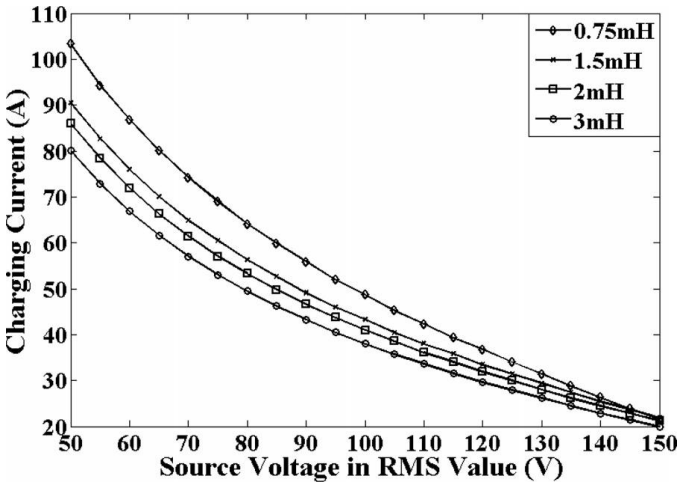


Fig. 10. Imax−VS curve of the SPB-AVQR with different inductances.

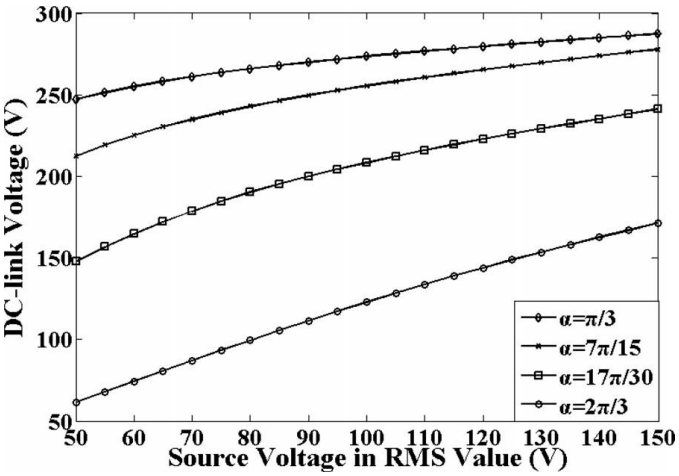


Fig. 11. Vdc−VS curve of the PB-AVQR with different trigger angles.

Although conclusions drawn from the theoretical analysis for the SPB-AVQR can also be applied to the proposed PB-AVQR topology, there still exist some differences in their dc-link voltages. When the proposed PB-AVQR is discussed, the trigger pulse angle α for VT3 and VT4 should also be taken into consideration. In the PB-AVQR circuit, the charging process begins after the VT3 or VT4 is triggered, so the initial superposition instant $n0$ in (11) is now determined by α denoted by $n1$ and the energy balance equation is written as follows:

$$\frac{T_s^2 V_S^2}{4L_1}\left(\sum_{n=n_1}^{n_e} A^2 + 2\sqrt{2}B\sum_{n=n_1}^{n_e} A^3 + 2B^2\sum_{n=n_1}^{n_e} A^4\right) + \frac{T_s^2\sqrt{2}V_S}{2L_1}\sum_{n=n_1}^{n_e}\left[(A+\sqrt{2}BA^2)\sum_{k=n_1}^{n-1}(\sqrt{2}V_{\mathrm{ref}}C - V_{\mathrm{dc}})\right] = \frac{T_0\Delta V}{2V_{\mathrm{ref}}}P_0. \quad (14)$$

Here, *ne* is still determined by (8) as aforementioned and *n*1can be derived as follows:

$$n_1 = \mathrm{ceil}\left(\frac{\alpha T_0}{2\pi T_s}\right). \quad (15)$$

Furthermore, the thyristors are triggered only once in each half-cycle and the current through them should be higher than the holding current to maintain the triggered state. So, α is required to meet the constraint expressed as follows:

$$\sqrt{2}V_{\mathrm{ref}}\sin\alpha > V_{\mathrm{dc}}. \quad (16)$$

The charging current peak value of the PB-AVQR can still be described by (12) as long as $n0$ is substituted with $n1$. As can be seen from (14) and (15), the trigger pulse of the PB-AVQR will certainly affect its dc-link voltage and charging current. Fig. 11 shows the V_{dc}−V_S curve under the influence of α according to (14). The charging inductor in Fig. 11 is set to 2 mH and other parameters remain the same as those in

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 07, July - 2017

Fig. 9. Fig. 11 demonstrates that the steady-state dc-link voltage gets higher with a smaller trigger angle as the charging time becomes longer.

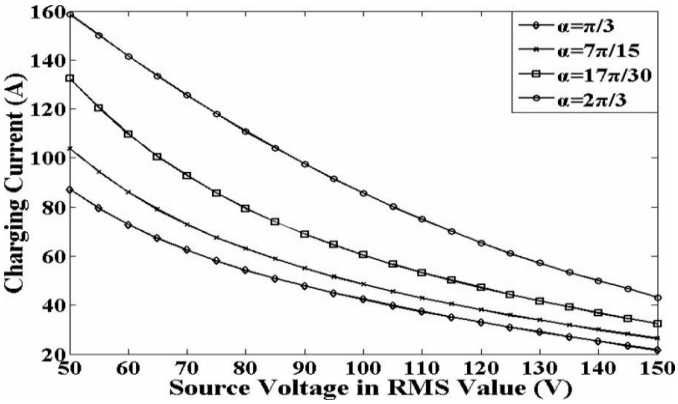


Fig. 12. Imax−VS curve of the PB-AVQR with different trigger angles.

It also indicates that the PB-AVQR is capable of mitigating deep sags with a proper trigger pulse. Fig. 12 presents how α affects the *I*max−*VS* curve under the same condition. As shown in Fig. 12, the charging current peak value can be reduced by decreasing α with the same supply voltage.

IV. SIMULATION AND EXPERIMENTAL VERIFICATION

In order to show the validity of the proposed PB-AVQR, simulation and experimental results are presented in this section. The simulation results are based on the MATLAB software and the experimental results are based on a 2 kW single-phase prototype.

A. System Parameters

There are mainly four parameters need to be designed, namely the dc-link capacitor *C*1 /*C*2 , the filter inductor *Lf* , the filter capacitor *Cf* , and the charging inductor *L*1 .

During the steady-state compensation, one capacitor discharges at the switched-on position and two capacitors are both charged at the switched-off position in each switching cycle. Furthermore, *C*1 and *C*2 discharge, respectively, in the negative and positive half-cycle of the supply. So, if the two capacitors are treated equally during the charging process, the energy balance equation that required for the capacitors can be written as

$$\frac{T_0 \Delta V}{4V_{\text{ref}}} P_0 = \frac{1}{2} C_{1(2)} V_{\text{dc}}^2 - \frac{1}{2} C_{1(2)} (V_{\text{dc}} - v_{\text{dc}})^2 \qquad (17)$$

Where *v*dc is the fluctuation voltage of *V*dc. In the theoretical analysis, the dc-link voltage is assumed to be a constant. So*v*dc/*V*dc here is limited within 5% at the voltage drop of 50%to minimize the overall dc-link voltage ripple. In this way, the estimated minimum value of *C*1 /*C*2 can be calculated according to (17) with *V*dc substituted by the dc-link set value *V*dc-set. How to set the dc-link value is introduced in [25] and in this paper it is given as

$$V_{\text{dc-set}} = \begin{cases} 1.2 \times \sqrt{2}(V_{\text{ref}} - V_S) + 40 & V_S < V_{\text{ref}} \\ 1.5 \times \sqrt{2(V_S^2 - V_{\text{ref}}^2)} + 40 & V_S > V_{\text{ref}}. \end{cases} \qquad (18)$$

TABLE I
SYSTEM PARAMETERS

Description	Parameters	Real value
Nominal voltage	V_{ref}	220V
Line frequency	f_0	50Hz
Switching frequency	f_s	15kHz
DC-link capacitor	C_1/C_2	4700μF
Filter inductor	L_f	1.5mH
Filter capacitor	C_f	20μF
Charging inductor	L_1	2mH

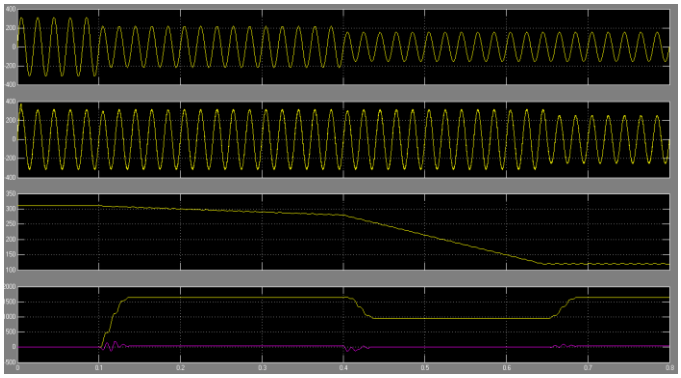


Fig. 13. Simulation result of the DySC.

As shown in Figs. 9–12, a higher dc-link voltage will be obtained with a smaller *L*1 , but the peak value of the charging
current will get larger at the same time. So, charging inductance*L*1 is designed as a result of the compromise between the compensation ability and the charging current peak value. The main function of the output LC filter in the proposed structure is to eliminate the harmonic components of the injected compensation voltage. The value of *Lf* and *Cf* are designed according to its natural frequency and several other criterions which are given as follows:

$$\begin{cases} \dfrac{1}{2\pi\sqrt{L_f C_f}} = \chi f_s \\ L_f < \dfrac{v_L}{\omega_0 I_{L\max}} \\ C_f < \dfrac{I_{\text{ripple}}(\chi^2 + 1)}{8 V_{\text{dc}} f_s} \end{cases} \qquad (19)$$

Where *fs* is the switching frequency, *vL* is the voltage drop Across the inductor *Lf* at *IL* max, *IL* max is the maximum value of the load current, *I* ripple is the maximum ripple current of the filter and χ is the coefficient between the switching frequency and the filter's natural frequency. Generally, χ ranges from 0.05to 0.2.

The PB-AVQR system's key parameters are listed in Table- I according to the design principles mentioned earlier.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 07, July - 2017

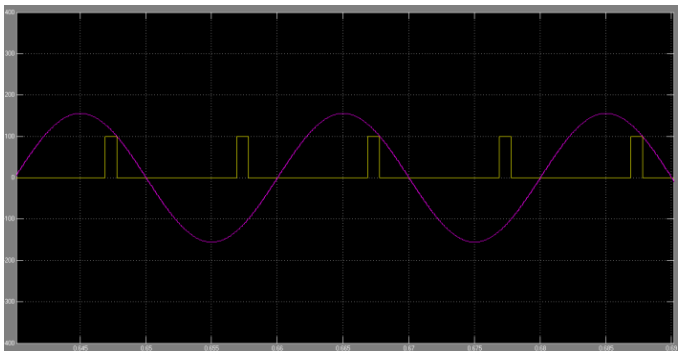
B. Simulation Results

Fig. 13 shows the simulation results of the DySC topology with different supply voltages. In the simulation, the supply voltage drops to 180 V at 0.1 s and then falls to 100 V at 0.4 s.

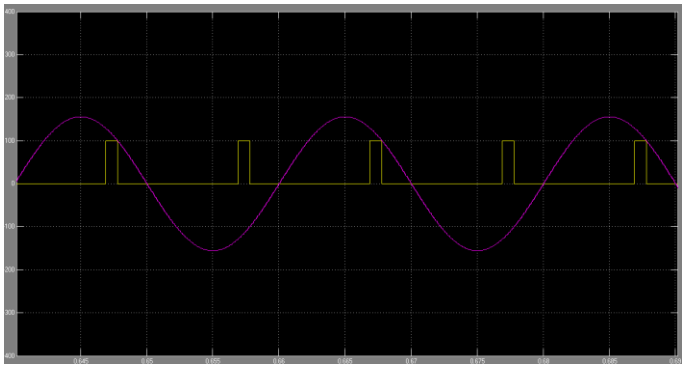
As shown in Fig. 13, when the supply voltage is 180V, the DySC can effectively compensate for the voltage sag; however, when the supply voltage drops to 100 V, the load voltage becomes not sinusoidal as the maximum injected compensation voltage is limited by the low steady-state dc-link voltage. Fig. 13 also indicates that the DySC can only mitigate deep sags for a few line cycles depending on the energy stored in dc-link capacitors as its steady-state dc-link voltage is always lower than the peak value of the supply voltage. The graphics of the active and reactive power are also included in Fig. 13. When the supply voltage is 180 V, the dc-link voltage does not reach its steady state value with limited simulation time, so the active power of the supply is lower than the load power and its value is about1.6 kW. When the dc-link voltage reaches its steady-state value with 100 V supply voltage, the active power of the supply is about 1.65 kW which means that the load voltage is no longer maintained.

Fig. 14. Simulation result of the PB-AVQR.

The simulation results of the proposed PB-AVQR topology under the same condition is shown in Fig. 14. As can be seen in Fig. 14, when supply voltage changes, the dc-link voltage precisely tracks *V*dc-set according to (18) and it also remains enough high for the compensation even with a 100 V supply voltage. Fig. 14 also indicates that the transient response here is not very good, but this can be improved by increasing the set value for dc-link voltage. The active power of the supply during the steady-state compensation is 2 kW, and it is the same as the load power which means that the load voltage is effectively ensured. The reactive power during the steady-state compensation is about 1.1 kvar with 180 V supply and is about 1.4 kvar with100 V supply. The reactive power of the proposed PB-AVQR is higher than that of the DySC due to the dc-link voltage adaptive control method. Additionally, the instantaneous value of the active and reactive power can be suppressed by properly designing *V*dc-set and the charging time of the capacitors. Fig. 15 show strigger pulses for thyristors under different grid voltage. The supply voltage is 180 V in Fig. 15(a) and is 100 V in Fig. 15(b).As shown in Fig. 15, the trigger angle becomes smaller to ensure the compensation energy needed when the grid voltage decreases.



(a)



(b)

Fig. 15. Trigger signals under different supply voltage values. (a) 180Vsupplyvoltage. (b) 100 V supply voltage.

V. CONCLUSION

This paper has presented the active voltage quality regulator with dc-link capacitor boost circuit to mitigate long duration deep voltage sags. The proposed PB-AVQR topology is derived from the DySC circuit and the compensation performance is highly improved without increasing the cost, weight, volume, and complexity. It is relatively cost-effective solution for deep sags with long duration time compared with the traditional DVR topology with load-side-connected shunt converter as a series transformer is no longer needed. The working principle and circuit equations are given through theoretical analysis. Simulation and experimental results are presented to verify the feasibility and effectiveness of the proposed topology in the compensation for long duration deep voltage sags that are lower than half of its rated value. The operating efficiency of the proposed PB-AVQR system also remains at a relatively high level as the dc-link voltage adaptive control method is adopted. Ina conclusion, the proposed PB-AVQR topology in this paper provides a novel solution for long duration deep voltage sags with great reliability and compensation performance.

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