THD Reduction in AC Drives with Z-Source Inverter

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Abstract- **Three-level Z-source inverters are recent single-stage topological solutions proposed for buck-boost energy conversion with all favourable advantages of three-level switching retained. Through careful design of their MCPWM technique, both inverters can function with the minimum of six device commutations per half carrier cycle (similar to that needed by a traditional buck three-level NPC inverter), while producing the correct volt-sec average and inductive voltage boosting at their ac output terminals. Physically, the designed modulation scheme can conveniently be implemented using a generic "alternative phase opposition disposition" multi carrier-based modulator with the appropriate triple offset and time advance/delay added. The designed inverters, having a reduced THD and high efficiency.**

Index Terms **– Z-source inverter, THD, multi carrier signal.**

I-INTRODUCTION

Many industrial applications require higher power converters (inverters) which are now almost exclusively implemented using one of the multilevel types. Multilevel converters offer many benefits for higher power applications which include an ability to synthesize voltage waveforms with lower harmonic content than two-level converters and operation at higher dc voltages using series connection of a basic switching cell of one type or another. Even though many different multilevel topologies have been proposed, the three most common topologies are the cascaded inverter, the diode clamped inverter, and the capacitor Clamped inverter. Among the three, the three level diode clamped [also known as the neutral point clamped (NPC)] inverter has become an established topology in medium voltage drives and is arguably the most popular certainly for three-level circuits. However, the NPC inverter is constrained by its inability to produce an output line-to-line voltage greater than the dc source voltage. For applications where the dc source is not always constant, such as a fuel cell photovoltaic array, and during voltage sags, etc., a dc/dc boost converter is often needed to boost the dc voltage to meet the required output voltage or to allow the nominal operating point to be favourably located . This increases the system complexity and is desirable to eliminate if possible. The Z-source inverter topology was proposed to overcome the above limitations in traditional inverters. The Z-source concept can be applied to all dc-to-ac , ac-to-dc, ac-to ac , and dc-to-dc , power conversion whether two-level or multilevel. The Z-source concept was extended to the NPC inverter where two additional Z-source networks were connected between two isolated dc sources and a traditional NPC inverter. In spite of its effectiveness in achieving voltage buck–boost conversion, the Z-source NPC inverter proposed in is expensive because it uses two Z-source networks, two isolated dc sources, and requires a complex modulator for balancing the boosting of each Z-source network. To overcome the cost and modulator complexity issues, the design and control of an NPC inverter using a single Z-source network was presented in . The operational analysis and optimal control of the reduced element count (REC) Z-source NPC inverter was subsequently described.

II-TOPOLOGY OF DIODE CLAMPED Z- SOURCE INVERTER

It basically has an impedance network that couple the converter main circuit to the power source. This addition of impedance network introduce a unique features that cannot be used or out of the capabilities of both the traditional three phase voltage source inverter and three phase current source inverter. The limitations for the traditional inverters are being solved in the Z-source inverter. Figure 3 shows that a two-port network that consists of a split-inductor L1 and L2 and capacitors C1 and C2 connected in X shape is employed to provide an impedance source coupling the inverter to the dc source. The dc source can be a current or a voltage source. Thus, the dc source can be a capacitor, an inductor, fuel cell, thyristor converter, diode rectifier, battery or a combination of those.

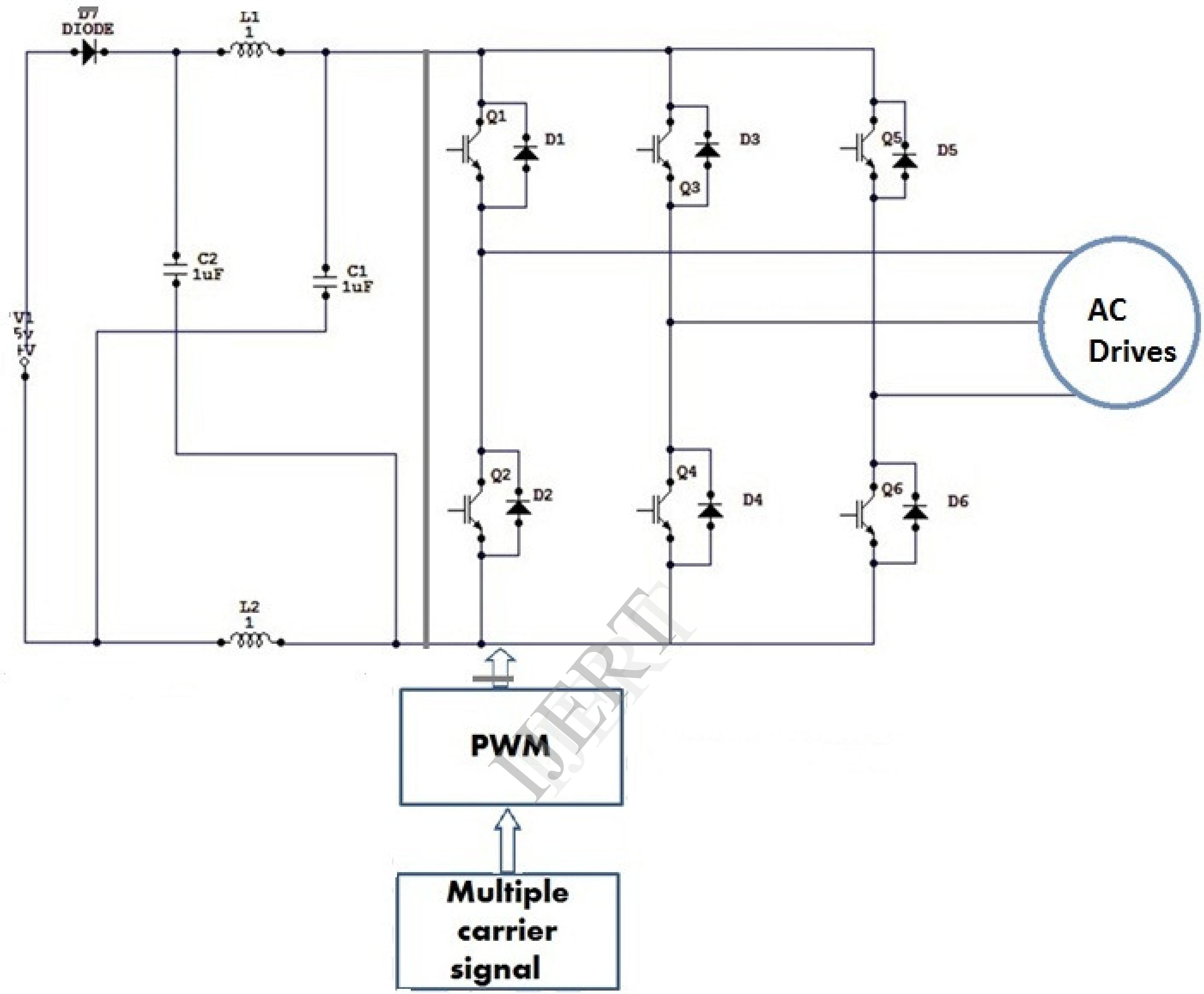

Fig.1.Topology of Diode-Clamped Z-Source Inverter

As mentioned earlier, by coupling an impedance network from the main circuit to the power source, Z-source inverter introduces a unique feature that cannot be observed in the traditional inverters. The unique feature of the three phase Z-source inverter is that the output ac voltage can be any value between zero and infinity regardless of the fuel cell voltage. This feature shows that the three phase Z-source inverter is a buck-boost inverter. Let us briefly analyse the three phase Z-source inverter structure before proceeding to its operating principle and control of the Z-source inverter. For a traditional inverters such as voltage source inverter and current source inverters, it has only eight permissible switching states. From those eight permissible switching states, six of them are active

In the traditional inverters, this shoot-through zero state is not allowed because it could destroy devices due to the electromagnetic interference (EMI). This third zero state is also known as the shoot-through zero state. The main reason for the shoot-through zero state is allowed in Z-source inverter is down to the inclusion of the impedance network. Thus, by using this extra permissible switching state, the three phase Z-source network can provide its unique feature which is buck-boost feature to the inverter. All the traditional switching control which is the pulse width-modulation (PWM) schemes can be apply to the Z-source inverter and their input-output relationship is maintained. By analysing the circuit, assuming that the capacitors C1 and C2 and inductors L1 and L2 have the same capacitance (C) and inductance (L), the Z-source network can become symmetrical. From the equivalent circuit, we can conclude that

$$V_{C1} = V_{C2} = V_C \; v_{L1} = v_{L2} = v_L \quad (1)$$

From equivalent circuit of the Z-source inverter viewed from the dc link when the inverter bridge is in the shoot-through zero state, given that the inverter is in the shoot-through zero state for an interval of T0, during the switching cycle, T, we can have

$$v_L = V_C \;\; v_d = 2V_C \;\; v_i = 0 \qquad (2)$$

From Equivalent circuit of the Z-source inverter viewed from the dc link when the inverter bridge is in one of the eight non shoot-through switching states ,the inverter is in one of the eight non shoot-through states for an interval of T1,during the switching cycle, T, we can have

$$v_L = V_0 - V_C \;\; v_d = V_0 \; v_i = V_C - v_L = 2V_C - V_0 \qquad (3)$$

Where T=T0+T1andV_0 is the dc source voltage

III- MODULATION TECHNIQUES

A. Definition of Modulation

Mainly the power electronic converters are operated in the “switched mode”. This means the switches within the converter are always in either one of the two states - turned off or turned on. Any operation in the linear region, other than for the unavoidable transition from conducting to non-conducting, incurs an undesirable loss of efficiency and an unbearable rise in switch power dissipation. To control the flow of power in the converter, the switches alternate between these two states. This happens rapidly enough that the inductors and capacitors at the input and output nodes of the converter average or filter the switched signal. The switched component is attenuated and the desired dc or low frequency ac component is retained. This process is called Pulse Width Modulation, since the desired average value is controlled by modulating the width of the pulses. For maximum attenuation of the switching component, the switch frequency fc should be high- many times the frequency of the desired fundamental ac component f1 seen at the input or output terminals. In large converters, this is in conflict with an upper limit placed on switch frequency by switching losses. For POWER MOSFET converters, the ratio of switch frequency to fundamental frequency fc/f1 may be as low as unity, which is known as square wave switching. Another application where the pulse number may be low is in converters which are better described as amplifiers, whose upper output fundamental frequency may be relatively high. These high power switch-mode amplifiers find application in active power filtering, test signal generation, servo and audio amplifiers. These low pulse numbers place the greatest demands on effective modulation to reduce the distortion as much as possible. The low pulse numbers place the greatest demands on effective modulation to reduce the distortion as much as possible. In these circumstances, multi-level converters can reduce the distortion substantially, by staggering the switching instants of the multiple switches and increasing the apparent pulse number of the overall converter.

B. Pulse Width Modulation

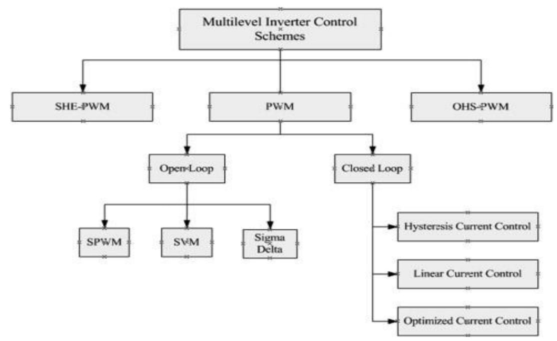

Fig.2. Classification of Multilevel Inverter Technique

The fundamental methods of pulse-width modulation are divided into the traditional voltage-source and current-regulated methods. Voltage-source methods more easily lend themselves to digital signal processor or programmable logic device implementation. However, current controls typically depend on event scheduling and are therefore analog implementations which can only be reliably operated up to a certain power level. In discrete current-regulated methods the harmonic performance is not as good as that of voltage-source methods. The carrier-based modulation schemes for multilevel inverters can be generally classified into two categories: phase-shifted and level-shifted modulations. Both modulation schemes can be applied to the cascaded H-bridge inverters. Total harmonics distortion of phase-shifted modulation is much higher than level-shifted modulation. Therefore we have considered level-shifted modulation. An m-level multilevel inverter using level-shifted multicarrier modulation scheme requires (m-1) triangular carriers, all having the same frequency and amplitude. The (m-1) triangular carriers are vertically disposed such that the bands they occupy are contiguous. There are three alternative Pulses with different phase relationships for the level-shifted multicarrier modulation three alternative carrier disposition Pulse width modulation strategies are commonly referenced, via,

(i) Alternative phase opposition disposition, where each carrier is phase shifted by π from its adjacent Carrier.

(ii), Phase opposition disposition where the carriers above the sinusoidal reference zero point are π Out of phase with those below the zero point.

(iii) Phase disposition, where all carriers are in phase own purchased power in a way that may be said to meet this definition.

IV- **SIMULATION RESULTS**

A. Simulation Circuit

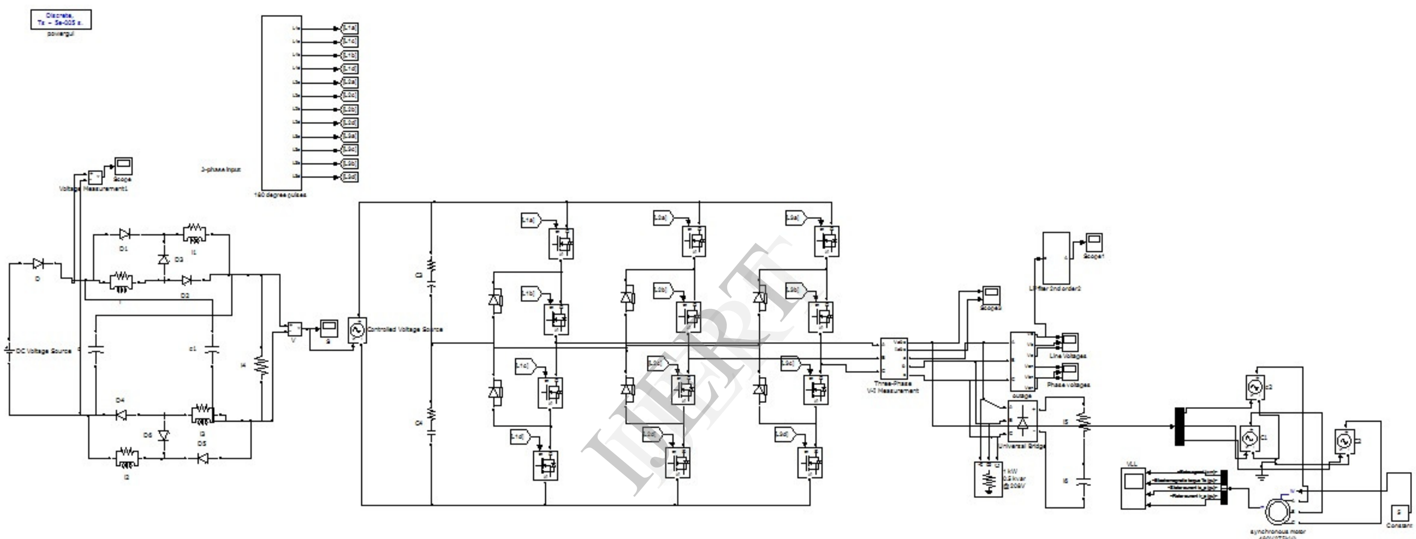

Fig.3. Simulation Circuit for Diode Clamped Z-Source Inverter

Finally, the simulation results of the carrier-based PWM described in using the same parameters as those of the proposed strategy are shown in Figs. 5 and 7, and the total harmonic distortion (THD) of the output line-to-line voltage is compared to that of the proposed strategy. And it can be concluded that the harmonic performance of the proposed strategy is comparable to the carrier-based PWM with zero-sequence voltage injection.

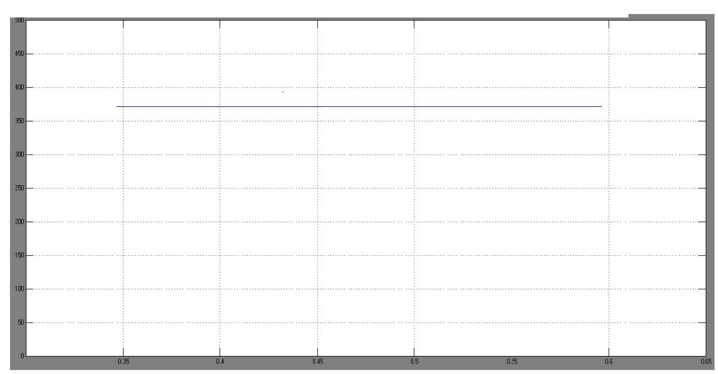

Fig.4. Input Z-Source Waveform

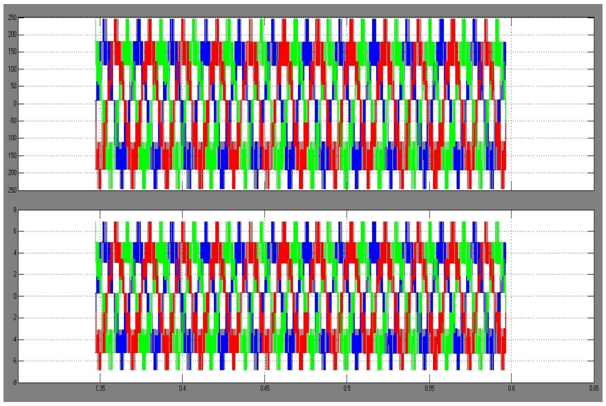

Fig.5. Output Voltage and Current Waveform

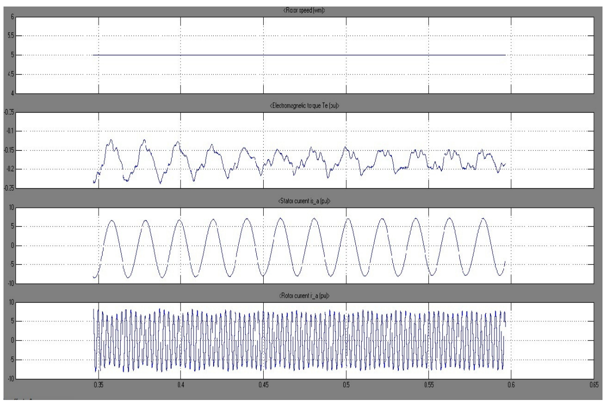

Fig.6. Motor Ratings Waveforms

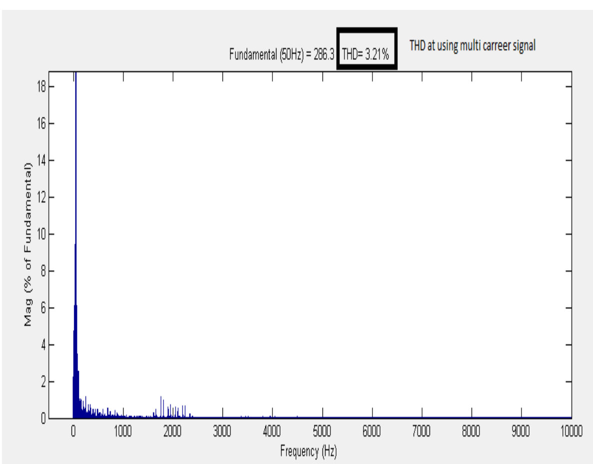

Fig.7. THD Analysis Waveform

The THD Analysis of Output Voltage can be determined by the simulation. The main advantage of this project is harmonic reduction. The THD analysis of the output voltage is 3.21%. When compared to other topology it has better harmonic reduction properties.

V- CONCLUSION

By referring to the project objectives, this project has been successful. This project mainly focuses on the study of Z source inverter and simple boost switching control method. The circuit has been designed based on the standard Z source inverter and simulated using MATLAB. The theoretical values have been calculated and the simulation results were gained through MATLAB simulations. The simulation results were almost similar to the calculated values both the output voltages and voltage stress. The output voltage also can be buck or boost depends on the requirement of the electronic or electrical power applications. However, for simple boost switching technique, the modulation index can only be in the range of zero and one. Thus, since the output voltage directly depending on the modulation index, the output voltage has been limited to a certain range for the Z source inverter instead of zero to infinity. From the results and progress throughout the project, Z source inverter has overcome the barrier of traditional inverters. The barrier is to produce AC output waveforms that are greater than the DC input sources. The project also can conclude that the simple boost switching control method still needs some improvement since the voltage stress is high. This makes the inverter demanding a very good switch for inverter operation.

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