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THD Minimization Based Asymmetrical Cascade Multilevel Inverter with Different Modulation Techniques

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***Abstract*— In this paper mainly focused on the implementation of novel topology in a series connection of battery voltages in 9-level asymmetrical cascaded multilevel inverter (ACMLI) help to reduced the total harmonic distortion (THD) output level and higher the number of different level generated. Multilevel inverters have unique structure which makes it possible to reach high voltages with less harmonic content and lower EMI. The harmonic content of the output voltage waveform decreases as the number of output voltage increases. This requires less number of components, and gate drive circuit as compared to other multilevel inverters. The paper presents of different types of modulation techniques based multicarrier level shifted pulse width modulation (PWM) and Finally simulation results of asymmetrical cascaded seven-level multilevel topology are carried out using MATLAB/simulink R2013a software version.**

Keywords*— Conventional multilevel-level inverter (MLIs), asymmetrical cascaded multilevel topology and PWM techniques.

I. INTRODUCTION

In the last few years, the power quality necessity of increasing in industry has the continuous development of voltage source multilevel inverter due to high efficiency with high switching frequency control method in the recent literatures [1-3]. Power electronics research in field has finding solutions in fields such as series and parallel connection of switches, multilevel inverter topologies, inverter reliability, modulation techniques and other. Three different basic multilevel- inverter are commonly used, the neutral point diode clamped multilevel inverter (DCMLI), flying capacitor inverter (FCMLI) and cascading h-bridge multilevel inverter (CHBMLI) literatures [4].

DCMLI method can applied lower to higher level converter [5]. The minimum harmonic distortion, the steps are more output voltage or current waveform, producing a sinusoidal wave with as the number of level increases [6]. More level also mean higher voltages can be series devices, voltages sharing problems without devices, a zero total harmonies distortion of the output voltage waveform can be obtained by an infinite numbers of level. The capacitor clamped inverter alternatively known as flying. The FCMLI involves series connection of capacitor was proposed by Meynard and Foch in 1992. The structure based flying capacitor is similar to that of the diode-clamped inverter except that instead of using clamping capacitor clamped switching cells. where the voltage on each capacitor different from that of the next capacitor [7].

Fig. 1 shows the representation of one phase leg of inverters for different levels in, and power semiconductors is represented by an ideal switch with several positions [8].

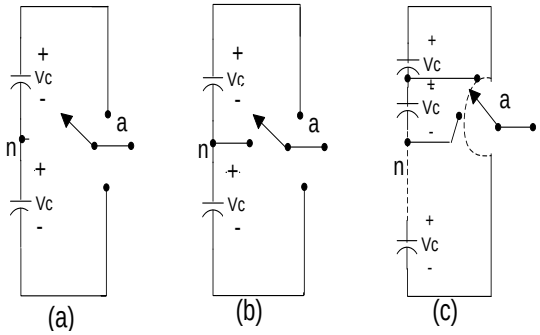

Fig. 1. one phase leg of inverter (a) two level (b) three level (c) n-levels

The symmetric cascading h-bridge MLI are use of equal voltage sources and cascading inverter per phase are 2N+1 level produced in output of phase voltages. Each cell of the h-bridge needs a separate DC-source [9]. They are arrangement of three-phase and single-phase cascading multilevel inverter. The number of voltages level increase when the cascading-cell DC supply voltages from a ratio-3 geometric sequence.

Asymmetrical cascading h-bridge inverter (ACHBI) based DC-supply voltages are unequal. This topology consist increase number of level of output voltage with reduced total THD and switching losses. ACHBI will be high efficiency up to 80% at fundamental frequency and voltage level of load terminals of (2^{N+1} - 1), N is number of DC-source [10]. ACHBI provided the large number of output voltage without number of increasing DC voltage source.

This paper presents a reduced devices topology for single-phase asymmetrical cascading multilevel inverter with a high number of even and odd steps. The cost and voltage installation area are the number of switches (IGBTs) will be reduced. The magnitudes of the utilized DC supplies have been selected in such a way that brings the high number of output voltage level increases with an effective application of PWM modulation techniques. Different modulation techniques have been employed, which are sinusoidal PWM. The proposed work is presented in five steps [11]. The first step focuses on the research advances in developing DCMLI, FCMLI and CHBLI topologies. In second step, the presents topology is well explained in terms of working principles, voltage step and DC supply selection. Third step brings out the

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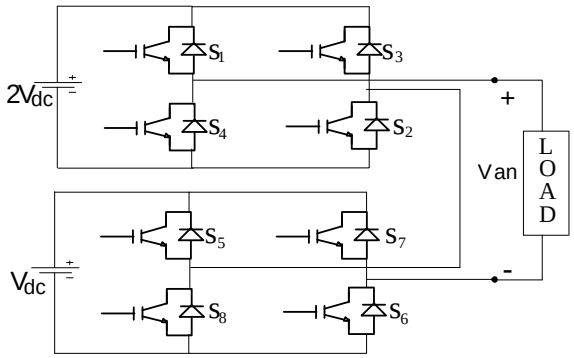
deployed modulation- techniques in detail. Forth step has been obtained the simulation results. The different control techniques based level shifting applied the proposed topology, with comparison between the proposed topology and the conventional inverter [12]. In fifth step, the proposed configuration determination of DC output voltage level are compared with other modulation techniques.

II. PROPOSED TOPOLOGY

Fig.2 and Fig.3 shows basic structure of proposed topology. A single-phase 7 and 9-level asymmetrical cascaded MLI. In this figure, the left side circuit generates the required output level is called output level generator. The proposed ACMLI topology for 9-level inverter requires eight semiconductor switches and two isolated dc sources shown in Fig.3 [13].



III. OPERTION OF THE PROPOSED TOPOLOGY USING 9-LEVEL ACMLI

Operation of the proposed 9-level MLI with ACMLI topology can be easily explained with the help of Fig. 3 and table I. When switches S5, S6, S4 and S2 are turned "on" the output voltage will be "Vdc" (i.e., level 1). The output voltage will be "2Vdc" (i.e., level 2) when switches S1, S2, S7 and S8 are turned "on". When S1, S2, S6 and S8 switches are turned "on" the output voltage will be "3Vdc" (i.e., level 3). When switches S1, S2, S5 and S6 are turned on the output voltage will be "4Vdc" (i.e., level 4). When switches S2, S4, S6 and S8 are turned "on" the output voltage is zero (i.e., level 0). When switches S7, S8, S4 and S2 are turned "on" the output voltage will be "-Vdc" (i.e., level -1). The output voltage will be "-2Vdc" (i.e., level -2) when switches S3, S4, S5 and S6 are turned "on". When S3, S4, S6 and S8 switches are turned "on" the output voltage will be "-3Vdc" (i.e., level -3). When switches S3, S4, S7 and S8 are turned on the output voltage will be "-4Vdc" (i.e., level -4).

The operation of this topology can also be easily understood by mode of operation of single-phase 9-level AC MLI shown in Fig. 4. Each voltage source "Vdc" is required 100V and 300V. There are nine sufficient switching modes in generating the multistep level for a 9-level MLI.

Voltage level	Switch State								Output Voltage
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	
4	1	1	0	0	1	1	0	0	$4V_{dc}$
3	1	1	0	0	0	1	0	1	$3V_{dc}$
2	1	1	0	0	0	0	1	1	$2V_{dc}$
1	0	1	0	1	1	1	0	0	V_{dc}
0	0	1	0	1	0	1	0	1	0
-1	0	1	0	1	0	0	1	1	$-V_{dc}$
-2	0	0	1	1	1	1	0	0	$-2V_{dc}$
-3	0	0	1	1	0	1	0	1	$-3V_{dc}$
-4	0	0	1	1	0	0	1	1	$-4V_{dc}$

Fig. 2. 7-level asymmetrical cascasded multilevel inverter.

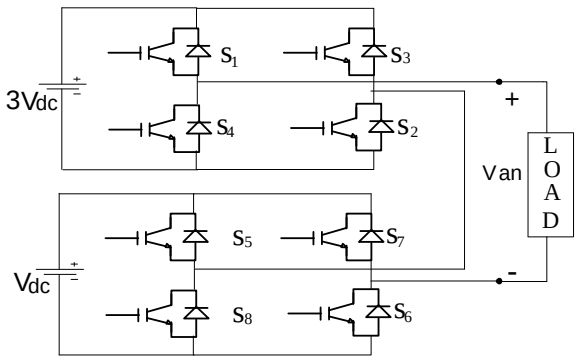


Fig. 3. 9-level asymmetrical cascaded MLI.

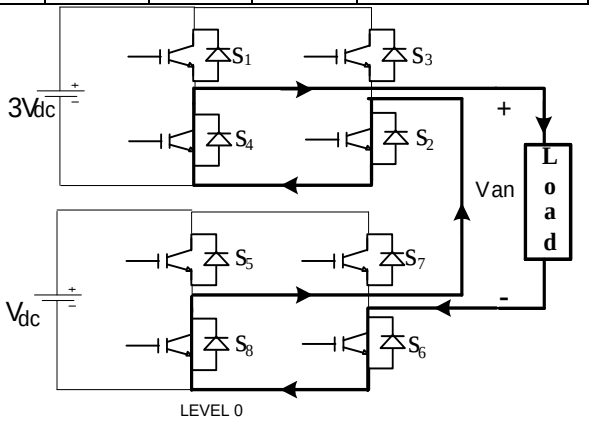


Fig. (a)

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TABLE I. MODE OF OPERATION 9- LEVEL ACMLI.

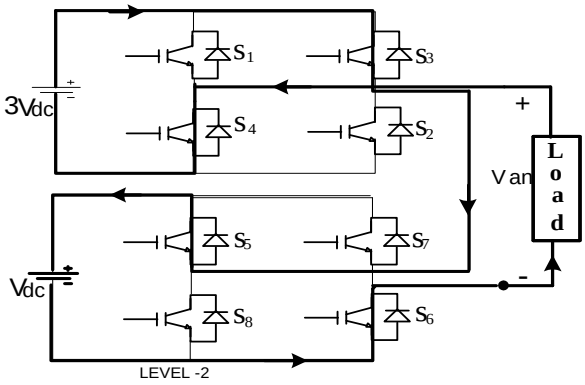

FIG. (B)

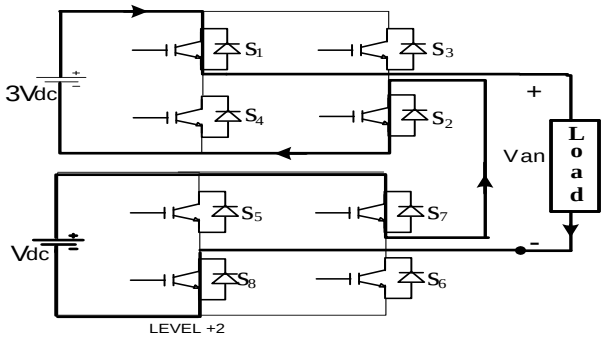

Fig. (c)

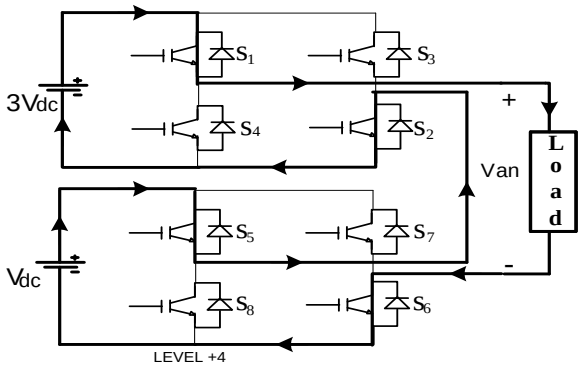

Fig. (d)

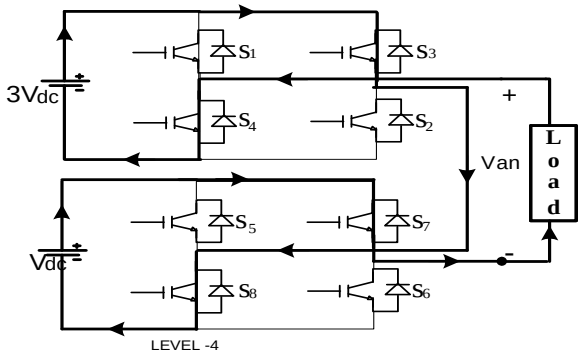

Fig. (e)

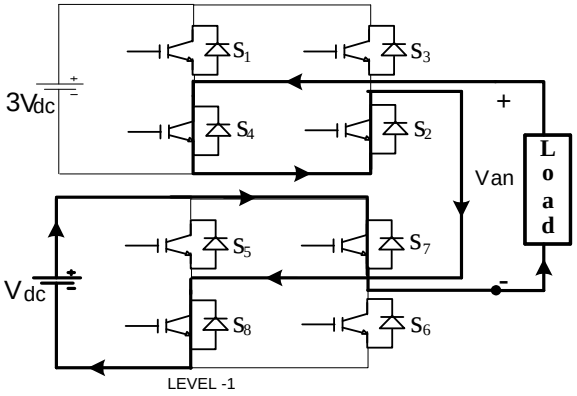

Fig. (f)

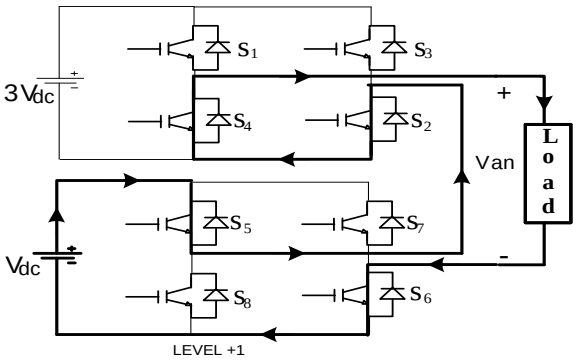

Fig. (g)

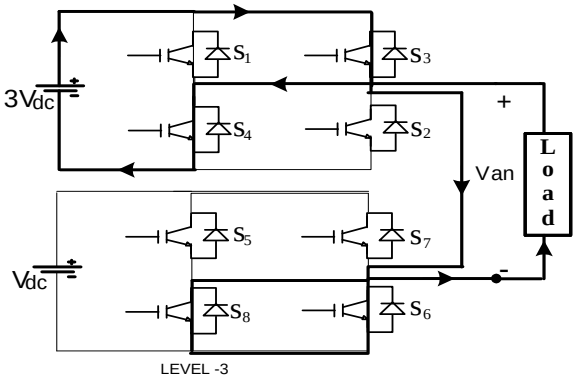

Fig. (h)

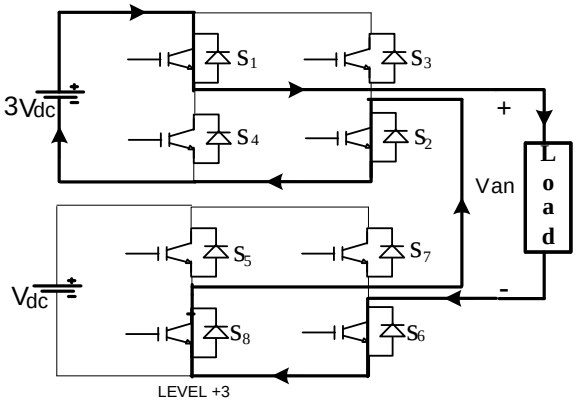

Fig. (i)

Fig. 4. Fig (a), Fig (b), Fig (c), Fig (d), Fig (e), Fig (f), Fig (g), Fig (h), and Fig (i) are Switching combination of 9-level ACMLI.

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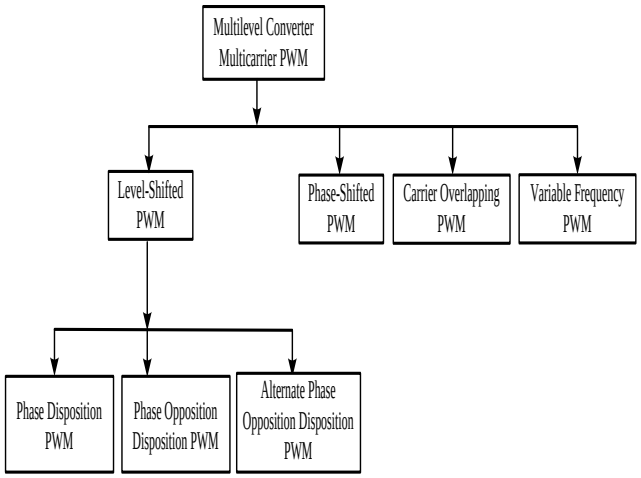
IV. MODULATION STRATEGIE



There are four different pulse width modulation strategies as given below [14-16].

A. Phase disposition pulse width modulation (PD PWM)

In this pulse width modulation strategy, each and every carrier waveforms are in same phase shown in Fig.3 for 5-level MLI. For discus 7-level inverter, 6 triangle carriers are used.

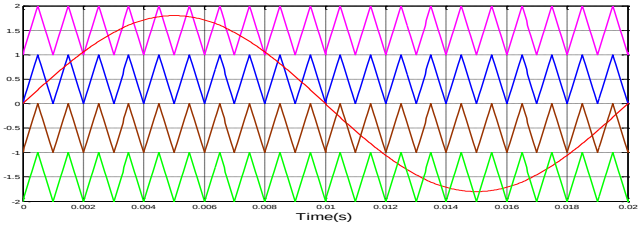


Fig. 5. Carrier arrangement for PDPWM strategy (ma=0.9 and mf=20)

B. Phase opposition disposition pulse width modulation (POD PWM)

In this PWM strategy, every carrier waveforms above zero reference are in phase and below zero reference are 1800 out of phase as shown in Fig.4 For discuss 7-level inverter 6 triangle carriers are used.

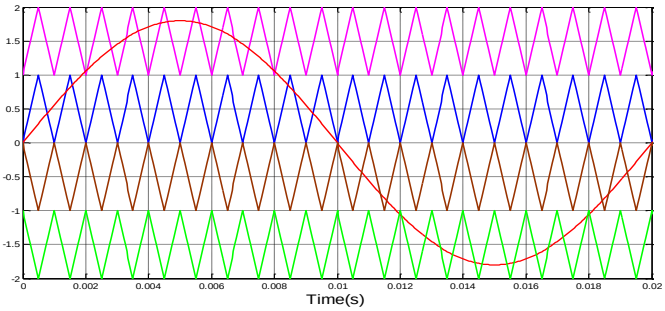


Fig. 6. Carrier arrangement for PODPWM strategy (ma=0.9 and mf=20)

C. Alternate phase opposition disposition pulse width modulation (APOD PWM)

In PWM strategy where every carrier waveform is in out of phase with its neighbour all carrier by 1800. Shown in Fig.5.

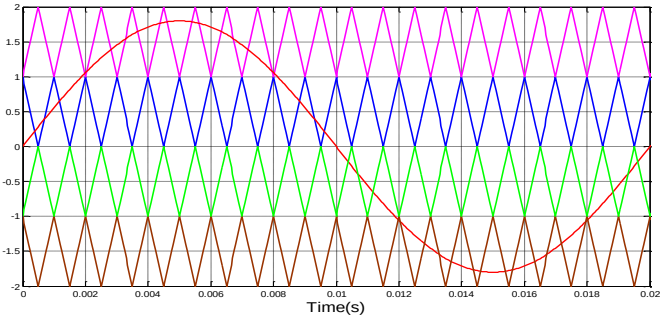


Fig. 7. Carrier arrangement for APODPWM strategy (ma=0.9 and mf=20)

D. Phase-shifted pulse width modulation (PS PWM)

Fig.6 shows the carrier pulse width modulation strategy. A carrier phase shifted PWM for multi-level inverter is used to produced the stepped multi-level output voltage waveform with lower % THD. Multilevel inverter with N levels requires (N-1) triangular carriers. In phase shifted PWM, all the triangular carriers have same frequency.

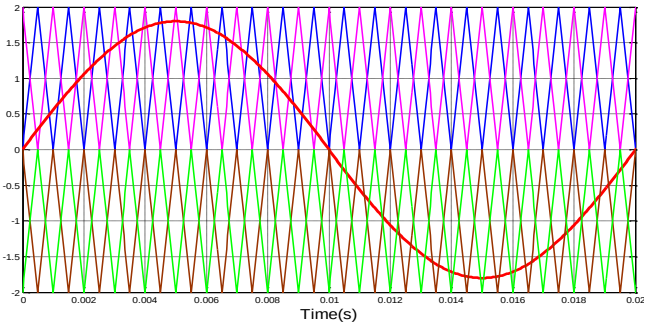


Fig. 8. Carrier arrangement for PSPWM strategy (ma=0.9 and mf=20)

V. SIMULATION RESULTS

The Fig. 9 and Fig. 10 shows the proposed topology model of single-phase asymmetrical 9-level and 7-level MLI. Table II shows THD comparison between different PWM techniques. The simulation parameters are as following R = 5 ohms, L = 5mH, and dc source voltage is 400V; Carrier signal frequency is 2 kHz. shown in Fig. 11. (a) – (d). The harmonic spectrum is carried out by using the FFT analysis in MATLAB/Simulink.

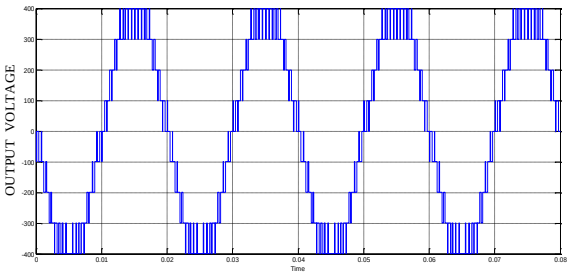


Fig. 9. Proposed single-phase 9-level ACMLI with R-L load

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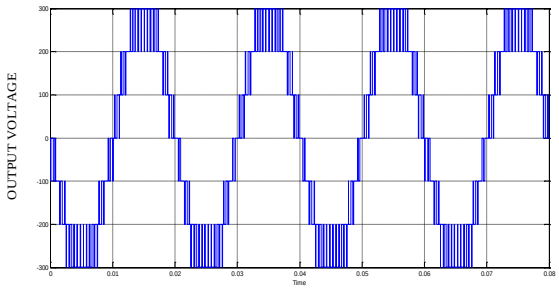
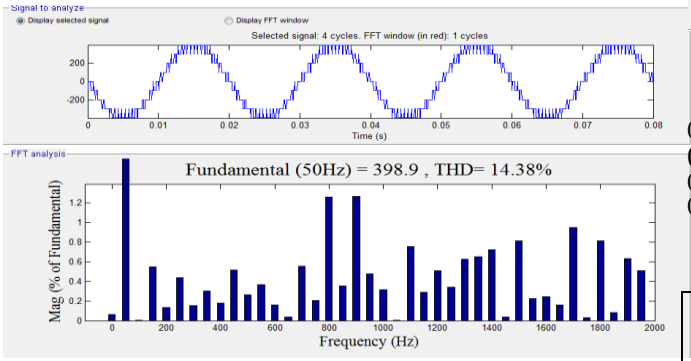
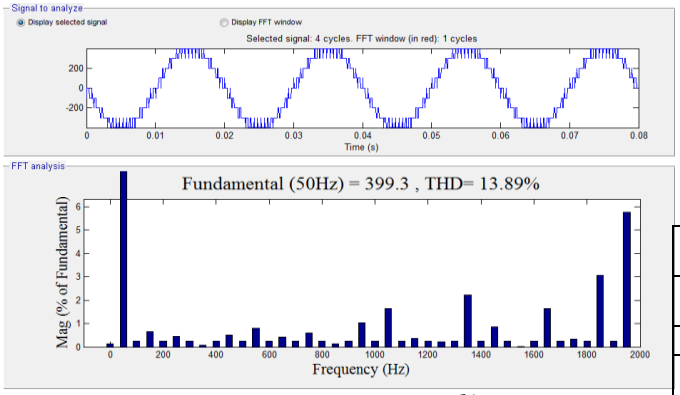


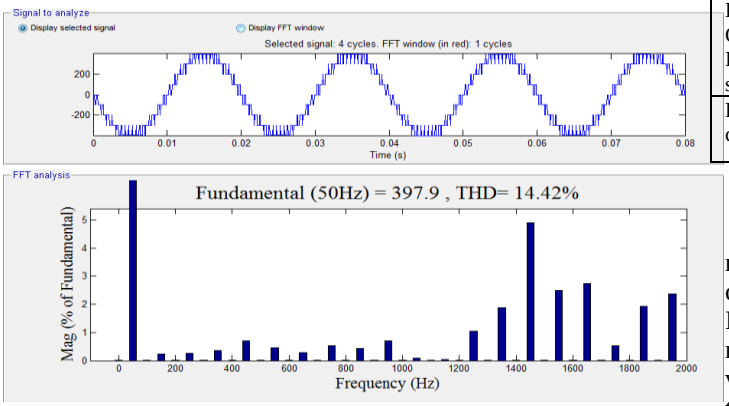
Fig. 10. Proposed single-phase 7-level ACMLI with R-L load



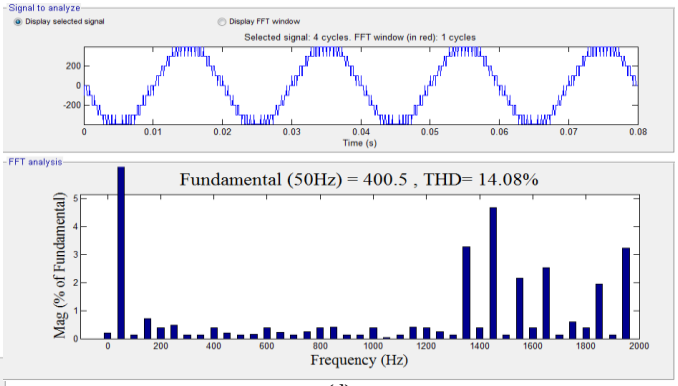
(a)



(b)



(c)



(d)

Fig. 11. FFT analysis for R-L load (Ma=0.9, Mf=20)

(a) Phase disposition pulse width modulation (PDPWM)
(b) Phase opposition disposition pulse width modulation (POD PWM)
(c) Alternate phase opposition disposition pulse width modulation
(d) Phase shifted pulse width modulation (PSPWM)

TABLE II. THD ANALYSIS B/W DIFFERENT PWM TECHNIQUES FOR 9-LEVEL ACMLI

Modulation Index	PS PWM %THD	PD PWM %THD	POD PWM %THD	APOD PWM %THD
1.1	11.89	12.64	11.93	13.19
1	14.08	14.38	13.89	14.42
0.9	17.25	17.13	17.04	16.89
0.8	17.84	17.71	17.90	17.46

TABLE III. COMPARISON BETWEEN DIFFERENT 9-LEVEL MULTILEVEL INVERTER TOPOLOGIES

Inverter type	NPC	Flying capacitor	CHB	Proposed ACMIL
Main switches	16	16	16	8
Main diodes	16	16	16	8
Clamping diodes per phase	56	0	0	0
DC bus Capacitor/ Isolated supplies	8	8	4	2
Flying capacitors	0	28	0	0

VI. CONCLUSIONS

In this paper, a presented topology for asymmetrical 9-level multilevel inverter with different PWM techniques. This is composed of the series connection of sub-multilevel inverters. In this topology presented with less number of switches and reduced percentage THD with less number of level output voltage. Proposed MLI topology with different PWM techniques is used to generate 9-level output phase voltage. The result of proposed topology is reducing installation area and cost. The presents topology was simulated and Harmonic analysis carried out using Mat Lab R2013a version software. Single-phase 9-level MLI improve the efficiency of system compare with different conventional topologies. The future may include an extension to four-wire loads with space vector PWM and other modulation techniques.

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