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THD Analysis for 3-Phase 5-Level Diode Clamped Multilevel Inverter Using Different PWM Techniques

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Abstract

Multilevel inverter technology has emerged recently as a very important tool to extend the high power applications with high voltage capability, low switching losses, good power quality and good electromagnetic compatibility (EMC). This report gives the variations of THD of three phase five level diode clamped multilevel inverter (DCMLI) fed three phase Induction motor drive using different sinusoidal PWM techniques. Since sinusoidal PWM is the switching technique which is commonly used in industrial applications over decades, the various Pulse width modulation techniques used in this report are 1) Variable Frequency PWM (VFPWM) 2) Carrier Over Lapping PWM (COPWM) 3) Phase Shift PWM (PSPWM).

Analytical solutions of PWM strategies for multilevel inverters (MLI) are used to identify the Current THD for various carrier frequencies for all the three PWM techniques Also the phase voltages, phase currents, line voltages, speed v/s time and torque v/s time graphs are also enumerated. The results described in this paper are based on MATLAB-SIMULINK. The output waveforms in the proposed PWM multilevel inverter are investigated thoroughly. It is concluded from the output waveforms that THD is least pronounced in PSPWM.

Key terms: MLI, PWM, COPWM, VFPWM, PSPWM, MATLAB, EMC, multilevel inverter.

1. Introduction

The concept of multilevel inverters (MLI) does not depend on just two levels of voltage to create an a/c signal. Instead several voltage levels are added to each other to create a smoother waveform with lower dv/dt and lower harmonic distortion. Multilevel inverters have become more popular in recent years in high power electric application with the promise of less disturbance and possibility to function at lower switching frequency than ordinary two-level inverters.

The term multilevel inverter starts with the three-level inverter introduced by Nabae et al. [1]. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. However, as high number of levels increases the control complexity and introduces voltage imbalance problems.

The most attractive features of multilevel inverters are as follows.

1. They can generate output voltages with extremely low distortion and lower dv/dt.
2. They draw input current with very low distortion
3. They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods [2].

4. They can operate with a lower switching frequency.

The recent applications of MLIs includes AC motor drives, active rectifiers, filters, interface of renewable energy sources, flexible AC transmission systems (FACTS), and static compensators. The diode clamped inverters, particularly the three-level structure, have a wide popularity in motor drive applications besides other multilevel inverter topologies. However, it would be a limitation of complexity and number of clamping diodes for the DC-MLIs, when the level exceeds three [3], [4], [5], [6].

Conventionally, to generate gate pulses, Triangular wave as a carrier signal is compared with sinusoidal wave, whose frequency is desired frequency. In this paper our main interest is to observe the variation of THD in three phase five level diode clamped multilevel inverter fed three phase induction motor using various PWM techniques with the help of MATLAB-SIMULINK

2. Multilevel Inverters

Multilevel inverters have become the enabling power conversion technology for high voltage, high power applications in today's power grids, transportation systems, and industrial motor drives. The multilevel concept was established in the early 1990s when the diode-clamped multilevel inverter, the capacitor-clamped (or flying capacitor) multilevel inverter, and the cascade multilevel inverter were proposed.

For example, many STATCOMs (a voltage and reactive power control device) based on the cascade multilevel inverter have been installed in power grids around the world. Finally, we will summarize that our multilevel inverter research highlights the analysis of total harmonic distortion in 3-phase 5-

level diode clamped multilevel inverter fed three phase Induction Motor using various pulse width modulating techniques. Figure 1 shows the one leg of five level diode clamped Multi Level Inverter.

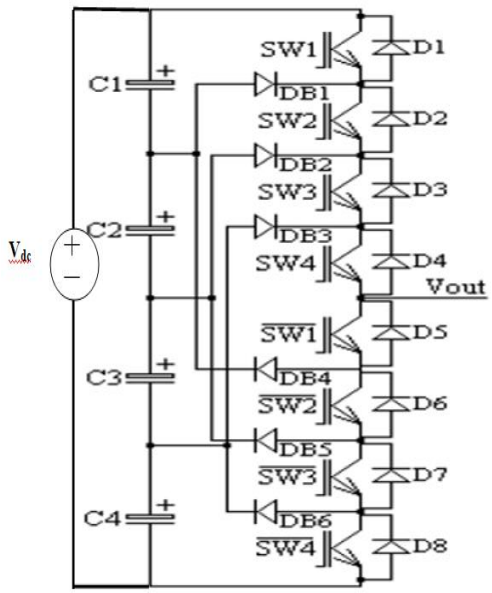

Figure 1. One leg of five level Diode clamped Multi Level Inverter

3 Modulation techniques

Modulation is the technique or process in which the characteristics of the carrier wave or signal such as amplitude, frequency and phase are changed in accordance with the instantaneous value of the original or message signal. The technique of superimposing the message signal on the carrier wave is called MODULATION. Modulation techniques are of two types they are continuous wave modulation and pulse modulation.

1. CONTINUOUS WAVE MODULATION: When the carrier wave is a continuous in nature, the modulation is known as continuous wave modulation or analog modulation.

Examples:- (a)Amplitude modulation (b)Angle modulation (c)Frequency modulation (d) Phase modulation

2. PULSE MODULATION: When the carrier wave is a pulse type waveform, the modulation process is known as pulse modulation. Examples: - (a) pulse amplitude (b) pulse width (c) pulse code

3,1Sinusoidal Pulse Width Modulation (SPWM)

In this method of modulation, several pulses per half cycle are used as in case of Multiple Pulse Modulation (MPM). In MPM, the pulse width is equal for all the pulses. But in SPWM the pulse width is a sinusoidal function of the pulse in a cycle.

The main principle of Sinusoidal Pulse Width Modulation is to compare many triangular carrier signals with one modulating Sinusoidal signal. For five level inverter, four triangular carriers are needed, which is shown in Figure 2. In General if m-level inverter is used, then (m-1) carrier signals are needed. The carrier signals will have same frequency f_c and same peak to peak amplitude A_c .At every instant sinusoidal signal at desired frequency is compared with each carrier signal at high frequency. In this comparison if modulating signal is greater than triangular carrier signal, then signal is given to appropriate semi-conductor switch in respective legs.

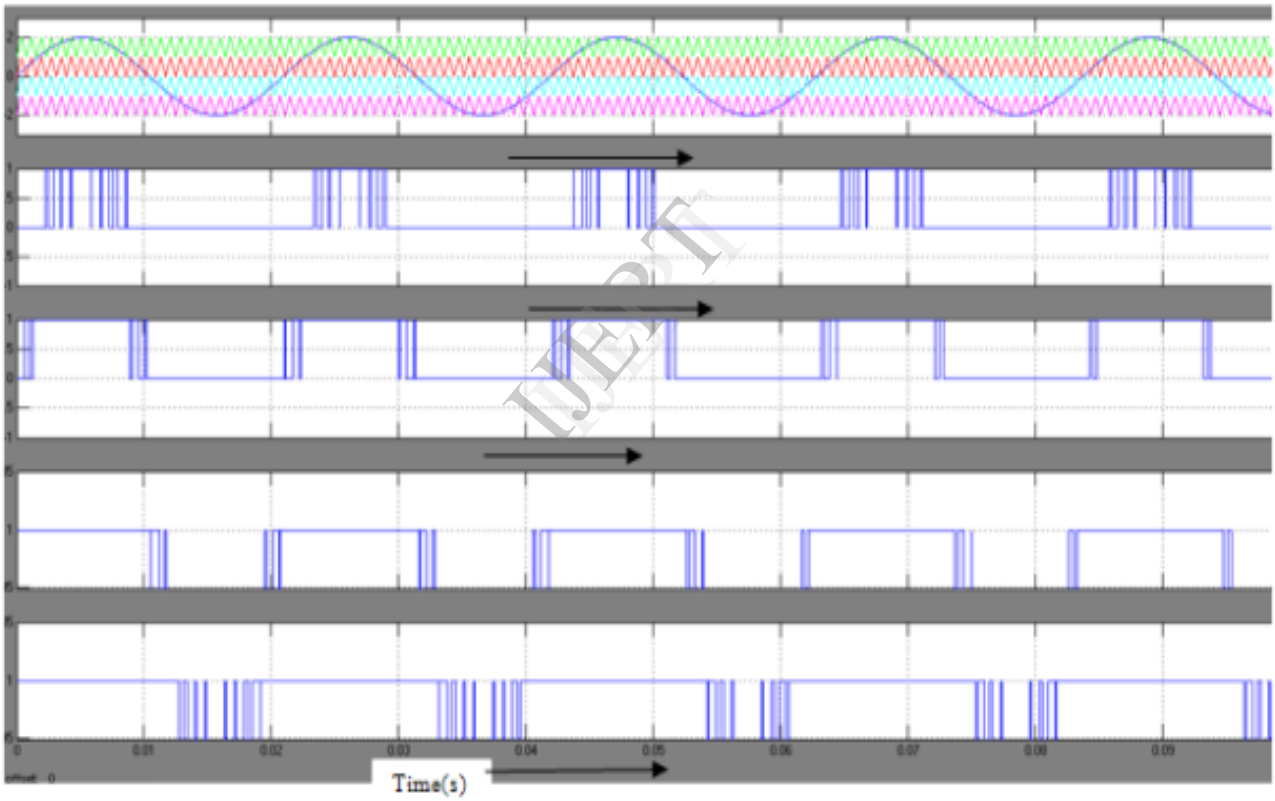

Figure 2. a) SPWM Technique –Carrier signals b) pulses to SW1 c) pulses to SW2 d) pulses to SW3 e) pulses to SW4

4 Multicarrier PWM strategies

Multicarrier PWM strategy is the widely adopted modulation strategy for MLI. It is similar to that of the sinusoidal PWM strategy except for the fact that several carriers are used. Multicarrier PWM is one in which several triangular carrier signals are compared with one sinusoidal modulating signal. The number of carriers required to produce m-level output is m-1. All carriers have the same peak to peak amplitude ac and same frequency fc except for variable frequency PWM.

The reference waveform has peak to peak amplitude of Am and a frequency fm. The reference is continuously compared with each of the carrier

signals and whenever the reference is greater than the carrier signal, pulse is generated. There are many carrier arrangements to implement the PWM strategies. In this work the following strategies were carried out.

1. Carrier overlapping PWM strategy (COPWM).
2. Variable frequency PWM strategy (VFPWM).
3. Phase shift PWM strategy (PSPWM).

4.1 Carrier Overlapping PWM (COPWM) Strategy

In COPWM strategy shown in Figure 3, for an m-level inverter using carriers with the same frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they occupy are overlapping each other; the overlapping vertical distance between each carrier is $A_c/2$. The reference waveform has amplitude A_m and frequency of F_m and is centred in the middle of the carrier signals. The frequency ratio (m_f) and modulation index (m_a) are defined in carrier overlapping method as follows

1. Frequency ratio (m_f) = f_c/f_m
2. Modulation index (m_a) =$A_m/(m/4)*A_c$

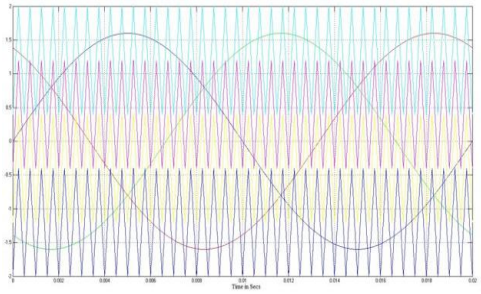

Figure 3. Carrier arrangement for COPWM strategy

4.2 Variable frequency PWM (VFPWM)

The number of switchings for upper and lower devices of chosen MLI is much more than that of intermediate switches in Sub-harmonic PWM using constant frequency carriers. In order to equalize the number of switching's for all the switches, variable frequency PWM strategy is used as illustrated in which the carrier frequency of the intermediate switches is properly increased to balance the numbers of switching for all the switches. The VFPWM strategy is shown in Figure 4.

Table 1 Variation of Stator current THD with carrier frequency

Carrier frequency (Hz.)	Current THD%	Carrier frequency (Hz.)	Current THD%	Carrier frequency (Hz.)	Current THD%
980	6.66	1320	5.84	1680	5.77
1020	6.13	1380	5.97	1720	5.25
1080	6.03	1420	5.32	1780	5.48
1120	6.15	1480	5.86	1820	5.64
1180	6.28	1520	5.44	1880	5.58
1220	5.73	1580	5.63	1920	5.59
1280	6.32	1620	5.69	1980	5.65

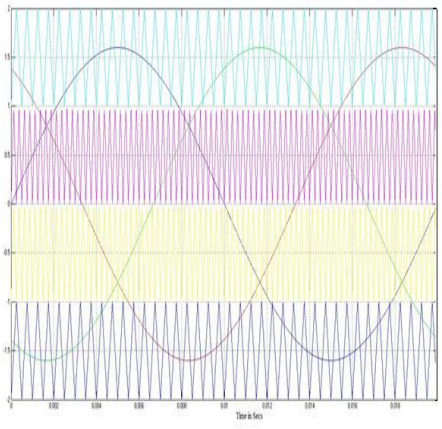

Figure 4. Carrier arrangement for VFPWM strategy

4.3 Phase Shift PWM (PSPWM) Strategy

The PSPWM technique, shown in figure 5, uses four carrier signals of the same amplitude and frequency which are shifted by 90 degrees to one another to generate the five level inverter output voltages. The gate signals for the chosen inverter can be derived directly from the PWM signals (comparison of the carrier with the sinusoidal reference).

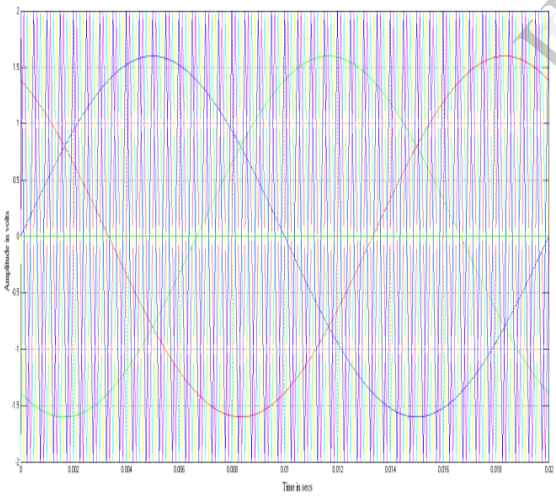

Figure 5. Carrier arrangement for PSPWM strategy

5 Simulation Results

The simulation results obtained for three phase five level diode clamped multilevel inverter fed three phase induction motor drive are given below. The rating of Induction motor is 3Φ, 4500 W, 415 V, 50 Hz

5.1 Simulation Results COPWM Technique

Table 1 shows the variation of stator current THD as the carrier frequency is varied. The carrier arrangement for COPWM technique is shown in figure 6. . Phase Current, Phase Voltage and Line Current are shown in Figure 7, Figure 8 and Figure 9 respectively. Figure 10 gives speed vs time , torque vs. Time is given in Figure 11.

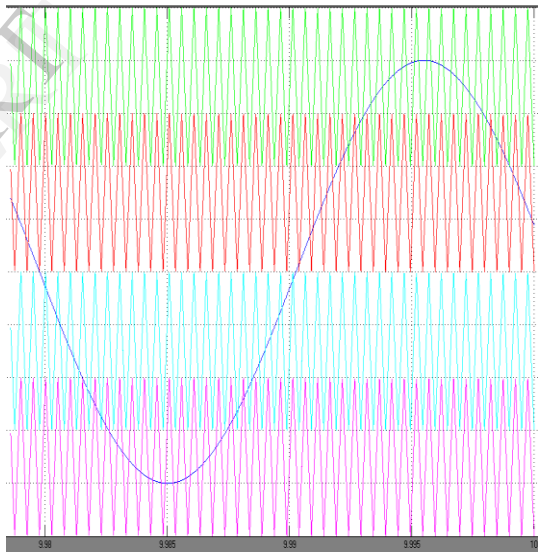

Figure 6. Carrier arrangement for COPWM

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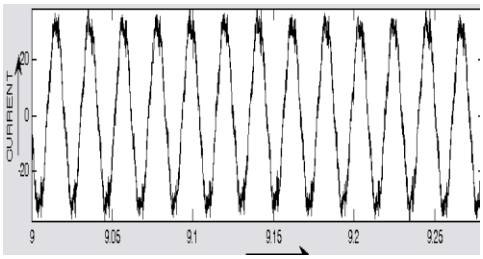


Figure 7. Phase Current Waveform

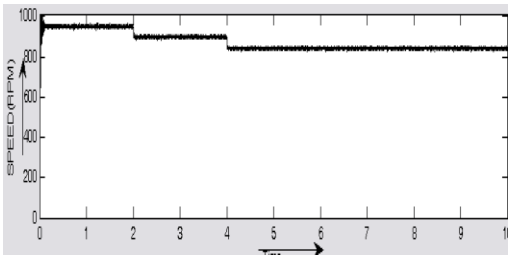


Figure 10. Speed v's Time Plot

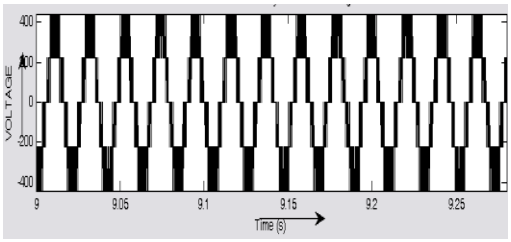


Figure 8.Phase Voltage Waveform

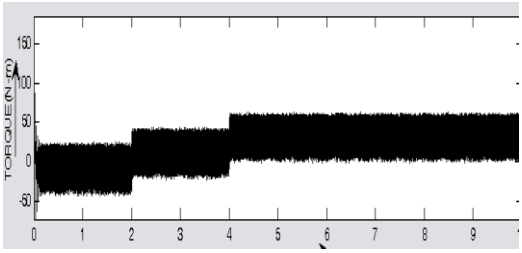


Figure 11. Torque v's Time Plot

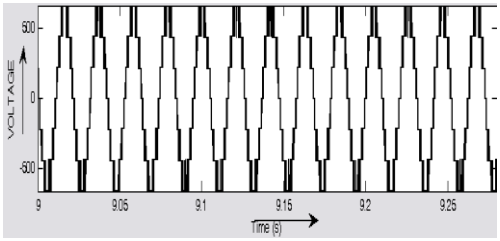


Figure 9. Line Voltage Waveform

5.2 Simulation Results for VFPWM Technique

Table 2 shows the variation of stator current THD as the carrier frequency is varied. The carrier arrangement for VFPWM technique is shown in figure 12. Phase Current, Phase Voltage and Line Current are shown in Figure 13, Figure 14 and Figure 15 respectively. Figure 16 gives speed vs. Time and torque vs. Time is given in Figure 17

.

Table-2
Variation of Stator Current THD with carrier frequency

Carrier frequency (Hz.)	Current THD%	Carrier frequency (Hz.)	Current THD%	Carrier frequency (Hz.)	Current THD%
980	9.12	1320	6.37	1680	6.29
1020	7.86	1380	7.33	1720	6.31
1080	8.30	1420	6.95	1780	6.65
1120	7.81	1480	6.82	1820	6.14
1180	8.07	1520	6.48	1880	**5.71**
1220	6.97	1580	6.42	1920	6.41
1280	7.41	1620	6.51	1980	6.34

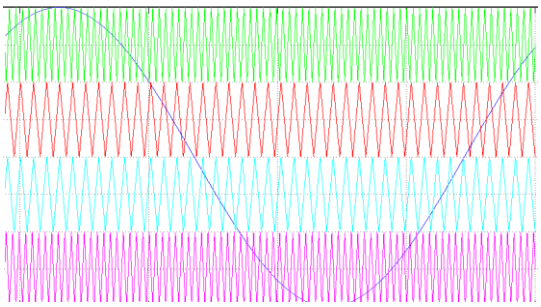


Figure 12. Carrier arrangement for VFPWM

Figure 14. Phase Voltage Waveform

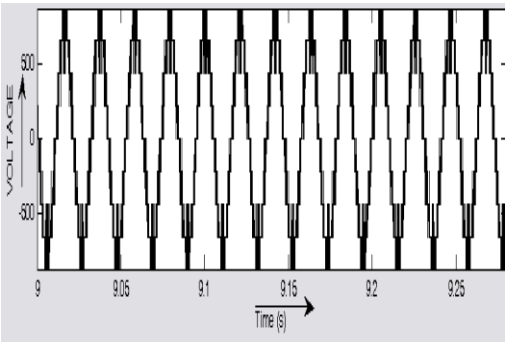


Figure 15. Line Voltage Waveform

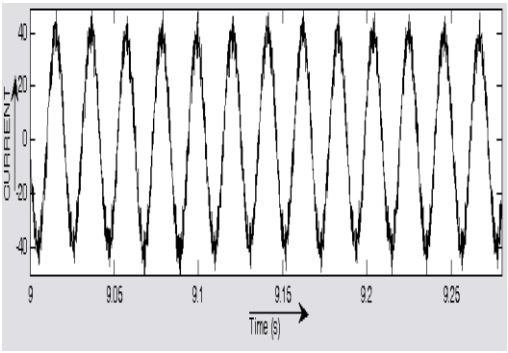
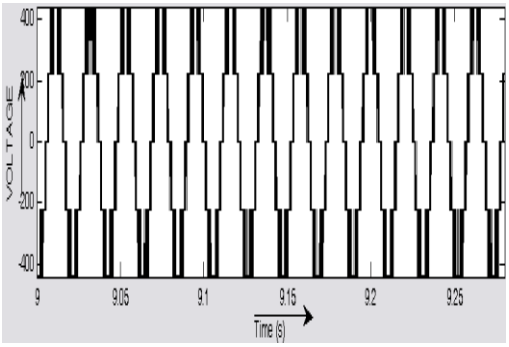


Figure 13.Phase Current Waveform



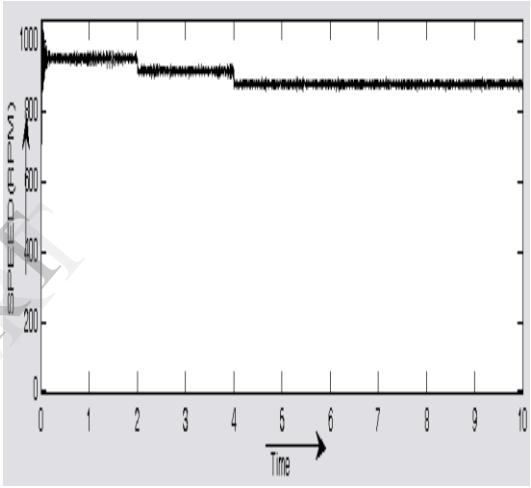


Figure 16. Speed vs. Time Plot

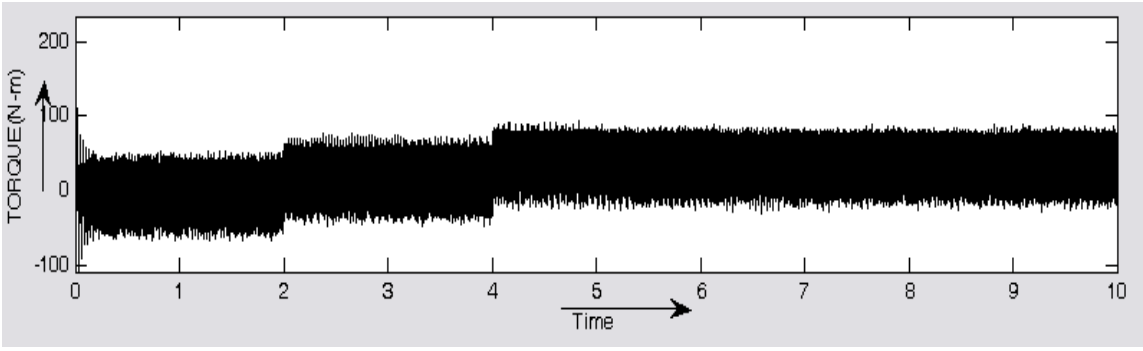


Figure 17. Torque vs. Time Plot

5.3 Simulation Results for PSPWM

Table 3 shows the variation of stator current THD as the carrier frequency is varied. The carrier arrangement for PSPWM technique is shown in figure 18.. Phase Current, Phase Voltage and Line Current are shown in Figure 19, Figure 20 and Figure 21 respectively. Figure 22 gives Speed Vs .time plot and torque vs. Time plot is given in Figure 23.

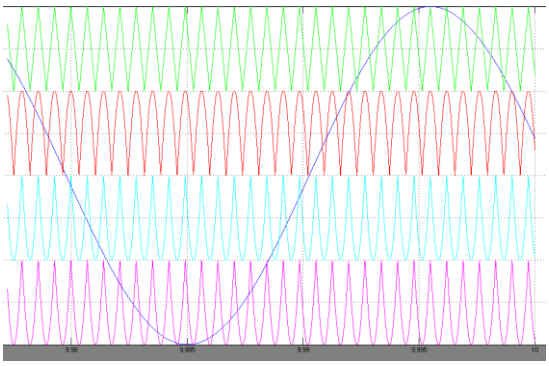


Figure 18 .Carrier arrangement for PSPWWM

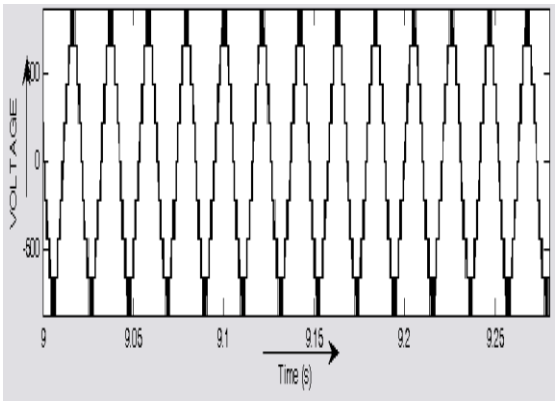


Figure 21. Line Voltage Waveform

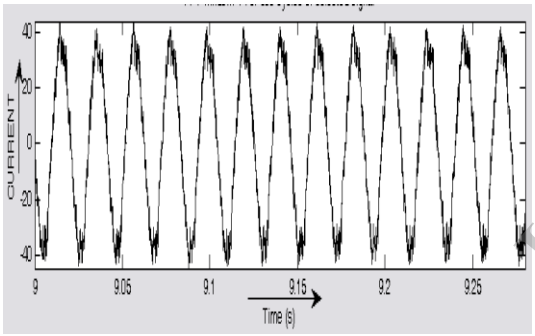


Figure 19 . Phase Current Waveform

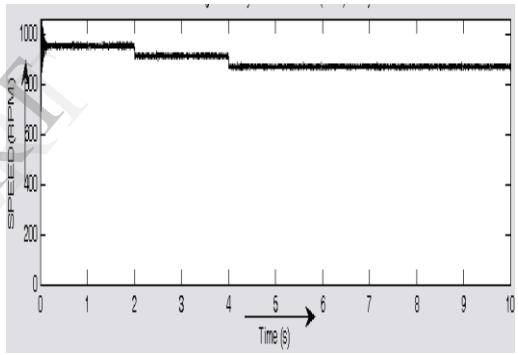


Figure 22. Speed vs. Time Plot

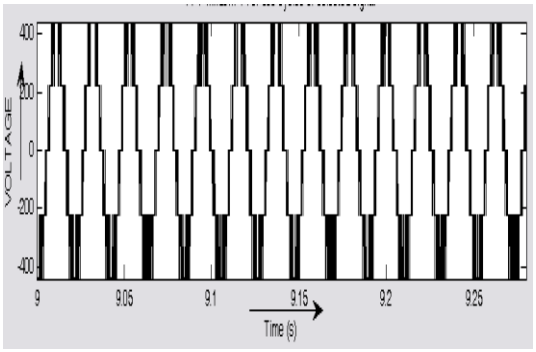


Figure 20 . Phase Voltage Waveform

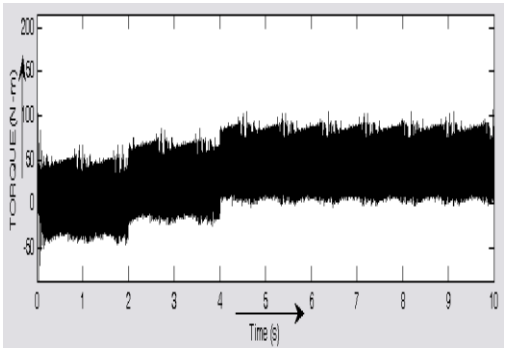


Figure 23. Torque vs. Time Plot

Table-3
Variation of Stator Current THD with carrier frequency

Carrier frequency (Hz.)	Current THD%	Carrier frequency (Hz.)	Current THD%	Carrier frequency (Hz.)	Current THD%
980	7.85	1320	5.96	1680	6.43
1020	6.17	1380	7.15	**1720**	**5.02**
1080	7.99	1420	5.75	1780	6.12
1120	6.27	1480	6.17	1820	5.18
1180	7.31	1520	5.92	1880	5.90
1220	6.86	1580	6.39	1920	5.66
1280	6.95	1620	5.73	1980	5.78

6. Conclusion

As carrier frequency is varied from 980 Hz. to 1980 Hz. it is observed that the output current THD varies between 5.02 % and 9.12 % in all three methods considered. In COPWM technique the minimum THD is 5.25 % at 1720 Hz. and maximum THD is 6.66 % at 980 Hz. in VFPWM technique minimum THD is 5.71 % at 1880 Hz. and maximum being 9.12 % at 980 Hz. While the minimum and maximum THD values in PSPWM techniques are 5.02 % at 1720 Hz. and 7.85 % at 980 Hz. respectively. It is clear from above results that although the range of variation of THD is less in VFPWM, the PSPWM technique is better as the THD is minimum (5.02 %) among all three methods. As the THD should be less than 5 % as per IEEE standards, further methods to be considered in improving THD.

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