Testing Power Reduction in Digital Circuits using Novel X-filling At-Speed Test

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Abstract- **In the modern electronics era, reduction in test power is important to improve battery lifetime in portable electronic devices employing periodic self-test, to improve reliability of testing, and to reduce test cost. In scan-based testing, a significant fraction of total test power is dissipated in the combinational block due to circuit switching activities. In this paper, we present a novel circuit technique to eliminate test power dissipation in combinational logic by masking signal transitions at the logic inputs during scan shifting. When the response to a test vector is captured by state elements in scan based tests, the switching activity of the circuit may be large resulting an abnormal power dissipation and supply current demand. The proposed method accepts a given test set and returns a set of the same or smaller size with reduced switching activity.By analyzing the impact of X-bits on circuit switching activities, we present an novel X-filling technique that can decrease both shift and capture power to guarantees the reliability of scan tests called iFill. Moreover different from prior work on X-filling for shift-power reduction which can only reduce shift-in power, iFill is able to decrease power consumptions during both shift-in and shift-out.**

Index Terms—At-speed scan-based testing, low-power testing, X-filling.

1. INTRODUCTION

1.1 General

The power dissipation of integrated circuits (ICs) inscan-based testing can be significantly higher than that during normal operation. This brings the following problems thatthreaten the reliability of the circuits under test (CUTs).The elevated average power consumption adds to the thermal load that must be transported away from the CUT and can cause structural damage to the silicon, bonding wires, or the package. Another the excessive peak power dissipation is likely to cause a large voltage drop that may lead to erroneous data transfer in test mode only, especially in capture phase of at-speed testing, thus invalidating the testing process and leading to unnecessary test yield loss.

It is likely that a CUT's power rating is violated in both shift mode and capture mode in scan tests. A significant amount of research work has been proposed to address this problem in theliterature, which can be broadly divided into two categories: design-for-testability (DFT)-based solutions and software based solutions. Generally speaking, DFT-based solutions are more effective for test power reduction by introducing dedicated DFThardware to suppress switching acclivities in the CUT. Software-based solutions, on the other hand, usually cannot achieve the sameamount of test power reduction as that of DFT-based solutions, but they do not involve any DFT overhead and can be easily integrated into conventional IC design flow [10].

1.2 Low Power Testing

Reducing power consumption has become an important objective of today's test development process. Prior work in this domain is mainly based on the following techniques: scan chain manipulation, circuit modification, test scheduling, and test cube manipulation. Techniques based on scan chain manipulation are very effective in reducing shift power, but usually do not help in reducing capture power. Reducing test power by modifying the circuit under test has also been proposed by several research groups. This includes clock gating, inserting circuitry between the scan chains and the combinational portion of the CUT to block transitions, scan enable disabling and circuit virtual partitioning. Circuit modification techniques are able to reduce both shift power and capture power, however, usually at a higher design-for-testability (DFT) cost [9].

1.3 X-Filling Technique

The most widely-used software-based solutions for test power reduction, which tries to reduce the CUT's switching activities by filling the don't-care bits (i.e., *X-bits*) in given test cubes intelligently, known as the *X-filling* technique.

By investigating the impact of X-bits on test power consumption, we propose a novel X-filling technique, namely "*iFill*", to reduce both shift- and capture-power during scan tests. In the proposed approach, first, we try to fill as few as possible X-bits to keep the capture-power under the peak power limit of the CUT to avoid test overkills, and then use the remaining X-bits to reduce shift-

power as much as possible to cut down the CUT's average power consumption, so that designers are able to use higher shift frequency and/or increase test parallelism to reduce the CUT's test time and hence cut down the test cost. Moreover, the proposed X-filling technique is able to reduce power consumptions in both shift-in and shift-out processes, thus leading to significant shift-power reduction. Research on low-power scan testing has been focused on

the shift mode, with little or no consideration given to the capture mode power. However, high switching activity when capturing a test response can cause excessive IR drop, resulting in significant yield loss. A novel low-capture-power X-filling method by assigning 0's and 1's to unspecified (X) bits in a test cube to reduce the switching activity in capture mode. This method can be easily incorporated into any test generation flow, where test cubes are obtained during ATPG or by X-bit identification [9].

1.4 Shift- And Capture-Power In At-Speed Scan Tests

As illustrated in Fig.1.1, there are two types of a scan test power, shift power and capture power, corresponding to the two basic scan test operations, shift operation and capture operation, respectively. New test stimuli (*A* in Fig.1.1) are loaded serially in the shift operation, while internal test responses (*B* in Fig.1.1) are loaded into scan flip-flops in parallel in the capture operation [7].

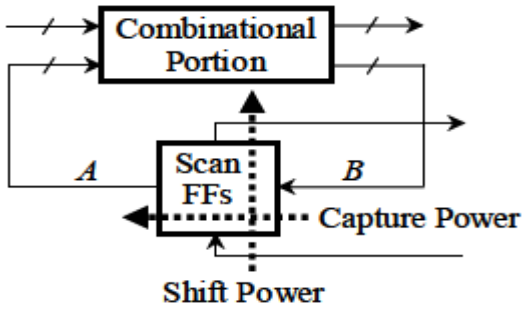

Fig.1.1 Two types scan test power

At-speed tests facilitate to detect speed-related and even un-modeled defects of the CUTs and have been widely accepted in the industry in recent years. As in Fig.1.2, at-speed tests typically involve a long low-frequency shift phase and a short at-speed capture phase. To reduce shift-power dissipation in order not to violate the CUT's power constraint, scan chains are usually shifted at lower frequency.

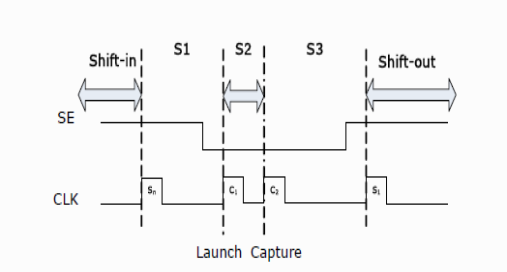

Fig.1.2 Timing diagram of Launch-on-Capture Tests

This strategy, however, may result in high test cost. We therefore should reduce the CUT's shift-power dissipation as much as possible, so that higher shift frequency can be used and/or test parallelism can be enhanced to reduce the testing time [9].

1.5 Impact of X-Bits on Shift- And Capture-Power

Test cube generally contains multiple X-bits, and as many X-bits in the test response are likely to become determined values after filling one single X-bit in the test stimulus, their filling order significantly affects the CUT's test power dissipation. In this the impact of an X-bit on a CUT's shift- and capture-power (namely S-impact and C-impact), and use them to guide the X-filling. Generally, an SFF with larger fan-out logic network involves more circuit transitions. Based on this observation, we model the impact of an X-bit on circuit transitions with its fan-out information only. Compared to the sophisticated method to calculate an X-bit's X-score in, our method does not need to conduct the time-consuming set-simulation and we can target two-pattern at-speed scan tests.

2. BACKGROUND

2.1 Power Consumption in At-Speed Scan-Based Testing

At-speed scan-based tests facilitate to detect speed-related defects of the CUTs and have been widely utilized in the industry in recent years, which typically involve a long low-frequency shift phase and a short at-speed capture phase. There are mainly two types of at-speed scan-based testing approaches: Launch-on-Shift (LoS) and Launch-on-Capture (LoC). LoC scheme is more widely utilized because it does not need the expensive high-speed scan-enable signal required by the LoS scheme. As shown in Fig. 1.2, there are three types of clock signals in LoC scheme: "SCLK" represents the shift clock signal, under which the test vectors are shift-in/out of the scan chains; "ACLK" is the at-speed clock in the CUT to be applied in the capture phase; "TCLK" is the clock signal that the sequential elements on the scan chain will receive, by MUXing "SCLK" and "ACLK" signals. Typically two capture cycles (c1 and c2) are used to detect defects. We denote the initial state of the scan cells and the nodes in combinational portion of the circuit before capture as S1. The first capture c1 launches the state S2 into the CUT, while the second capture c2 store the circuit state S3 after the CUT is applied in functional mode.

2.2 X-Filling for Shift- and Capture-Power Reduction

It has been shown that test cubes for industrial circuits contain as much as 95%-98% X-bits, which can be filled with logic "0" or logic "1" freely without affecting the CUT's fault coverage1. It should also be noted that, even if the given tests are fully specified, the don't-care bits can still be identified with techniques such as the one proposed in [11]. X-filling for shift-power reduction tries to generate fewer differences between adjacent scan cells. The so-called *weighted transition metric (WTM)* was proposed to estimate shift power caused by these logic value differences. That is, the shift power in the the test vector is estimated as follows:

$$\mathrm{WTM}_i = \sum_{j=1}^{N-1} (S_{i,j} \bigoplus S_{i,j+1}) \times j \qquad (2.1)$$

where N is the number of scan cells in the scan chain, represents the logic value of the the scan cell in this test vector.

Wen *et al.* [8] first addressed the lowcapture-power X-filling problem. They mainly considered the transitions at the output of scan flip-flops (SFFs) during X-filling, which, however, does not necessarily have a good correlation with the total capture-power of the whole circuit (i.e., both FFs and combinational gates). Later, in [7], they took the above shortcoming into consideration and introduced a new method to select the X-filling target based on a so-called set-simulation technique, which is proved to be a more effective X-filling method with experimental results on ISCAS'89 circuits.

In [6], Remersaro *et al.* developed an efficient probability- based X-filling technique, called *Preferred fill*, which tries to fill all X-bits in the test cube in one step, instead of using incremental fill and logic simulation. Their technique, however, is inherently less effective as the available information for the probability calculation in their single-step filling is quite limited. Also, only transitions at the SFFs are considered while the transitions at logic gates are ignored in their work.

The above X-filling techniques target either shift-power reduction or capture-power reduction, but not both. This is unfortunate, because filling these unspecified bits has impact on both shift- and capture-power. Because the number of X-bits in test cubes is limited but the objectives are different, low shift-power X-filling techniques may result in high capture-power dissipation, and vice versa. As a result, it is necessary to consider both shift- and capture-power reduction during the X-filling process to gain both satisfied test power result during at-speed scan testing.
Remersaro *et al.* [5] takes a fully specified test set as input and generates a new test set with reduced shift-power and capture- power. The authors first identify X-bits in the test set and then fill 50% of the X-bits using *Preferred fill* [6] while the remaining X-bits are filled next using *Adjacent fill* [3]. However, filling half of the X-bits for capture-power reduction and the other half for shift-power reduction is not a very good strategy. This is because, as discussed previously, the shift-power dissipations and the capture-power dissipation should be dealt with differently. The main objective in shift-power reduction is to decrease the average test power dissipation *as much as possible*; while the main duty in capture-power reduction is to keep it under a safe peak power limit.

3. RELATED WORK

A new X-filling technique to reduce both shift power and capture power during scan tests, namely LSC-filling is proposed [1]. The basic idea is to use as few as possible X-bits to keep the capture power under the peak power limit of the circuit under test (CUT), while using the remaining X-bits to reduce the shift power to cut down the CUT's average power consumption during scan tests as much as possible. In addition, by carefully selecting the X-filling order, our X-filling technique is able to achieve lower capture power when compared to existing methods. The proposed novel X-filling technique to reduce both shift-in power and capture power during scan tests, namely LSC-filling. The basic idea is to use as few as possible X-bits to keep the capture power under the peak power limit of the CUT, while using the remaining X-bits to reduce the shift-in power to cut down the CUT's average power consumption during scan tests as much as possible.

Large test data volume and high test power are two of the major concerns for the industry when testing large integrated circuits. With given test cubes in scan-based testing, the "don't-care" bits can be exploited for test data compression and/or test power reduction. Prior work either targets only one of these two issues or considers reducing test data volume and scanning shift power together [2]. To achieve a capture power-aware test compression scheme, namely CPA-compress is able to keep scan capture power under a safe limit with little loss in test compression ratio.

ICs have been observed to fail at specified minimum operating voltages during structured at-speed testing while passing all other forms of test. Methods exist to reduce power without dramatically increasing pattern volume for a given coverage. The pattern generation approaches are to minimize power consumption that would be used if power-related problems were discovered after design completion. It investigates various heuristics for modifying test content to address power concerns. These techniques require no modifications to the basic design nor its test logic [3]. The proposed method compare the heuristics in terms of the amount of switching reduction, and also the increase in pattern volume and decrease in coverage for a given fault coverage figure of merit.

An automatic test pattern generation (ATPG) technique, which simultaneously reduces capture and shift power during scan testing, is presented [4]. This ATPG performs power reduction during dynamic test compaction so the test length overhead is very small. It has been widely known that circuit power dissipation in test mode is much higher than that in function mode. Since automatic test pattern generation (ATPG) software has made great progress in performance, it is now worthwhile to trade-off ATPG performance for low power. The most important reasons for low-power ATPG are given as follows. First of all, low-power testing avoids the risk of damaging the circuits under test (CUT). In addition, low-power testing enables parallel testing of multiple cores in the system-on-chip (SoC).

The supply current and power dissipation during scan based test may be much higher than during normal circuit operation due to larger switching activity caused by the tests. Higher peak current demands may cause supply voltage droops causing good chips to fail at-speed tests. Higher average switching activity causes higher power dissipation and chip temperature that may cause hot spots and damage circuits under test. Several works have proposed methods to derive tests with lower peak and average switching activity during test response capture or

during scan shifts. Some of these methods require additional hardware and modifications to the scan chains [5]. We investigate a method to derive tests with reduced switching activity both during scan shifts and during test response captures. The method does not require additional hardware or modifications to the scan chains. The proposed method accepts a given test set and returns a test set of the same or smaller size with reduced switching activity.

When the response to a test vector is captured by state elements in scan based tests, the switching activity of the circuit may be large resulting in abnormal power dissipation and supply current demand. High supply current may cause excessive supply voltage droops leading to larger gate delays which may cause good chips to fail tests [6]. This workrepresents a scalable approach called Preferred Fill to reduce average and peak power dissipation during capture cycles of launch off capture delay fault tests. Itavoids the detection of faults during shift cycles. Excessive switching activity is caused by scan tests requiring the circuit under test (CUT) to operate outside of the normal functional operation. Excessive switching activity during the application of scan tests are caused both during scan chain shifts to load tests and unload test responses as well as when
the scan cell contents are updated using functional clocks in what are referred to as capture cycles. Abnormal switching activity causes abnormal peak as well as average power dissipation and supply currents. Excessive power dissipation may cause hot spots that could damage the CUT.

X-filling is preferred for low-capture-power scan test generation, since it reduces IR-drop-induced yield loss without the need of any circuit modification. However, the effectiveness of previous *X*-filling methods suffers from lack of guidance in selecting targets and values for *X*-filling. Both shift and capture power dissipation may have instantaneousimpact. This is because high switching activity at circuit nodes due to the non-functional characteristic of test stimuli and test responses in scan testing may cause excessive IR-drop. Consequently, flip-flop malfunctions and/or timing violations may occur, resulting in significant test-related yield loss. Shift power dissipation may also have accumulativeimpact. This is because high switching activity often lasts for an extended period of time due to a large number of consecutive clock pulses in the shift operation. The shift operation only needs to guarantee that scan chains operate correctly and has nothing to do with ATPG, a wide range of techniques can be fully explored to efficiently reduce shift power [7].

Research on low-power scan testing has been focused on the shift mode, with little or no consideration given to the capture mode power. However, high switching activity when capturing a test response can cause excessive IR drop, resulting in significant yield loss [8]. This method can be easily incorporated into any test generation flow, where test cubes are obtained during ATPG or by X-bit identification. It addressed a new test power reduction problem, i.e. reducing capture power dissipation to avoid yield loss caused by faulted test responses in capture mode. A novel low-capture-power (LCP) X-filling method has been proposed for assigning 0's and 1's to unspecified (X) bits in a test cube in order to reduce the switching activity at FFs and in the circuit for the resulting fully-specified test vector. More evaluations are under way to assess the effect of the LCP X-filling method directly through power consumption instead of switching activity at flip-flops

4. NOVEL X-FILLING

Power consumption during at-speed scan-basedtesting can be significantly higher than that during normal functional mode in both shift and capture phases, which can cause circuits' reliability concerns during manufacturing test. This paper proposes a novel X-filling technique, namely "*iFill*", to address the above issue, by analyzing the impact of *X-bits* on switching activities of the circuit nodes in the two different phases. In addition, different from prior X-filling methods for shift-power

reduction that can only reduce shift-in power, our method is able to cut down power consumptions in both shift-in and shift-out processes

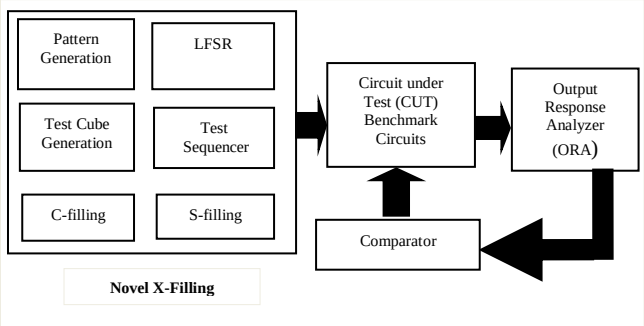

Fig.4.1 Novel X-filling block diagram

The above Fig.4.1 illustrates the block diagram of novel X-Filling to reduce the both capture and shift power. A detailed description of all the modules present in the block diagram is given below.

4.1 Test Vector Generation

The test vector generation produces a set of test vectors that include the inputs, expected outputs, and requirement traceability link. These vectors are generic in that the inputs and expected outputs are based on the names from the model. Users often visualize the vectors in an html table matrix to examine and assess the values produced in the process. The resulting vectors can be applied to unit, integration, or system testing. The applicability of the vectors to these various layers of testing is based on the model.

4.2 Test Cube Conversion

Increasing complexity of integrated circuits has forced the industry to abandon partial scan, which necessitates a computationally demanding and unaffordable

sequential ATPG, and to rather adopt full scan despite its costs. In this paper, we propose a partial scan scheme driven by a computationally efficient test cube analysis Upon the identification of a maximal-sized set of scan flip-flops that are converted to non-scan, a simple post-processing of the test cubes helps compute the values to be loaded into the scan flip-flops, eliminating the need to re-run ATPG while at the same time ensuring the quality of full scan. The proposed scheme combines the simplicity of the conventional ATPG flow with the area, performance, test time, and test power reduction benefits of partial scan. The proposed test cube analysis driven partial scan scheme is orthogonal and thus fully compatible with other test cost reduction techniques, such as test data compression and test power reduction, which can be applied in conjunction.

4.3Linear Feedback Shift Register

A linear feedback shiftregister (LFSR) is a shift register whose input bit is a linear function of its previous state. Mostly used linear function of single bits is XOR, thus normally it is a shift register whose input bit is driven by the exclusive-or (XOR) of some bits of the overall shift register value. The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the stream of values produced by the register is completely determined by its current (or previous) state. Likewise, because the register has a finite number of possible states, it must eventually enter a repeating cycle. However, an LFSR with a well-chosen feedback function can produce a sequence of bits which appears random and which has a very long cycle.

4.4 S-Filling for Shift-Power Reduction

Prior X-filling methods for shift-power reduction consider the shift-in power only, but filling X bits may have impact on both shift-in and shift-out power. This section shows how we consider both shift-in and shift-out power reduction with X-filling. As previously discussed, we fill the X-bit with the highest *S-impact* first. To model the shift transition probability in the test stimuli, we calculate the *Shift-In Transition Probability* (*SITP*) caused by filling one X-bit as follows:

$$SITP_i = (P_{1S_{i-1}} \times P_{0S_i} + P_{0S_{i-1}} \times P_{1S_i}) \times (i-1) + (P_{1S_i} \times P_{0S_{i+1}} + P_{0S_i} \times P_{1S_{i+1}}) \times i \quad (4.1)$$

Where P_{1si} *(*P0si*)* represents the probability of *Xi* to be 1(0).

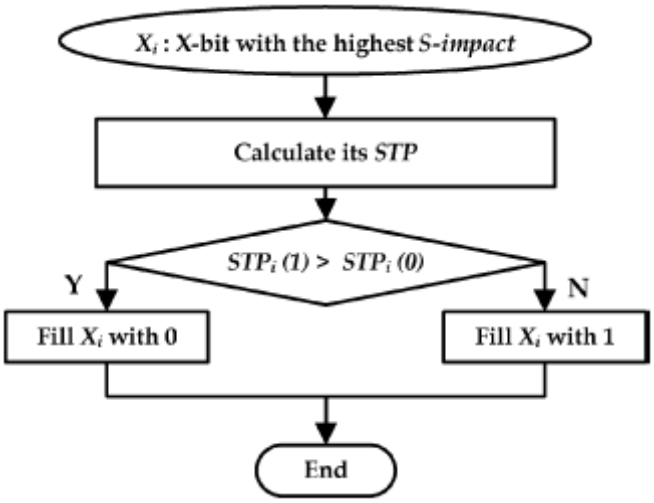

Fig.4.2 *S-filling* for shift-power reduction

The calculation of the *Shift-Out Transition Possibility* (*SOTP*) caused by filling *Xi* is quite similar, as:

$$SOTP_i = \sum_{j \in fan\text{-}out(X_i)} [(P_{0_{R_{ij}-1}} \times P_{1_{R_{ij}}} + P_{1_{R_{ij}-1}} \times P_{0_{R_{ij}}}) \times (l_{sc,j} - j + 1) + (P_{0_{R_{ij}}} \times P_{1_{R_{ij}+1}} + P_{1_{R_{ij}}} \times P_{0_{R_{ij}+1}}) \times (l_{sc,j} - j)] \quad (4.2)$$

Where *j* ranges all the X-bits affected by *Xi*, notice that these X-bits can be in different scan chains.

Now the *Shift Transition Probability (STP)* is decided as:

$$STP_i(1) = SITP_i(1) + SOTP_i(1)$$
$$STP_i(0) = SITP_i(0) + SOTP_i(0) \quad (4.3)$$

As shown in Fig.4.2, if *STPi*(1)<*STPi*(0), filling *Xi* with '1' is likely to generate fewer shift transitions on scan chains.

4.5 C-Filling for Capture-Power Reduction

Capture power reduction is more difficult than shift power reduction. This is because the capture operation is directly related to such critical issues as circuit timing and ATPG complexity, which, if not properly handled, could render a solution for capture power reduction impractical. For this reason, X-filling is widely considered a preferred approach to capture power reduction, as it needs no modification to circuit design or ATPG.

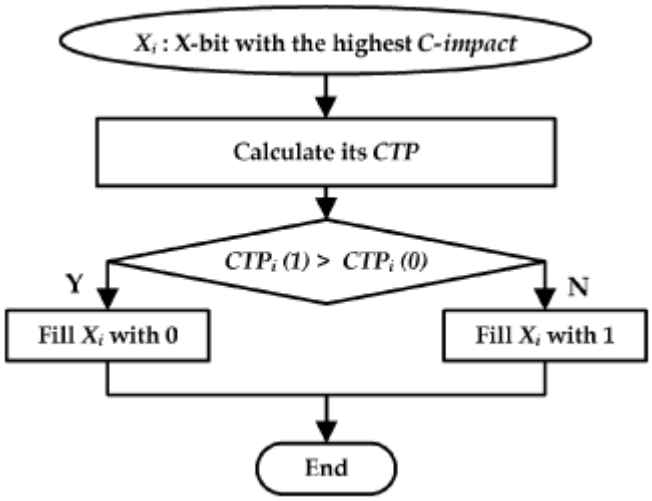

Fig.4.3 *C-filling* for capture-power reduction

X-filling is the process of assigning logic values to the unspecified bits (X-bits) in a test cube so as to obtain a fully-specified test vector with a certain characteristic. For example, random X-filling has long been used in dynamic compaction for detecting more faults by a test vector. Recently, a few X-filling methods have been proposed for capture power reduction, and they can be collectively called LCP (Low-Capture-Power) X-filling.

Similarly, when we conduct *C-filling* for capture-power reduction, we target the X-bits with higher *C-impact* earlier, and we measure transition probability of logic nodes
in fan-out of the filled bit in the capture cycle. The *capture transition probability* (*CTP*) caused by filling an X-bit *Xi* in test stimuli is calculated as:

$$CTP_i = \sum_{fan-out_{X_i}} (P_1' \times P_0 + P_0' \times P_1) \qquad (4.4)$$

where for all logic nodes affected by *Xi*, *P*1' (*P*0') is its probability to be '1' ('0') in the launch cycle, and *P*1 (*P*0) is its probability to be '1' ('0') in the capture cycle.
As shown in Fig.4.3, if *CTPi*(1)<*CTPi*(0), filling *Xi* with '1' is likely to generate fewer capture transitions on scan chains.

4.6 Overall Flow

The objective of the proposed *iFill* X-filling technique for simultaneous shift- and capture-power reduction is to keep the capture transitions under threshold and reduce shift transitions as much as possible. To meet this target, we proposed the overall flow as outlined in Fig.4.4.

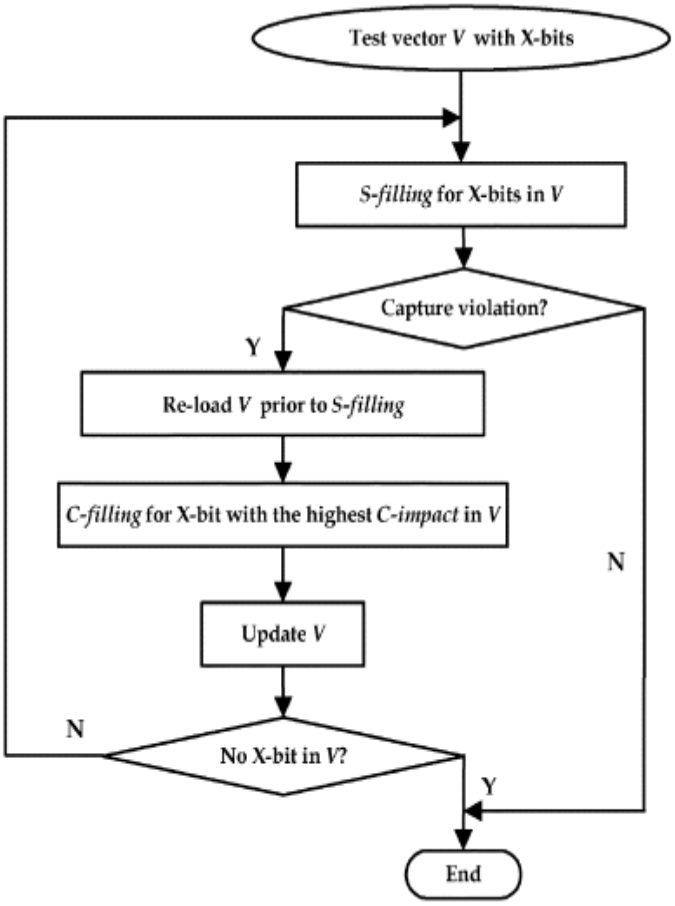

Fig.4.4 Overall flow

First, we try to conduct *S-filling* to use all the X-bits in test vectors for shift-power reduction and check whether the capture-power violates the constraint after the *S-filling* process. If it does, we need to re-load the initial test cube, and fill one X-bit with the highest *C – impact* value for capture-power reduction. After filling every X-bit for capture- power reduction, the test vector will be updated, and we will apply *S-filling* procedure one more time to fill the remaining X-bits and then the capture-power will be checked again to see whether this test vector still has capture-power violation.

When there is no power violation, we have completed filling the vector; otherwise, *C-filling* procedure will be called again to reduce capture transitions. The above steps iterate themselves until there is no peak power violation or all X-bits have been utilized to reduce capture-power.

If the capture transitions still violates the limit after all X-bits have been filled, this test pattern need to be discard. After X-filling for all the test patterns in give test set, new test patterns need to be generated for the faults the test pattern violating the capture power limit covered.

4.7 Circuit Under Test

The CUT compare the current output of the circuit which is tested by generated test pattern with the correct

fault free output. Benchmark circuits are taken as a reference for comparing the results.

5. CONCLUSION AND FUTURE ENHANCEMENT

The proposed work is an effective and efficient impact-oriented X-filling method, namely "*iFill*", which is able to keep the CUT's capture-power within its peak power rating while reduce the CUT's shift-power as much as possible. Another contribution of the proposed technique is that it is able to cut down power consumptions in both shift-in and shift-out processes. In this work, all X-bits in given test cubes will be used for test power reduction.

In practice, however, these X-bits may be used for other purposes (e.g., test compression). This work is considerable for future to develop holistic X-filling solutions that are able to fulfill different needs.

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