Test pattern generation for longest path eliminating SDD using ATPG

P.SHERUBHA
M.E Vlsi Design,
Srinivasan Engineering College,
Perambalur-621 212
Tamilnadu, India.
Sheru_June@Yahoo.Co.In

S.CHITRA
Assistant Professor,
Srinivasan Engineering College,
Perambalur-621 212,
Tamilnadu, India.
Chitra_1234@Yahoo.Com

Abstract—Faster than-at speed Testing is an efficient way to test small delay defect in a circuit. Small delay defects can be eliminated using this method. Test patterns are selected in accordance with the sensitized path. Those selected test patterns are grouped, and given into the test path. Hence, the fault coverage for transition delay fault can be identified. The method can still be promoted by grouping the path instead of test* patterns *to make the testing of longest path more efficient. The frequency provided is higher for the longest path with ATPG tool. While testing the longest path the output Flip-flop should be masked to avoid the false timing. As a result, for testing the longest path, the test quality for Small delay defects is higher with reduced CPU time and widely used for industrial purposes with reasonable test pattern size.

Key terms: Faster Than-at speed testing, small delay defects, sensitized path, ATPG, test patterns.

1. Introduction

Testing has been under the process of evaluation in every developing circuit. Since testing performed in circuits with shrinking size is a challenging task in all industrial applications. Usually transition fault targets large delay faults in the circuit mainly in fault site. Researches shows that resistive open in a circuit also causes delay faults and small delay defect cannot be ignored in the circuit. Transition fault is composed by pairing stuck-at-0 and stuck-at-1[4]. Transition fault is mainly investigated in sequential circuits and it is also highly expensive. A new automatic testpattern generation (ATPG) tool for path delay faults in sequential circuits has to be developed. Recent research developed that the cost is reduced in the combinational circuits, i.e. the test vectors are dependent on the test lines. This cannot be applied in sequential circuits because of the design- for- Testability (DFT) structures. Here the test vectors are independent and consume more silicon area. The ATPG was developed by extending a path generation algorithm for combinational circuits to handle scan-based synchronous sequential circuits. The runtime of timing-aware automatic test pattern generation (ATPG) may be 20 times higher than that of a traditional ATPG[10]. Poor testability oflongest paths, it is nearly impossible for ATPG procedures to find a longest testable path set to cover all the fault sites.

Grouping of test pattern is an important strategy while providing faster-than at speed testing. It reduces the delay variation when selecting the test pattern for propagation. Higher test frequency is determined for longest path. To avoid the false timing failure in the longer sensitized paths the output flip-flop is masked. Masking the flip-flop is undesirable and it should be highly avoidable. Selecting the path which has shorter delay provides better testability to cover the transition fault in the circuits. Controlled power dissipation under high frequencies is used here for testing.

2. METHODS FOR PATTERN SELECTION

In this section, high-quality patterns from n-defect transition fault are provided:

- Determination of number of test patterns[2] to be used in the test path. This may be of users' choice, e.g., N.
- Let 'N' be the parameter to detect the test pattern, that value should fit the test budget.

- Select the largest-deviation pattern and by creating the observation point. The selected test patterns are sorted and this is known as pattern re-ordering.
- Run the Top-off delay fault (TF) in ATPG to increase the fault coverage.

2.1 Results based on pattern selection

The result based on evaluation of the longest path provides some of the expected output. The pattern counts for larger values are higher than that of the timing-aware ATPG. When the given input test pattern [2] increases, the longest paths are seems to be excited. To evaluate the timing-aware constrains and the fault detection performance of our selection path, we inject a fault into the test path. While evaluating the longest path, a pattern matching procedure can also be done to merge the patterns with the given frequency. This method could reduce the number of calls to the test patterns provided by the ATPG. When the patterns are merged the newer pattern is consistent with the previous pattern and this is known as traversing.

3. **D**ETERMINATION **O**F **T**ESTABLE **P**ATH

The ATPG procedure is to identify whether the path is testable, after the path with certain length is found. We may attempt multiple patterns to the path which can be testable. By implying the faster-than at speed testing technique to the circuit under test(CUT) the slack should be as lower as possible. Slack is defined by the difference between the required arrival times of the signal to the actual arrival time of the signal[10]. While traversing the parameter such as latest arrival time, minimum required time, earliest arrival time, maximum required time should be noted in order to evaluate the slack of the testable path.

Definition I: Delay traversing from the primary input to the edge of the test path is given as *latest arrival time.*

Definition II: Difference between the delays of the longest path of the circuit minus the delay of the longest path from edge to the primary output (PO) is given as*minimumrequired time.*

Definition III: The delay starting from any input (PI) to the edge is known as the *earliest arrival time.*

Definition IV: The difference between the delays of the longest path to the delay of the shortest path starting from the edge to the output is known as *maximum required time*. The delay of the selected path should fall within the given length span.

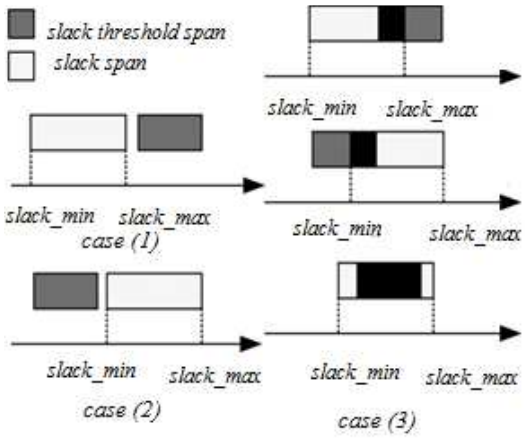

Fig 1.Slack analysis.

3.1 ATPG Method

When analyzing the path delay the complexity is higher and cost oriented. While using the timing aware ATPG the shorter path (SP) and intermediate path (IP) are held constant. The probability of fault coverage in longer path is being detected using multiple-detect method. The ATPG tool utilizes the capability to activate the longer path. The observation point of the longer path is mandatory[4]. The internal node of the circuit is observed separately. The values captured during pattern generation are ignored in the IP and SP of the circuit. The longer paths which make the transition is known as active end point and if there is no transition then it is known as non-active endpoints. The IP and SP of the circuit node are non-observable.

3.2 Testable path with certain delay

A path stem grows from the seed transition fault (TF) by selecting edges from its fan-in edge and fan-out edge. The fan-in edge is called head and the fan-out edge is called tail. It is better to choose the uncovered TF than covered TF, because the transition direction is consistent than the current transition. The slack of the longest path along with the edges is given as,

Slack_min = T*req_min* – T*arrival_latest*

Slack_max = T*req_max*– T*arrival_earliest*

By using the slack analysis, paths belong to certain length spans could be effectively targeted. The delay fault of the sinal is provided by two logic values, i.e., low (L) and high (H). The possible signal transitions are L → L, L → H, H → L, H → H.

When the multiple inputs are required to change at the same time to provide the output, all the input-to- output paths are considered by eliminating the redundant path. When the multiple inputs are given to the path of the circuit under test, the output is provided with the highest deviation.

4. DETERMINATION OF TEST FREQUENCY

The test frequency is considered in two ways. First one ismaximum [3] and the possible frequencies that can be used by faster than-at speed testing. Second one is the delay in the sensitized paths. The minimum clock cycle generated for the circuit under test should be 15.45ps, and the buffer delay may be 0.18µm.The test clock of the *xth*frequency is calculated by,

$$C(x) = (x \div m) \times Dmax, \quad 1 \leq x \leq m$$

Where 'm' is the test frequencies. To avoid the path delay analysis a method called multiple-detect method is introduced. This multiple-detect method activates the fault sites of the longest path. Since the ATPG tool has the capability, we may utilize it to analyze the faulty path.

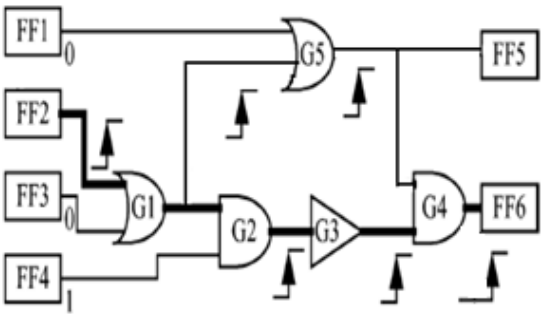

Fig 2: Higher clock frequency for test path.

4.1 Analysis of test frequencies for merged paths

Merging of paths can also be same as that of the pattern merging. In pattern merging the test vectors are merged to reduce the run time of the CPU, whereas when merging the test path of same gate length will reduce the hardware complexity also reduce the overall process of the circuit under test. Merging of paths may include both the longest path and the shortest path. Here the longest path is considered to remove the fault, which degrades the system performance. Highly faultless circuit is widely used in the industrial purposes. Faulty circuit makes the system to provide the output in unexpected time.

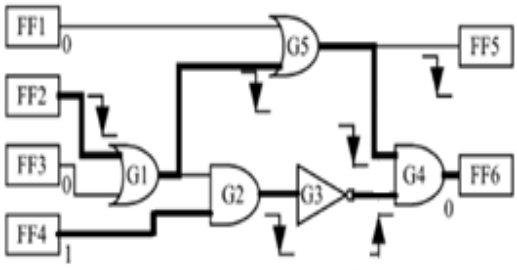

Fig.3. Testable paths with same gate length.

Fig(3) shows that the G1-G5-G4-FF6 and the G2-G3-G4-FF6 have the same gate length. Hence these two paths can be merged or provided with the same frequencies. So the output can be extracted in the expected time.

5. EXPERIMENTAL RESULT

The proposed method test pattern generation for longest path, enables transition fault coverage still higher than using normal at-speed testing [1]. Two methods has been proposed, first one is multiple-detect pattern and second one is path merging. The proposed method can be implemented in modelsim 6.5b, and runs on windows 8 at a 1.8GHz processor with 2-GB memory. The buffered delay value may be of 0.18µm.

As we see the proposed method could achieve high TF coverage with acceptable CPU time. Here we consider the pattern merging procedure; hence the switching activity of the generated test patterns can be comparatively lower. Using ATPG the pattern merging and X-filling methods can reduce the switching activity [10] in the circuit when the frequency is provided. Faster than-at speed testing provides the lesser switching activity when circuit under test. The timing- aware

ATPG tool provides the method to generate the test patterns that sensitize the longest testable paths through the fault sites to detect the small delay defect(SDD). However in some internal circuit nodes the SDD cannot be detected because they have larger timing slacks. While using an on-chip clock generation system in the faster than-at speed testing, test clock with dynamic range and higher resolution of frequencies can be provided.

6. CONCLUSION

The paper presents the concept of pattern-pairs which shows the effectiveness of TF coverage [4] in a circuit. Transition fault is achieved along with the reduced CPU time. This method can be extended by using the pattern merging and the X-filling methods. The testable paths along with the lower slacks are proposed in this paper. Multiple-detect pattern provided in the timing-aware ATPG excites the longest path and makes the faster than-at speed testing more efficient. The method detects the small delay defect which escapes through the gross delay pattern set. Thus it increases the reliability of the circuit under test. Test pattern compression can also be done. Lesser switching activities can reduce the power constrains. Finally small delay defects caused due to resistive opens, resistive shorts and process variation can be detected using ATPG.

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