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Ternary Analog to Digital Converter using Carbon-Nanotube FET: A Survey

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***Abstract*—ADCs are important devices in communication application field. There is a requirement of efficient & highly accurate ADCs. This paper investigates possible implementation of ADCs using Ternary logic and Carbon-nanotube FET and its advantages. CNTFET is a promising device for submicron node in terms of power efficiency and leakage. Also, use of ternary logic improves the accuracy & area efficiency by using less number of interconnects. Hence, Ternary ADCs using CNTFET are appropriate for advanced system needs.**

Keywords—Analog-to-Digital converter; Carbon-nonotube field effect transistor(CNTFET);efficiency;scaling;Ternary logic; Multi-valued Logic(MVL);unity current gain frequency;low power; leakage

I. INTRODUCTION

Modern technology requires devices with high speed, more accuracy & low power consumption. World is coming closer and closer by means of high speed communication links and wireless media, which ultimately makes use of high frequency analog signals.

Normal high speed processing is usually done using digital computers, processors, etc. Hence, in this modern one click accessible world, requirement of advanced high speed & efficient Analog-to-Digital converters and Digital-to-Analog converters is crucial.

Currently varieties of ADC & DACs are available in market for various applications. This paper investigates a possible implementation idea for future high speed & efficient ADC with use of ternary number system and CNTFET device, which can fulfill the requirements of future ADCs like low power consumption, high speed, efficient and compact design. In this paper, a brief survey is presented about ADCs, ternary logic, Carbon nanotube Field effect transistor & their trends. Paper is arranged in sections as follows.

Section II discusses about ADCs, its architecture and trend. Section III describes about the features of Ternary number system and its advantages and section IV discusses about CNTFET characteristics and its usability. Section V presents brief information about existing literature about Ternary analog-to-digital converters and in last section a conclusion is made on the basis of discussion in previous sections.

II. ANALOG-TO-DIGITAL CONVERTER

Some previous surveys on Analog-to-digital converters discuss important trends and future ADC trends. In which R.H. Walden's survey on ADCs and B.E. Jonsson's survey on area efficient architecture are important.

In [2] Walden surveyed commercially available ADCs and experimental ADCs.ADC's performance can be analyzed using parameters like stated resolution, SNR, spurious-free dynamic range (SFDR) and power dissipation.Thissurvey showedtwo important observations. First,approximately 1 bit of resolution is lost for every doubling of sampling rate. Secondly, sampling rate is affected by comparator's efficiency in terms of making unambiguous decision. The 1-bit per octave slope is related to the sample-to-sample variation of the instant in time at which sampling occurs. This variation is called aperture jitter or aperture uncertainty.Advanced ADC requires low noise designs that achieves less than 0.5ps of aperture uncertainty and/or technology with f_T>>50GHz (unity current-gain frequency of transistor).[2]

In Ref.[5],Jonsson found from state-of-the-art data points that the area increase by 2.05× for every additional bit of ENOB for DSM, and by 2.22×/bit for the most area-efficient Nyquist converters.State-of-the-art Area, A is approximately proportional to 2ENOB. Area per effective quantization step, A_Q are almost independent of ENOB. State-of-the-art area is almost independent of sampling rate. The overall smallest area reported for Nyquist converters decrease by ~100× for every 10× of process with no signs of saturation down to 40 nm.Delta-Sigma Modulator implementations appear to be in a saturated state. It is increasing slightly for latest node. Thus A_Q remains constant. [5]

To analyze and compare the area efficiency of individual architectures, the state-of-the-art A_Q envelopes were observed versus ENOB, sampling rate and fixed-bandwidth SNR from

which we can conclude that among Nyquist converters, the cyclic and SAR converters are most area efficient.[5]

In [7] Murmann has discussed ADC trends over past eleven years with respect to parameters like power dissipation, scaling and digital assistance of architectures. From this data he has drawn various graphs relating SNDR, Power Efficiency, speed, f_T, gain, conversion bandwidth, etc.

From plot of SNDR against power efficiency & bandwidth, speed limit of technology & Power efficiency are the design tradeoffs.Approximately power dissipation reduces by 2 every two years and bandwidth doubles every 4 years. Device scaling requires a reduction in supply voltage (VDD), the noise in the analog signals must be reduced proportionally to maintain the desired signal-to-noise ratio. One way to overcome supply voltage limitations is to utilize thick-oxide I/O devices. However they reduce speed of system. To increase SNR by 6dB requires power efficiency improvement by factor of 4. For high-resolution designs scaling technology over time, associated with lower supply voltages, cannot help improve power efficiency. This has led to a general trend towards lower resolution designs.Analog subcircuits are complex which limits the reduction in power dissipation. The goal of minimalistic design is to improve power efficiency and to increase speed by reducing analog subcircuit complexity.A general concern with most minimalistic design approaches is that they tend to sacrifice robustness (e.g. power supply rejection & common mode rejection).[7]

III. TERNARY NUMBER SYSTEM

Binary logic technology has come across the dramatic changes and advances. Although efficient and powerful, binary logic is not the most efficient & powerful switching logic. Non-binary logic or Multiple Valued Logic (radix>2) has been around for quite a while and is known as Multi-Valued Logic. Ternary is a special case of multi-valued logic where radix=3.

In existing binary digital system, the output of the system is decided by considering two input conditions i.e. either ON or OFF leaving behind the third conditions i.e. when both the input conditions are same, here decision is considered as don't care or it is discarded by the system.

Alexander [1964] showed that natural base (e ≈ 2.71828) is the most efficient radix for implementation of switching circuits. It seems that most efficient radix for the implementation of digital system is 3 than 2. Ternary logic system has 3 valued switching. Ternary system has several important merits over binary. It can be listed as reductions in the interconnections required to implement logic functions, thereby reducing chip area, more information can be transmitted over a given set of lines, lesser memory requirement for a given data length.

Several advantages of ternary over binary representations are as follows:

A. *Number representation:-*

To represent same number ternary system requires fewer digits than binary. E.g. decimal 16 requiresfive digits in binary (10000) while only three digits in ternary (121). In short ternary takes less word width than binary. This can be useful to reduce area of chip and improve speed of operation.

B. Processing:

Increasing radix of the system can increase processing capacity of the processor. Thus it reduces design complexity, number of interconnections & power consumption of the system.

C. Communication:

In communication based on ternary digital system, a minimum of 3 digits is required to code ten decimal digits. Possible states will be 27! / (27- 10)! ≈ 3.1x 1012 ternary coded decimal, which can be used in various communication applications for error correction, encoding, etc.

D. Converters:

In case of ADC applications, it increases the number of quantization levels compared to binary. It leads to more accuracy & efficiency of converter.

E. Memory:

Requirement of less interconnects in ternary logic has advantages like cost/bit ratio reduction, reduced access time & increased storage capacity [8]

IV. CARBON-NANOTUBE FIELD EFFECT TRANSISTOR

The transistor (MOS) size has shrunk from a several microns to less than 45 nm during the last two decades. The short channel effects, threshold voltage roll-off and drain induced barrier lowering, become increasingly significant as the channel length of semiconductor devices is reduced. The short channel effect limits the scaling capability of MOSFET. The new device, such as SOI MOSFET, FinFETs or nanowire MOSFETs obtained additional performanceimprovements that overcome the device scaling difficulty.One of the basic ideas is to replace the silicon MOSFETs with CNTFETs to overcome all the limitations of silicon MOSFETs such as the exponential increase of leakage currents in scaled devices.In MOSFET, we observed that after decreasing the gate oxide thickness the quantum capacitance increases for the different gate voltages. Whereas in case of CNTFET under identical simulating condition as in case of single gate MOSFET, we observed that as the oxide thickness goes down from 1.5 nm to 0.7 nm the quantum capacitance decreases, when we apply gate voltage from 0.5 V and above.Quantum capacitance (Qc) is the property of channel material. The movement of Fermi level requires energy and this conceptually corresponds to quantum capacitance.[1]

In CNTFET devices effect of temperature on threshold voltage is negligibly small. Temperature hardlyaffects the threshold voltage as there is only 4.6 % variation recorded while raising the temperature from 27ºC to 227ºC. Minimization of leakage currents is enormously important in VLSI these days. As the devices scaled down in nanometer regime the threshold voltage is also scaled, consequently the leakage power increases. Leakage current has become the limiting factor for oxide thickness thinner than 1.5 nm. Decreasing the channel length increases the current drive of the transistor. Much of the scaling is therefore driven by decrease in channel length. If only this parameter is scaled many problems are encountered, such as increased electric field. If the channel length becomes too short, the depletion region from the drain can reach the source side and reduces the barrier for electron injection. This is known as punch through, and because of this, device's characteristics degrade. In long channel devices, the gate is completely responsible for

depleting the semiconductor. In short channel devices, part of the depletion is accomplished by the drain and source bias. Since less gate voltage is required to deplete the transistor, the barrier for electron injection from source to drain decreases. This is known as drain induced barrier lowering (DIBL).Below 20 nm channel length the threshold voltage increases rapidly in case of CNTFET device and the threshold voltage goes on decreasing beyond 20 nm channel length in case of MOSFET.which leads to more leakage power and finally device degrades in terms of performance in MOSFET .[1]

In Ref.[3], Sayeed Hasan *etal* used quasi-static approach in combination with theory of ballistic nanotransistors to assess high frequency performance potential of carbon nanotube FET. Through this analysis they obtained limiting value of f_T approximately as 130GHz/L(μm), where L is channel length.[3]

The CNT channel region is undoped, while the other regions are heavily doped, thus acting as the source/drain extended region and/or interconnects between two adjacent devices.A ballistic or near-ballistic transport can be obtained under low voltage bias with CNTs due to the CNT'sultralong (1micrometer) mean free path (MFP) for elastic scattering. By positioning additional CNTs, a linear increase in current can be achieved; however, depending on the distance between CNTs (pitch) and the diameter of each CNT, the current cannot be increased linearly with the number of CNTs in a CNTFET because a small pitch causes the screening effect to occur and the diameter determines the amount of current in a CNT[4]

In Ref.[4], simulation of basic gates & some benchmark circuits was performed to assess the variation in response depending on PVT (process, supply voltage, temperature) variations during which they found that the current change in a MOSFET is about ±30% (±13%) for a ±10% change in length (width) at a gate voltage of 0.9V while the current change in a CNTFET is below ±0.5%. However when the diameter of the CNTFET is changed by ±10%, the current change in a CNTFET is about ±17%. Therefore for a CNTFET, the diameter variation is more important because a CNTFET is more sensitive to diameter variation than length and width variations. The maximum leakage power increases when the diameter is increased.

Also they have tested Power Delay Product (PDP) and maximum leakage power for 32nm MOSFET and 32nm CNTFET logic gates, respectively when the supply voltage is decreased until the gate stops functioning correctly. Change of PDP in a CNTFET is less than a MOSFET because a CNTFET has a lower gate capacitance and a higher mobility than a MOSFET. Also maximum leakage power for CNTFET reduces linearly while for MOSFET it decreases exponentially. The maximum leakage power of the MOSFET gates increases linearly with temperature, while for the CNTFET-based gates this increase is exponential.[4]

Average delay and power consumption of the 32nm MOSFET circuits is about 10 times and 100 times higher than for the 32nm CNTFET circuits respectively.[4]

In Ref. [6], stability of CNTFET is tested using common source (CS) amplifier configuration by means of step response. The importance of such analyses for CS CNTFETs lies with the fact that they can amplify the amplitudes of overshoot/undershoot coming from interconnects.Amplification of each harmonic can deteriorate the input to the next stage on the chip. This increases the importance of the stability analysis for CNTFETs.The small-signal model with a Nyquist stability criterion and step time responses was used. The relative stabilities for CNTFETs with channels containing 100 CNTs at 10-nm pitches with randomly varying diameters were studied. The same analyses for single-channel CNTFET were also performed. The analyses show that, for both types of CNTFETs, with an increase in either channel diameters or lengths, the system becomes more stable. This is because an increase in either parameter gives rise to a switching delay and hence, the corresponding step response exhibits smaller overshoot peak. This behavior is due to the dominance of the larger capacitive elements. However, in general, the channels with 100 CNTs at 10-nm pitch exhibit overshoots that are ~11%–14% larger than those of single channels with similar dimensions.[6]

V. Ternary ADC Literature

In most of the ADC implementation literature, digital circuitry is used to repair errors occurs due to non-ideal behavior of analog circuits. Some ADC implementations try to do it by means of implementing multi valued /non-binary digital circuitry.

In [9] Ternary number system is used for digital correction. They have implemented 1.5bits/stage pipelineADC architecture. Conventional arrangement is replaced as follows:-

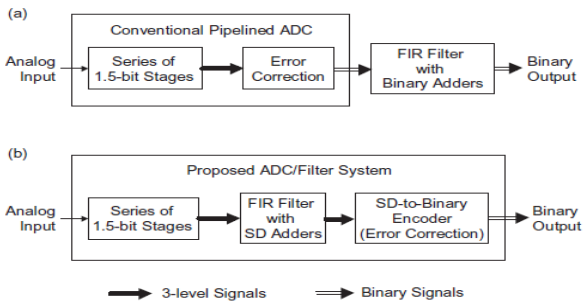

Fig. I:Ternary Pipelined ADC proposed in[9]

In this system, ternary signals are used for filtering purpose. Digital output is in binary form. In this 1.5 bits are interpreted as {-1, 0, 1} & signed digit addition is used.

In Ref. [10], current mode comparators are used. It is 2-digit flash ADC giving multivalued (quaternary) output. It is designed using 0.13μm CMOS process model. 0.35μm channel length is used to achieve favorable current drive. An inverter is used to strengthen the signal. Logic level currents are chosen as multiples of 1μA.They found reduction in circuit complexity

VI. Conclusion

Important data from this survey of ADCs, Ternary numeral system & carbon-nanotube FET are the speed, stability, unity current gain frequency, mobility of transistor, bandwidthand powerefficiency. From all these data following observations can be made.

A. For modern converters there is need of f_T>>50GHz & CNTFET provides unity current gain frequency greater than 130GHz/L(μm).

B. Device scaling comes with a power supply scaling which in turn affects SNR.

C. Average delay and average power consumption for CNTFET circuit is 10 times & 100 times lesser than conventional MOS transistor.

D. CNTFET is more stable according to Nyquist stability criterion.

E. For low and moderate resolution ADCs, power efficiency improves with technology advancement or scaling.

F. Ternary logic improves accuracy & efficiency of converter with less resolution.

G. Area efficiency improves 100× for improvement of process by 10× (scaling down)

H. CNTFET threshold voltage increases below 20nm node.

From above observations it can be concluded that CNTFET and ternary logic are promising technologies for modern ADCs. From observation A, B, C, F& G, it can be seen that CNTFET is superior to MOSFET in terms of speed, power consumption, stability & low leakage at lower feature size.

Existing literature is based on using ternary for analog corrections or designs based on current mode input.Also ternary logic is promising to cope up with tradeoff between resolution & power efficiency.Hence modern high speed & highly accurate ADCs can be designed using ternary logic and CNTFET devices.

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