

Synchronous Transmit Receive controller for POWER-PC using VHDL

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Abstract—In recent years the communication requirements have drastically gained importance and complexity. Large range of systems is now being designed using Field Programmable Gate Array (FPGA) due to its important features which include size feasibility and availability of resources. In this paper the design and implementation of a Universal Synchronous Receiver Transmit (USRT) interface suitable for the use in a POWER-PC based system to perform serial communication are implemented.

Index Terms— Communication, USRT, VHDL, FPGA, Serial Communication.

I. INTRODUCTION

USRT is an important mode of the serial communication. For the entire duration of synchronous communication a common clock is required to transmit and receive data [1]. USRT mostly comes with communication and these systems can handle mostly parallel data [2]. At the transmitter side, parallel data is taken from processor and converts it into serial form and at the receiver, meanwhile another USRT receives this serial data that is transmitted from the transmitter and converts it to parallel form into the computer understandable form.

Another important feature in synchronous is that configurable high speed transmission rates and transmission error detection and recovery CRC is used. Processor configures through specialized registers namely control registers. The design can also be implemented using Asynchronous mode incorporating some changes.

Here USRT code for implementation of USRT to USRT communication application is described and is tested with POWER-PC based Single board computer. The FPGA is also used as it is the best available solution for reconfiguration of the system hardware modification.

Basic UART communication requires mainly two signal lines (RXD, TXD) to complete data communication whereas in USRT there is a clock signal. At the transmit side, If no data to be transmitted, the transmission line will be idle until

triggered. RXD is the receiver, the input to the system. The signal which is high when no transmission or reception goes active low when the transmission starts. In RS-232 the logic '0' will have voltage levels from +3 V to +12 V and logic '1' will have voltage levels from -3 V to -12 V.

II. DESCRIPTION OF EFFICIENT USRT DESIGN

The architecture of USRT contains: Transmitter module and Receiver module as shown in Fig. 1. RAM, 16-bit Cyclic Redundancy Check(CRC) generator using Linear Feedback Shift Register(LFSR) and a register to store the value obtained after the calculation, 8-bit Sync register parallel to serial shift register, glue logic, transmitter logic are the sub modules of USRT transmitter. Similarly USRT receiver consists of serial to parallel shift register, CRC and Sync comparator and RAM, CRC generator. RAM is used for data storage purpose and we have

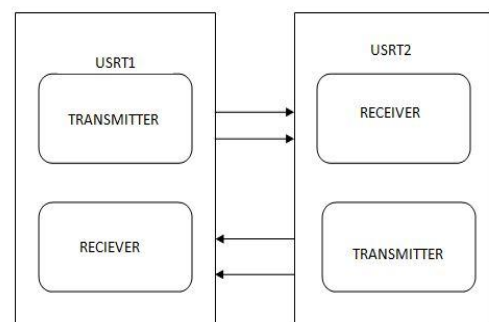


Fig. 1 USRT module

USRTs operate as parallel to serial converters as well as serial to parallel converter. This can be explained as: At the transmitter's side the data is transmitted as individual bits in a sequential fashion the parallel to serial converters come into picture whereas at the receiver's side, USRTs assemble the bits into complete data and thus act as serial to parallel converters.

The processor can send individual or a block of data, whose size is determined by model, through the transmitter section of the USRT. Data is stored into the Random Access Memory, then framed accordingly to the transmitter and user defined options. Finally, the frame is sent to its destination bit

by bit with respect to a clock signal. At the receiver side, the data frame bits are received and sampled. The extracted data from the received frame resides in the internal receiver RAM waiting to be read by the processor with respect to the same clock. The receiver monitors the reception for possible errors and informs the recipient of their existence by setting the proper control bit(s). USRTs have a status monitoring mechanism through dedicated status register(s), a 16-bit register, through which some of the internal operation aspects can be observed. A simple block diagram of the internal structure of a USRT is shown in Fig.2

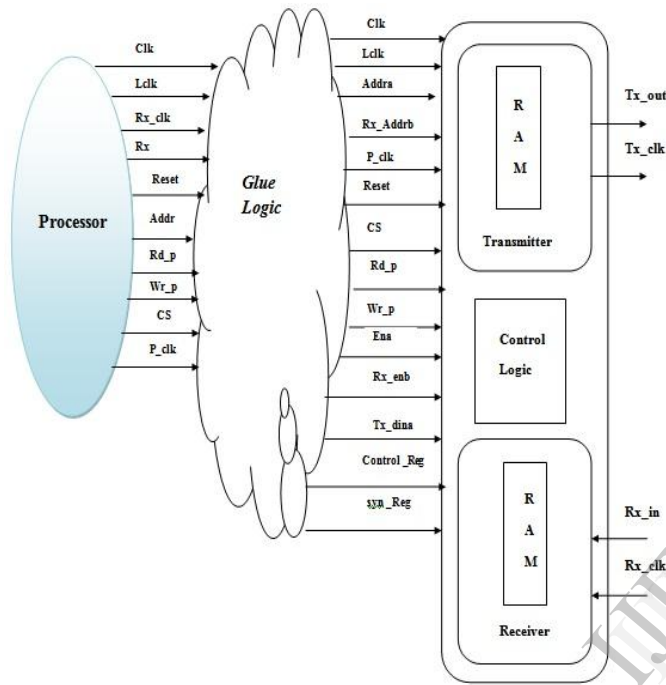


Fig. 2 simple block diagram

A. Modes of Operation

The main modes of operation in USRT is Synchronous. The latter prevails in most applications. Our area of interest lies with the former.

In synchronous mode, both the transmitter and receiver are synchronized to the same clock signal which is usually with respect to the data sent from the transmitter and the data is sent along with the clock on a separate link to the receiver. The receiver in turn utilizes the received clock in extracting the timing sequence and the data and determining the beginning and end of the received bit interval.

In this mode of communication, the transmitter and receiver are pre-configured to the required timing parameters in advance and special bits namely Synchronous bit which is sent initially and n-bits of data and then the 16 bit CRC bits are appended to the data frame for synchronization purposes. Thus timing is embedded in the frame and the need to send a timing signal to the receiver is eliminated

B. Common Communication Errors Encountered in USRTs

The most common errors encountered in USRTs are sync errors, CRC error showing the detection of noise during transmission; such errors occur frequently in hostile environments especially when cables are damaged, if the data have been lost in the receiver side because the internal reception RAM is full then the overrun error occurs.

III. SPECIFICATIONS OF THE DEVELOPED USRT

The modern serial communication demands of high performance and reliability. This also takes compatibility with legacy devices into consideration, these demands were considered in the design specifications

To adapt to modern practices, the USRT offers eight bit mode synchronous or asynchronous communication, variable stop bit options and full duplex mode. However to retain compatibility, it also offers five to seven bit transfer and half duplex mode of communication. Table 1 lists the detailed specifications of the proposed USRT.

Table 1 USRT functional specifications

Specification	Justification
Supports the following transmission modes : <ul style="list-style-type: none"> Asynchronous (Full/Half duplex modes) Synchronous (Full/Half duplex modes) 	In modern systems, full duplex mode is employed while half duplex mode is retained for compatibility with legacy systems.
Supports a wide range of transmission/reception rates (from 50 Hz to 3MHz). This range is obtained using a baud rate generator that	High frequencies are essential for high speed communication. Lower speeds are needed to communicate with older USRTs. Moreover, lower speeds can be used to minimize cross talk if similar links are adjacent.

Eight-level Transmitter/Receiver Buffer	To account for the high speeds of communication that the USRT can reach, blocks of data can be received and buffered until read by the user. Also, this allows the user to issue the transmission of a block of eight-frame size in a single operation. This will also reduce the load on the USRT operation in the system.
Parity Supported (Programmable - Enable/Disable parity and Odd/Even parity).	Single error detection techniques might prove beneficial in noisy operation environments.
Variable data lengths supported (Programmable - five to eight bits)	Byte communication is the modern norm. Five to seven bits data length is to retain compatibility with legacy systems.
Variable stop bits supported. (Asynchronous mode) (Programmable – One or two stop bits)	This is to comply with the RS232 standard where two stop bits mode is used to accommodate slightly different clocks in the transmitter and receiver sides when USRTs from different vendors are connected together.
Error Detection of the following errors: <ul style="list-style-type: none"> • Parity Error • Overrun Error • Framing Error (Asynchronous mode)	Parity error detection provides a measure of the reliability of communication. Framing error detection indicates the necessity of reconfiguring the internal clocking sources at both ends correctly. Finally, overrun error informs that data has been lost and the need to frequently read the received data.

Supports Interrupts (Programmable – with ability of Global Masking)	Most modern systems are interrupt-driven for the reason that interrupt techniques save processing clock cycles in comparison with polling techniques and are essential in real time applications.
Supports Addressable (8-bit Universal – Addresses up to 256 devices)	Mainly used in industrial and control applications in multi-drop networks where a master USRT can communicate with a certain other slave USRT.

IV. DESIGN METHODOLOGY OF THE USRT SYSTEM

The methodology adopted in carrying out the USRT system design was based on systems and software engineering approaches though no single definitive approach was considered in its own regard. Minor variations to systems engineering approaches were considered to account for the working environment under which the project was developed. The design steps that the system went through are [3]:

1. Requirements Definition. The requirements definition phase specified the functionality as well as the essential and desirable system properties. This involved the process of understanding and defining what services were required from the system and identifying the constraints on system operation and development.
2. System/Subsystem Design [4]. This phase was concerned with how the system functionality was to be provided by the components of the system and where the system specification was converted into an executable system specification.
3. Subsystems Implementation and Module Testing. The subsystems identified during subsystem design were implemented and mapped into hardware code using the VHDL. In this critical stage, individual modules were extensively tested for correct functional operation. Each component, once implemented, was tested independently without the other system components and the assessment of the functional behavior was concluded from the simulation output.
4. System Integration. During system integration, the independently developed subsystems were merged together to build the overall USRT system in an incremental approach.
5. System Testing. The overall integrated system was subjected to an extensive set of tests to assure correct functionality, reliability and performance. The tests were

aimed to test the behavior of the system as a whole in addition to the interfacing between the subsystems.

VHDL was used to develop and simulate the USRT system and subsystems under Xilinx ISE 13.1 environment. USRT modules have been designed and verified separately, before being integrated together.

A. The Baud Rate Generator

The USRT system contains a programmable clock generator. Inputs are the system clock and the values of the two divisor registers.

This module is designed to generate a square clock irrespective of the divisor value. In synchronous mode of communication, this clock is transmitted along with the data. Also, it is used to generate the baud-rate clock, through a division by 16.

Assume that the system clock Frequency is 50MHz, baud rate is 9600bps, and then the output clock frequency of baud rate generator should be $1 * 9600\text{Hz}$. Therefore the frequency coefficient (M) i.e. counts value of the baud rate generator is: $M = 50\text{MHz} / 1 * 9600\text{Hz} = 5208$ When the USRT receives serial data, determining where to sample the data information will be very critical. The ideal time for sampling is at the center of each serial data bit.

In this design, we generate a baud rate of 115200 using the 75 MHz clock that the system have and then we divide this baud rate into various other baud rates to generate the different values. We have designed configurable baud rate generator, the selection of baud rate shown in Table 2.

Table 2 Selection of Baud Rate

S0	S1	S2	BAUD RATE
0	0	0	115200
0	0	1	57600
0	1	0	38400
0	1	1	19200
1	0	0	9600
1	0	1	4800
1	1	0	1200
1	1	1	300

Hence, different baud rate has different frequency coefficient (M) i.e. count value of the baud rate generator.

For ex: for 2400Hz, $M = 50\text{MHz} / 1 * 2400\text{Hz} = 20833$

B. Glue Logic

The processor sent the Sync, Data, Address and the Control register bits together. The Glue logic is used for obtaining the required information from the one which is sent by the processor. The Glue logic checks for the address and then decodes the information, and then sent it to the respective registers present. The data from and to the processor from external source is sent through a single line which is taken care by this glue logic.

D. The Transmitter Module

The transmitter module is responsible for transmitting the data serially utilizing the criteria set by the user through special control registers. These criteria include the data rate, number of data bits, 8-bit Sync bits and CRC bits. The processor gives its requirement through a control register that is present. Based on the control register values the CRC- one,- zeros, -all sync etc. may be enabled or disabled based on this value that is given.

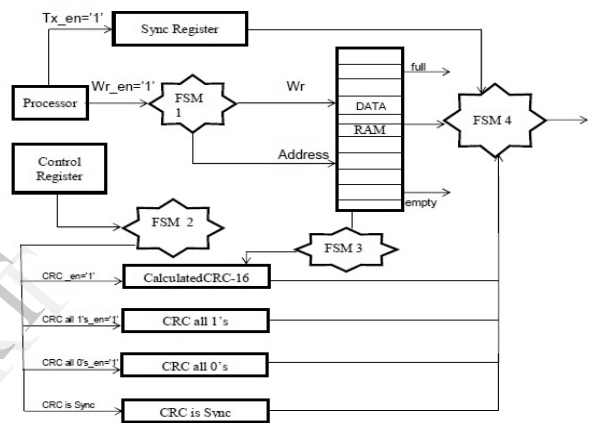


Fig. 3 Transmitter subsystems block diagram

D. The Receiver Module

Fig. 4 shows the different subsystems used for the design of the receiver section. Again, we chose a sample to show the internal design details of one of the subsystems.

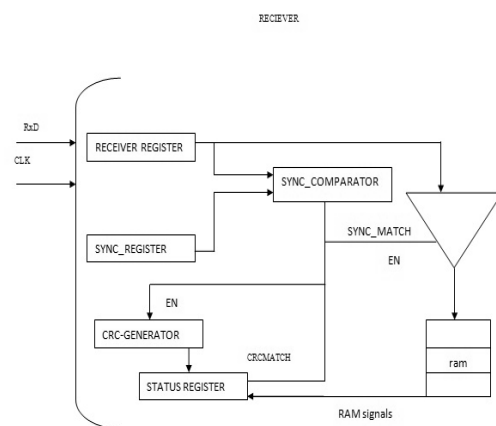


Fig. 4 Receiver subsystems block diagram

E. The CRC generator

A 16-CRC generator is present at both the transmitter as well as at the receiver end. At the transmitter end the CRC generator uses the data sent by the processor and generates 16-bit CRC and at the receiver side the data along with the CRC sent from the transmitter will be sent to the CRC generator at the receiver side leaving the CRC register with all “zeros” when the last bit of the CRC is passed through the CRC register.

V. TESTING AND VERIFICATION PROCEDURES

In general, the system testing process has two distinct goals:

1. To demonstrate to the developer and the customer that the system meets its requirements.
2. To discover faults or defects in the system where the behavior of the system is incorrect, an undesirable or does not conform to its specification [3].

The first goal leads to validation testing, where the system is expected to perform correctly using a given set of test cases that reflect the system's expected use. Defect testing is the second goal, where the test cases are designed to expose defects. The test cases can be intentionally obscure and need not reflect how the system is normally used. For validation testing, where the system performs correctly it is a successful test. For defect testing, a successful test is one that exposes a defect that causes the system to perform incorrectly.

In general, the project went through several phases during the testing process as illustrated in Fig. 5:

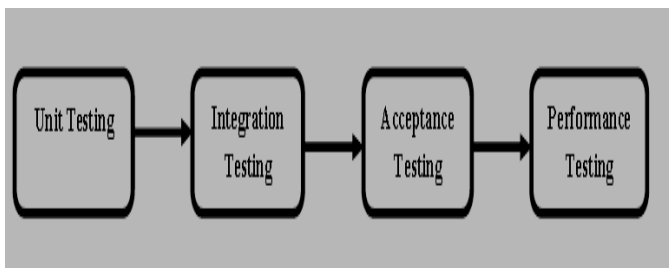


Fig. 5 System testing phases

VI. RESULTS

The implementation of a USRT interface suitable for use in FPGA based systems is done. The individual codes had been simulated and the results are verified as well as the result is verified after the code is integrated into a single module. The USRT module works according to the specification given and is tested with the FPGA and POWER-PC.

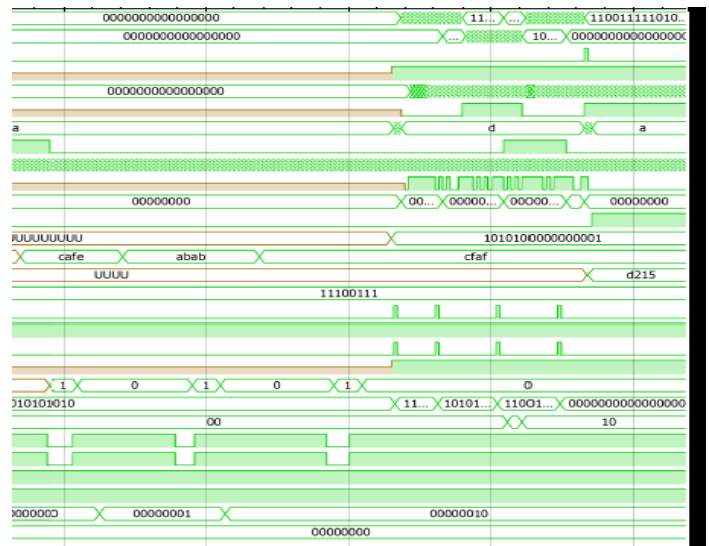


Fig.6 CRC result

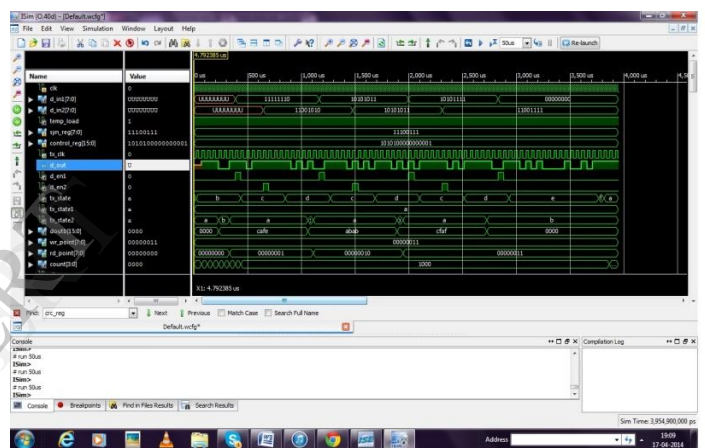


Fig.7 USRT Transmission

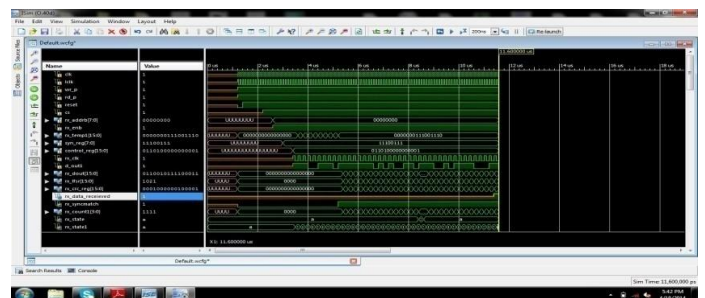


Fig.8 USRT Receiver

VII. CONCLUSION

The design and implementation of a USRT interface suitable for use in POWER-PC based single board computers was presented. The design features both synchronous and asynchronous operation and can uniquely operate using 9-bit address detection mode suitable for use in multi-drop networked serial communication devices. The USRT is able to detect and recover from common serial communication errors such as overflow and framing errors. It can also detect false

start bits. The design is implemented using VHDL and programming it into the FPGA with POWER-PC.

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