Synchronous and asynchronous Counter using an Adaptive Frequency Search Algorithm

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Abstract— A new adaptive frequency search algorithm (A-FSA) is presented for a fast automatic frequency calibrator in wideband phase-locked loops (PLLs). The proposed A-FSA optimizes the number of clock counts for each frequency com-parison cycle, depending on the difference between the target frequency and the PLL output frequency, as opposed to a binary frequency search algorithm (B-FSA), where the frequency search time per cycle is fixed. This eliminates unnecessary clocking times during the frequency comparison process, and thus reduces the total PLL lock time. The additional circuitry needed for A-FSA is only a simple counter controller, thus minimizing hardware overhead. To verify the effectiveness of the proposed algorithm implemented using VHDL modelsim verified by xilinx.

Index Terms— Adaptive frequency search algorithm (A-FSA), automatic frequency calibrator (AFC), binary frequency search algorithm (B-FSA), voltage-controlled oscillator (VCO), wideband phase-locked loop (PLL).

I. Introduction

The phase-locked loop (PLL) is one of the essential building blocks of radio frequency (RF) transceivers for portable wireless devices. To reduce the power consumption and/or cost of such transceivers, while supporting multiband communication standards, it is desirable to design a single wideband PLL. Because of the stringent phase noise require-ments, PLLs in RF applications typically employ an LC-tank-based voltage - controlled oscillator (LC-VCO). However, if a single capacitor is only used in the LC-tank for frequency tuning, it is difficult to achieve wide operating frequency bands. To overcome this difficulty, switched capacitor banks (cap-banks) have been widely used in LC-VCOs [1]–[3], with the cap-bank capacitance being digitally controlled to generate multiple subband frequency tuning curves. Another advantage of this technique is that the VCO gain (KVCO) is lowered for a given PLL tuning range, which helps improve phase noise performance.

Fig. 1 shows a cap-bank-based wideband PLL with an automatic frequency calibrator (AFC) [4]–[11]. The AFC and cap-bank perform coarse frequency tuning by searching for the sub band tuning curve closest to the target frequency.

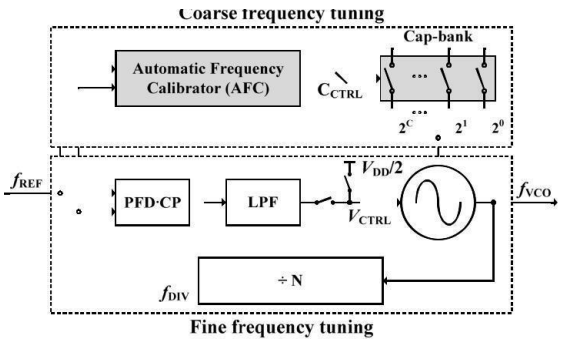


Fig. 1. Overall structure of an AFC-based wideband PLL.

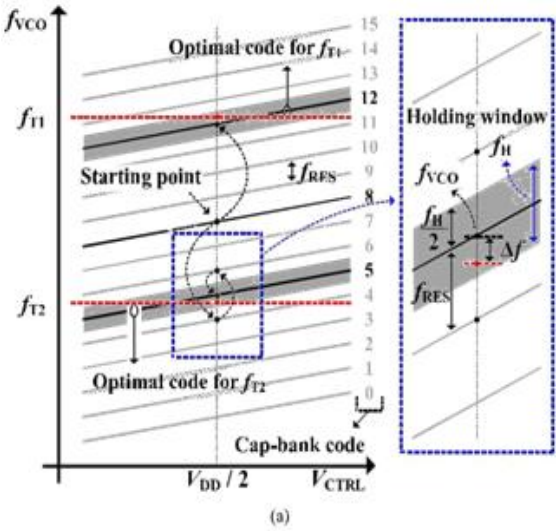
During this coarse tuning, the analog VCO input *V*CTRL is connected to a fixed voltage, typically equal to half the supply voltage (*V*DD/2). Fine frequency tuning is then accomplished by an ordinary PLL locking process, which is performed by phase frequency detector, a charge pump, a low-pass filter, a feedback frequency divider, and a VCO. The most important PLL performance metrics, such as phase noise, clock jitter, and spurious tone suppression, are dominantly determined by the fine frequency tuning part, because the AFC is turned OFF right after the completion of the coarse frequency tuning. The total PLL lock time, however, is greatly affected by the coarse tuning part, which calibrates the VCO output frequency before the PLL lock so as to find the optimum cap-bank input *C*CTRL. Given that the time needed for this calibration is inversely

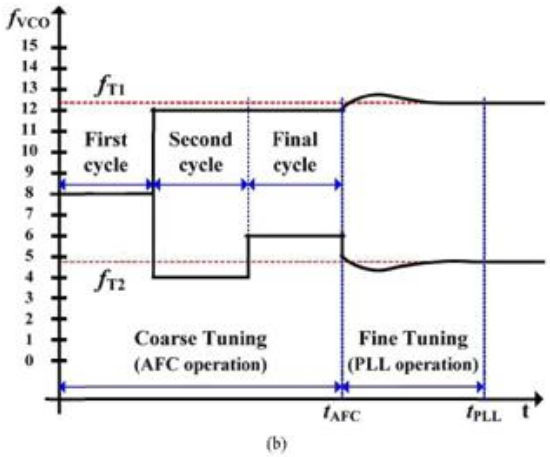
proportional to the calibration accuracy, it can impose stringent timing constraints on the PLL, especially in frequency hopping systems.Binary frequency search algorithm (B-FSA) has been widely used in many AFCs because of its simple structure and relatively fast calibration time [6]–[11]. Using successive the AFC holds the current cap-bank code. The frequency holding window is typically set to be equal to frequency resolution in the B-FSA, i.e., $f H = f$RES.

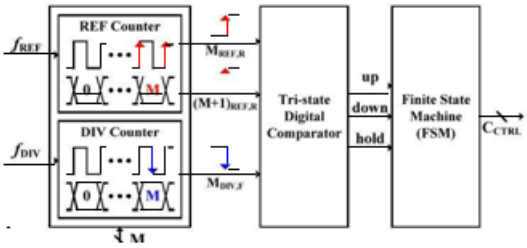
In other words, if the target frequency fT is

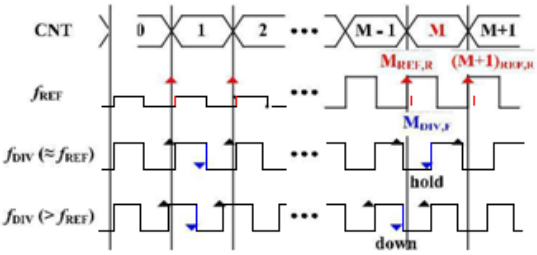
$$f H \quad \text{VCO} - 2 \leq fT \leq f\text{VCO} + 2 \qquad (1)$$

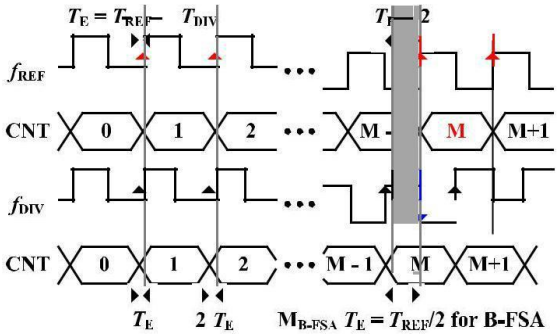
If the target frequency is set to fT 1, as in the top part of Fig. 2(a), the AFC shifts the cap-bank code from 8 to 12, and holds the code until calibration ends. If, on the other hand, the target frequency is fT 2, the AFC will have to perform three frequency comparisons, shifting the cap-bank code from 8 to 4, then to 6, and finally to 5. Therefore, for k-bit cap-bank, calibration requires up to $(k - 1)$ frequency comparisons. Fig. 2(b) shows the time-domain VCO frequency shifts during the calibration processes for the target frequen-cies fT 1 and fT 2. The required number of clock counts is the counts is derived later in this section). Therefore, the total AFC calibration time (tAFC) is linearly proportional to the number of cap-bank bits. The total PLL lock time (tPLL) is the sum of the AFC calibration time and the PLL fine-tuning time. Since the coarse and fine-tuning processes are independent of each other, we will only deal with the AFC calibration time in the rest of this paper.











In this paper, an A-FSA is proposed for automatic frequency calibration in wideband PLLs with multibit cap-bank VCOs. Using a reduced number of clock counts to determine each bit of the cap-bank, the A-FSA achieves faster frequency calibration than a conventional B-FSA. The additional circuitry required for the A-FSA is only a DCVC, minimizing hardware overhead. Circuit simulations using a 5-bit cap-bank VCO confirms that the frequency calibration time of

the proposed A-FSA is less than half the time spent in a B-FSA.

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