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Survey on High Speed Low Power Full Adder Circuits

Shrivathsa B
Student of E&C Department
SCEM
Mangalore, India

Kiran Kumar V.G.
Associate Prof. E&C Department
SCEM
Mangalore, India

Nisha
Asst. Prof. E&C Department
SCEM
Mangalore, India

***Abstract*--- The performance of an adder has a major effect on the overall performance of a digital system. The adder is the digital circuits which perform addition of the numbers. In many processors and controllers, the adders are used to do the arithmetic and logical operations in the ALU. As the technology is scaled down continuously, several techniques are implemented to reduce power dissipation with high-speed operation. In this paper, the various low power full adder circuits with high-speed operation have been analyzed. The adder is the fundamental building blocks of arithmetic circuits. An arithmetic circuit is the combination of many adders. Therefore a little amount of power savings or reduction in delay times leads tremendous power saving and better performance of the overall circuit. There are several design techniques and methods are available for low powered high-speed full adders. Some of the design techniques are analyzed in this paper.**

Keywords—Power Delay Product (PDP); Gate Diffusion Input (GDI); Transmission Function Full Adder (TFA); Static Energy Recovery Full Adder (SERF); Arithmetic Logic Unit (ALU).

I. INTRODUCTION

The power consumption factor is important while designing high-speed portable devices. Nowadays designing a low power, high-speed VLSI system has given more importance due to fast-growing portable devices. The power consumption and performance of the circuits are the major trade-off factors in low power VLSI design. The efficiency of implementation of arithmetic circuits affects the performance of overall integrated circuits and digital signal processors. The efficiency of implementation of arithmetic circuits in the execution of dedicated algorithms largely affects the performance of processors and application specific integrated circuits.

The increasing density of transistors results in complexity in the integrated circuits demands high speed, power efficient designs. The researchers have developed number of CMOS Logic styles to improve the performance and to lower the power dissipation in the VLSI chips. All these researches helped to meet the constraints of the rapidly growing industry. The easiest method to reduce the power dissipation of the circuits is to by minimizing the supply voltage thereby reducing the operating voltage of the circuit. But reducing the operating voltage leads to degraded driving capability and increased circuit delay of the cells.

The performance of many applications such as digital signal processor, ASIC depends upon the performance of the arithmetic circuit to execute complex algorithms. Arithmetic and logical operations like convolution, correlation, and digital filtering are executed using arithmetic circuits.The processors and integrated systems commonly consist of adders and multipliers which are most frequently used for fast arithmetic computation. Full adders are not only used to perform arithmatic operation but also in calculating adresses, building block on the chip library. The power consumption of full adder has to be reduced so that overall all power consumption of the chip is reduced. Performance of the circuit reduced due to propagation delay, therefore propagation delay needs to be optimized to get high-speed operation.

Section II consists of a literature review of full adder circuit designs and the Section III consist of a comparison of different full adders. Conclusion in sections IV.

II. Literature Review of Full Adder Circuit Designs

The several power optimization methods and different digital circuit design are discussed in this chapter.Different important sources which cause power dissipation in CMOS circuits are also reviewed in this paper. Techniques to reduce the effect of such sources in different research articles are discussed here. There are two types of styles, they are static style and dynamic style.

Full adder with full voltage swing and full adder without full swing adder are two types of full adder logic based on their output voltages. The output of full swing adder circuit has less noise output and example for this are C-CMOS, CPL, TGA, TFA, Hybrid, 14T, and 16T. It uses XOR/XNOR circuit to reduce the number of transistor in circuit there by it reduces area occupied and helps in power savings. 10T, 9T, and 8T are full adders without a full swing in which the output voltages are not full swing. Full swing adders has better performance but larger circuits are constructed using non-full swing adder because it occupies less area. High speed transistor with low power consumption adder cells are generally constructed using pass transistor and C-MOS logic styles.

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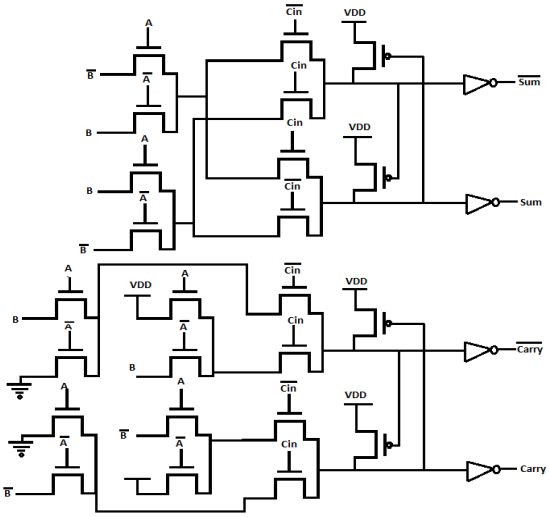

Fig 1: Complementary Pass-Transistor

Complementary Pass transistor (Fig 1) logic (CPL) [1] is that the pass transistor has an input in its source side.The Complementary Pass-Transistor (CPL) technique which generates complemented outputs in same design like AND/NAND, OR/NOR and XOR/XNOR together. In this technique it uses only pass transistor logic due to this it has small input capacitances and high function design with less number of transistors. But in order to stop degradation of performance additional circuits like swing restoration circuit and dual-rail encoding are used. CPL logic is more preferable than the CMOS logic but not than the C-CMOS, due to threshold voltage drop. Also, this logic requires inverters in the output stage for getting enough drivability.

C-CMOS full adder (complementary CMOS) consist 28 transistors and works based on CMOS structure (Fig. 2)which is a amalgamation of pull up and pull down networks to produce outputs[2]. It has stable operation even at low voltages and robustness aginst transistor scaling. Due to high transistor count, there is problem of delay imbalance and it consumes more area and power. The delay is produced due to Sum signal need to rely on generation of carry signal.

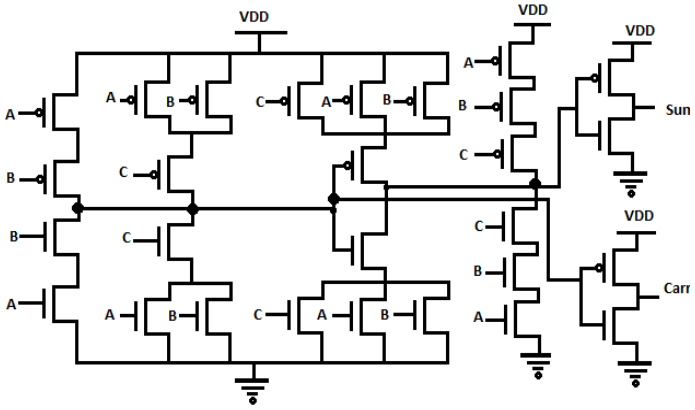

Fig 2: Complementary CMOS

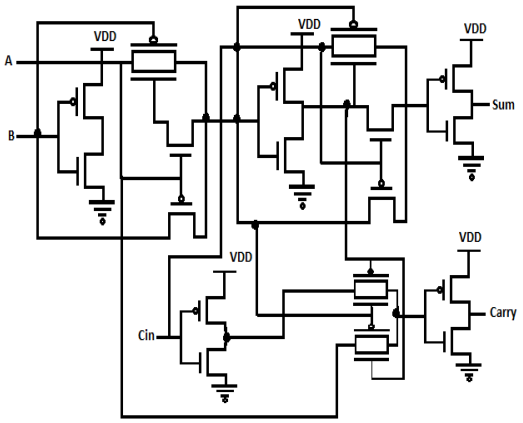

Fig 3: Transmission Function Full Adder (TFA)

Total 16 transistors are used in TFA or Transmission Function Full Adder (Fig 3) which consists A, B, Cin as inputs to produce outputs as sum and carry [4]. NMOS transistor is used as pull down network and PMOS transistors used as pull up network. This adder has no problem with voltage drop. TFA adder has less power consumption [5] and the disadvantages are lack of driver capability and requires more number of transistors.

14T Full Adder is the combination of pass-transistor and TG techniques to produce full adder output. 14T Full Adder (Fig 4) has 14 transistors and it has three inputs to produce sum and carry as output. The full swing carry voltage and non-full swing sum voltages are produces as output by making uses of pass transistor logic and XOR/XNOR circuit. The carry is produced by transmission gate and sum by pass transistor logic. To achieve better speed and power it sacrifies four transistors per adder cell. But still there is increase in transistor number. Better cascading capability, low power consumption, and higher operating frequency are the advantages in 14T [6].

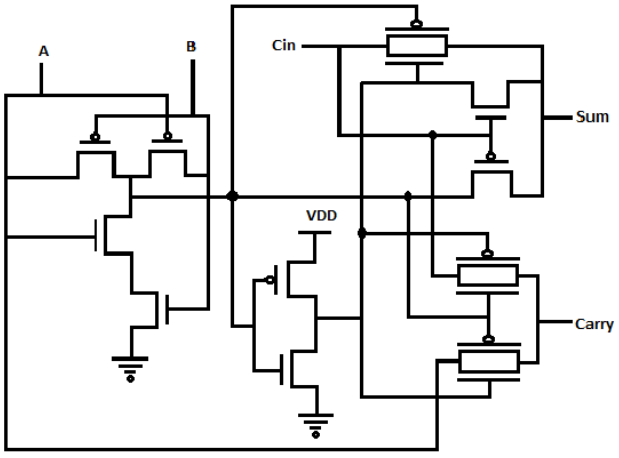

Fig 4: 14T full adder

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Static Energy Recovery Full Adder or SERF (Fig 5) consist 10 transistor and this adder performs good even at higher voltages.The advantage of SERF is it does not requires inverted input signals like other types of full adders and it uses energy recovery technique for power saving purpose. When the voltage value reaches lower than 0.3V SERF adder fails to works at this extreme low voltages[7]. Power consumption of this is low because there is no direct path to ground.

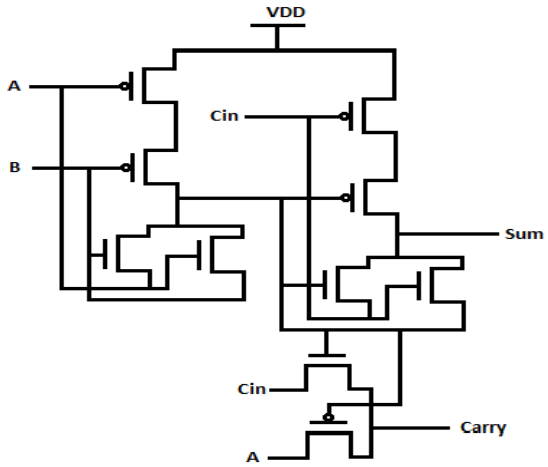

Fig 5: SERF

Multiplexer Based Full Adder which is also called as MB12T [9] (Fig 7). MB12T has 12 transistors which acts as 6 multiplexers. One multiplexer are implemented using two pass transistor logic. Therefore 6 multiplexer can be implemented using12 pass transistors in MB12T. In Multiplexer Based Full Adder the short circuit power that produced in the circuit can be reduced. since this circuit has no supply voltage and ground connection. But this method produces high delay due to high fan out.

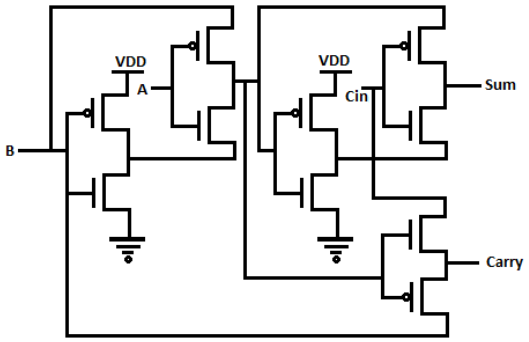

Fig 6: GDI full adders

Gate Diffusion Input Full Adder or GDI full adder (Fig 6) has three inputs signals, namely G (gate input), N (nmos input) and p (pmos input). GDI method is used for low power digital circuit design. It has 10 transistors [9] and It is the high performance and low power full adder. GDI cell requires extra process like twin-well CMOS or silicon on insulator (SOI) for opearting is main disadvantage of GDI full adder

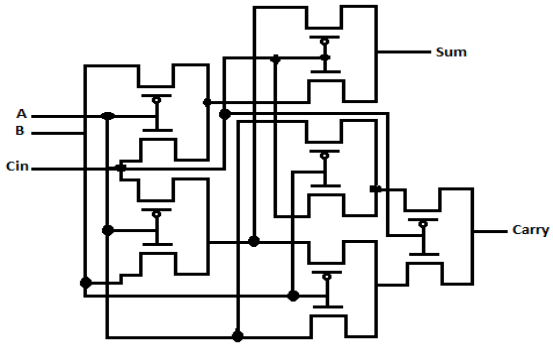

Fig 7: MB12T

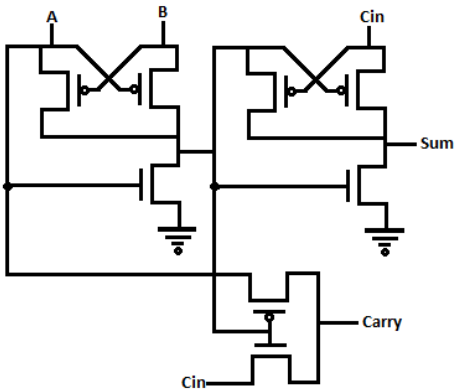

Fig 8: 8T full adder

8T full adder [10] adder consists of 3T XOR gates and contains 8 transistors. Therefore its manufacturing cost is less. There are 2 transistors in Carry module and 6 transistors in sum module. Due to less number of the transistor, it requires less area and also performs at high speed. The disadvantage of the 8T method is that three input capacitances are used to implement different functions.

III. COMPARISON OF DIFFERENT FULL ADDERS

The comparison between all the full adders are shown in below table.

Design	Delay (ns)	PDP (aj)	No. of transistors
CPL	138.70	189.31	32
C-CMOS	143.13	135.68	28
TFA	141.92	148.38	18
14T	792.42	529.17	14
SERF	401.05	695.88	10
GDI	286.33	96.93	10
MB12T	252.35	94.38	12
8T	178.50	74.79	8

When comparing the delay CMOS and TFA produces almost delay compared to other types of adders. 14T produces more delay and CPL produces the least. The increase in delay time of the circuit and power dissipation produces more PDP delay. SERF and 14T full adders has higher PDP delay in comparison with other types of adder circuits. The CMOS, TFA, CPL, and MB12T have lower PDP and gives almost

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similar results. In that SERF has worst delay time. C-CMOS and CPL uses more a number of transistors. TFA uses more transistors compared to 14T and MB12. SERF and GDI use 10 transistors.

IV. CONCLUSION

A survey is done for different design methodology of a full adder. Also, Comparison of different full adders in terms of delay time, PDP and a number of transistors are done. Based on a survey that the new 8T consume less power and have high speed compare to all other designs which works at the low supply voltage and it also has a good signal level. Other than 8T configuration MB12T and GDI also has low PDP and less number of transistors. But 8T is preferred over other type of full adder circuits. Due to very low power consumption and very high-speed performance 8T circuit is suitable for arithmetic circuits and other VLSI applications Depending on the application, one has to choose best full adder for better performance.

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