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Study of SRAM Cell for Balancing Read and Write Margins in Sub-100nm Technology using Noise-Curve Method

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Abstract*—In this paper we perform a study of 3 SRAM cell architectures, namely conventional (single port) 6T (6-transistors), 8T (8-transisitors) and 9T (9-transistors) both with dual ports, to review and evaluate Static Noise Margin (*SNM*) at low operating voltages. These cells are simulated using SimuCad EDA tool by Silvaco, using generic 90nm process design kit (PDK). It is observed that the 6T SRAM cell suffer from poor writability and severe read disturbance. The write margin of the 8T SRAM cell considered in this paper is comparable with 6T SRAM, having superior read stability. The 9T SRAM cell has superior read and write margins even at extremely scaled supply voltage, V_{DD}. The implication of cell transistor widths on the cell stability and power dissipation are analyzed based on the noise curve technique at V_{DD}=1V. For conventional 6T SRAM, the sensitivity of its 'static power noise margin' (*SPNM*) to NMOS pull down transistor width (W_{dn}) is *1.3µW/µm* and *5.5µW/µm* when W_{ac}=W_{pu}=0.4µm and 2µm respectively, where W_{ac} and W_{pu} are the widths of the NMOS access and the PMOS pull up transistors, respectively. For the same 6T cell, the sensitivity of 'write trip power' (*WTP*) to W_{dn} is *3.7µW/µm* and *3µW/µm* when W_{ac}=W_{pu}=0.4µm and 2µm, respectively.

***Keywords*: Read stability, Write margin, Static voltage noise margin, Static current noise margin, Write trip voltage, and Write trip current.**

I. INTRODUCTION

Modern microprocessor units (MPUs) have multilevel cache for achieving high throughput of instruction execution for performance critical applications such as digital signal processing, modern Internetworking, etc. The overall integrated circuit (IC) process flow integration for logic and SRAMs have a better compatibility as against the logic versus embedded DRAMs (eDRAMs) [1]. This makes SRAMs a suitable choice for cache, over eDRAMs in the modern MPUs [1, 2]; but the SRAMs are known to be power hungry. To reduce SRAM power consumption, one of the well known approaches is to lower the 'cell-V_{DD}' (CV_{DD}) [3].The reduction in CV_{DD} results in decreased static noise margin (*SNM*) [3, 4]. The estimation of SRAM cell metrics such as read stability and writability based on cell static noise margin (*SNM*) is too pessimistic because the *SNM* approach assumes static noise; in reality the noise will appear at discrete instants, lasting for a short duration when once it appears [5]. The *SNM* metrics characterize the noise margin of an SRAM cell only during its hold state [3, 5]. The *SNM* has the drawback of disregarding its time dependence during read and write operations [5, 6].

The read and write margins that are statically determined, cannot predict dynamic read and write margins of the SRAM cell. During the normal cell access, the wordline (*WL*) is pulsed to V_{DD} for T_{WL} duration. We succeed in cell access, if and only if the cell response time T_R<T_{WL} for both read and write operations [3, 5, 7]. The T_R is a random variable across the array, which is a function of process variations. So the T_{WL} must have sufficient margin to include the maximum T_R i.e. $T_R+3\sigma_{T_R}$, where σ_{T_R} is its standard deviation [5].

The dynamic read and write margins of SRAM cell are also functions of various other parameters such as CV_{DD}, threshold voltage V_T of the cell transistors, cell ratio $CR=\beta_{dn}/\beta_{ac}$, and β ratio $BR=\beta_{ac}/\beta_{pu}$, where β_{dn}, β_{ac}, and β_{pu} are the transconductance parameters of the pull down, access, and pull up transistors, respectively [8]. For a reliable read and write operations both the *CR* and *BR* should be greater than 1.

The 'noise-curve' or 'N-curve' (*NC*) method is one of the practical inline measurement techniques used to determine the cell stability [6]. In this method a set of *NC*-parameters, namely 'static voltage noise margin' (*SVNM*), 'write trip voltage' (*WTV*), 'static current noise margin' (*SINM*), and 'write trip current' (*WTI*) are derived from the *NC*. The *NC*-parameters finds good correlation with the cell *SNM*. They also provide additional information about cell such as 'static power noise margin' (*SPNM*) and 'write trip power' (*WTP*) [5, 6, 9] which are calculated using the *NC*-parameters. The *SPNM* and *WTP* metrics provide deeper insight into the cell power consumption during the read and write operations, respectively. The *NC* is essentially the cell I-V (current–voltage) relation determined by sweeping the voltage at the internal '0' node of the cell, under certain bias conditions, discussed later. The *NC* enables extraction of all the *NC* parameters at relevant coordinates of *I-V* plane.

This paper is organized as follows: Section-II gives an overview of the conventional single port 6T, 8T and 9T cells both with dual ports. Section III presents the fundamentals of the N-curve methodology used to determine the various *NC* parameters of the SRAM cell. Section IV discusses on various *NC* parameters extracted using the methodology of section III. In section V, conclusion is drawn with a discussion on the observations made and its novelty.

II. An Overview of conventional 6T, Dual port: 8T and 9T SRAM Cells

Aggressive scaling of device dimensions and voltage gives rise to unacceptable variability in SRAM cell characteristics. The *SNM* is a function of V_{DD}, threshold voltage V_T, *CR* and *BR*. The variability in these parameters translates directly to variability in *SNM* [4, 8]. The increased 'variability' σ_{V_T} in V_T due to random dopant fluctuation (RDF) is very severe in sub-100nm MOSFETs [4, 6]. Finally, this variability has severe implications on yield of SRAM chips [4, 10-13].

While going beyond sub-100nm technology node, dual port 8T and 9T cell architectures will be of choice to achieve the required read stability and writability [3]. In this paper the discussion and analysis of dual port 8T and 9T SRAMs follows the earlier reports from [3, 7].

Fig. 1(a) shows the conventional 6T SRAM cell, connected to bitlines *BL*, *BLB* and the wordline *WL*. The storage action is accomplished by two inverters on left and right sides, built using a pair of transistors *M1-M3*, and *M2-M4*, respectively. The *BL* and *BLB* contents will be written to *Q* and *QB* nodes via. the access transistors *M5* and *M6* when their gates connected to *WL*, is pulsed. The reading of the cell content (from *Q* and *QB* nodes) is done by precharging both the *BL* and *BLB* bitlines to V_{DD} normally, followed by pulsing of the wordline, *WL*. The complementary bits stored in the *Q* and *QB* nodes develop a differential voltage δV across *BL* and *BLB* through charge sharing effect. The voltage δV is amplified by a sense amplifier to interpret the bits stored in the cell.

The read stability and writability are very important metrics that characterize SRAM cells. During the read operation, the cell bits are flipped due to read disturbance mainly at the internal '0' node (i.e. the node holding '0' bit). At this node the precharged *BL* and *BLB* lines develop a voltage above V_{TRIP} also called inverter threshold voltage. When this condition is met, the back to back connected left and right side inverters will enter into a regenerative feedback action, eventually flipping the cell bits. For the SRAM cell to flip, the feedback has to be maintained for a minimum duration of cell response time T_R. The condition of $T_{WL} > T_R$ must be satisfied for a successful read and write operations [5]. The V_{TRIP}, voltage defined earlier related to V_{DD} and transconductance parameters of *M1-M3* or *M2-M4* (Fig. 1) is given as:

$$V_{TRIP} = \frac{V_{DD} + V_{Tn}\sqrt{\frac{\beta_{dn}}{\beta_{pu}}} - |V_{Tp}|}{1+\sqrt{\frac{\beta_{dn}}{\beta_{pu}}}} \qquad (1)$$

where β_{dn} and β_{pu} are the transcoductance parameters of pull down (*M1* or *M2*) and pull-up (*M3* or *M4*) transistors, respectively in the SRAM cell of Fig. 1(a). V_{Tn} and V_{Tp} are the threshold voltage of the *M1* (or *M2*), and *M3* (or *M4*) transistors, respectively. From Equation (1)$V_{TRIP} = \frac{V_{DD}}{2}$, when $|V_{Tn}|=|V_{Tp}|$ and $\beta_{dn}=\beta_{pu}$. When the access transistors *M5* and *M6* are turned ON by pulsing the *WL*, the internal '0' node will try to rise above ground potential. If this rise reaches V_{TRIP} level given by Equation 1, it leads to read disturbance, eventually flipping storage node (*Q* and *QB*) bits, which has its implications over W_{dn}.

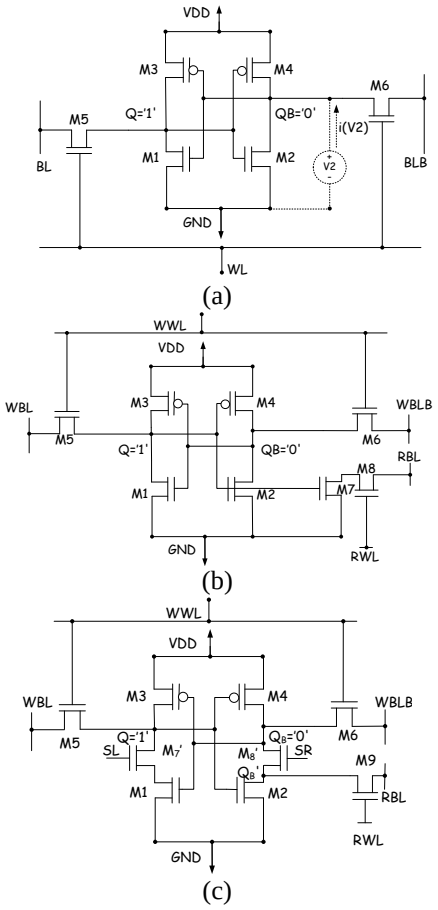


Fig. 1: Various SRAM cell topologies (a) Conventional 6T, (b) Dual port 8T, and (c) Dual port 9T. Note: GND is the ground terminal.

The cell ratio *CR* and beta (β) ratio *BR* defined earlier will characterize read stability and writability of the SRAM. Balancing the dynamic read stability and dynamic writability requirements in 6T SRAMs considering the critical timing of various signals such as *WL*, *BL*, *BLB*, etc., is very challenging. In view of addressing the read stability and writability issues, the SRAM cell architecture has evolved to advanced dual port 8T and 9T architectures. These cell architectures overcome the challenges that arise in sub-100nm conventional 6T SRAM cells using 'write-assist' and 'read-decouple' techniques. These techniques are explained for 8T and 9T cells shown in Fig. 1(b) and Fig. 1(c), respectively.

Fig. 1(b) and Fig. 1(c) presented in this paper are dual port 8T and 9T SRAM cells developed for low power applications, as reported in [3]. Fig. 1(b) shows an 8T cell with independent read and write ports which is a modification of the conventional 6T SRAM cell of Fig. 1(a) by the addition of transistors *M7* and *M8*. The read and write operations are performed through two mutually exclusive datapaths (ports), one for writing into cell similar to *BL/BLB* bitlines of conventional 6T SRAM cell, while the other datapath is a single ended read port *RBL*, decoupled from the internal storage nodes (*Q/QB*). When the write wordline *WWL* is pulsed, the write bitline *WBL*/*WBLB* voltages will be written into the *Q/QB* storage nodes of the cell. This write operation is similar to writing in the conventional 6T SRAM of Fig. 1(a).

The 8T cell decouples the storage nodes while reading, using *M7* and *M8* transistors. When the gate of *M8* transistor *RWL* is pulsed, the internal storage node voltage causes the voltage on the precharged *RBL* bitline to change (by δV), which is sensed and amplified to logic levels corresponding to 0V or V_{DD}. The gate of *M7* transistor provides the necessary read decouple of *RBL* from *Q/QB* storage nodes. However, this 8T cell does not increase the write margin significantly. This cell is reported to work till a minimum range of V_{DD}*=260-450mV* [3].

The Fig. 1(c) shows a 9T SRAM cell with exclusive read and write datapaths (ports) which works till a minimum V_{DD}*=130mV* [3] corresponding to deep subthreshold operation, and is found functionally successful at this value of V_{DD}. The 6T SRAM of Fig. 1(a) is modified to achieve this 9T cell with a 'write-assist' feature [3, 7] implemented by the addition of *M7'* and *M8'* transistors. The inclusion of these two transistors will provide control over feedback in the basic bistable latch comprising *M1*, *M2*, *M3*, and *M4* transistors. The gate signal *SL* and *SR* of the transistors *M7'* and *M8'* provides the required control in achieving the enhanced write-margin. The inclusion of the transistor *M9* provides the isolation of read port from the internal storage nodes during the read operation.

For dynamic read and write operations, precise timing of various signals in Fig. 1(c) is very important. When a '0' has to be written into internal node *Q*, the *WBL* is low, *WBLB* is high, *SL* is high, *SR* is low, and *WWL* is pulsed. This configuration opens the feedback loop, thereby assisting the write operation. When a '1' has to be written into internal node *Q*, the *WBL* is high, *WBLB* is low, *SL* is low, *SR* is high, and *WWL* is pulsed. The internal node *QB* holds the complement bit of *Q* node.

During the read operation, *M8*' of this 9T SRAM cell is turned off by setting *SR* to 0V. When the *RWL* is pulsed, *M9* connects *QB*' to the read port, *RBL*. As *M8*' is off, nodes *QB* and *QB*' are decoupled. This prevents the voltage rise at node *QB*' passed from *RBL*, and inturn passing to the node *QB*; thus improving the read stability. In hold mode, both *SR* and *SL* are kept at V_{DD} to turn ON the feedback loop of the cross coupled inverters. Thus the hold *SNM* of this 9T SRAM cell is similar to 6T and 8T, but with slight degradation due to stacking.

Fig. 2 illustrates superimposed voltage transfer characteristics (*VTCs*) of the two back to back connected inverters. The separatrix of the SRAM cell is defined as the crossover point of *Q* and *QB* node voltages through which a 45^{o} line passes through as shown in Fig. 2. The *VTCs* of Fig. 2 is also called as butterfly curve [4, 5, 7, 8]. The *SNM* of the SRAM cell is defined as the side of square with smallest diagonal fitted into the eye of the butterfly as shown in Fig. 2.

As reported by Evert Seevinck *et al* [8], the *SNM* of 6T SRAM cell is a lengthy expression with 3 explicit terms; its simplified version is given as:

$$SNM_{6T} = V_T \pm \Delta \qquad (2)$$

where two terms are implicit in Δ, in this equation. In Equation (2), first term is exclusively 'V_T', the second term Δ is a function of V_{DD}, V_T ($\approx V_{Tn} \approx V_{Tp}$), *CR*, and *BR*; thus Δ is inclusive of V_T term again. All these quantities are defined in the earlier section. Thus *SNM* of 6T SRAM cell is directly proportional to V_T and a small fraction ±Δ. The variability of V_{DD}, V_T, *CR*, and *BR* will translate to the variability in the *SNM* of 6T SRAM cell. Maintaining sufficient cell *SNM* across *PVT* (Process-Voltage-Temperature) space and across all the cells is a major challenge in sub-100nm technology nodes [4, 10].

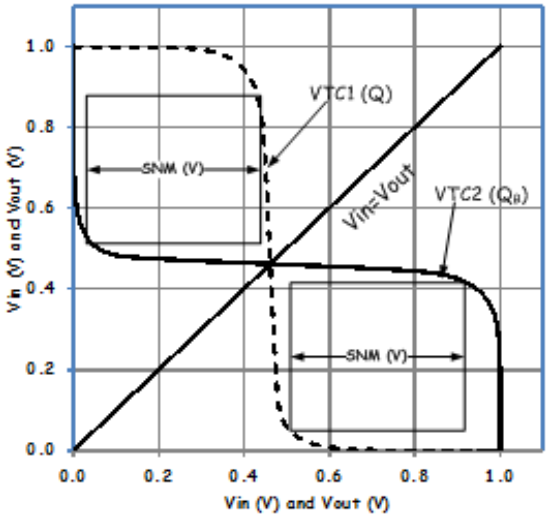


Fig. 2: Butterfly curve for 6T SRAM cell (when the access transistors are off). Inscribed squares in its eye depicted an *SNM* ≈ 0.4V, at V_{DD}=1V. The separatrix point is where the *Q* and *QB* node voltages are same on the line which is drawn through maximum inverter gain of 2 *VTC* curves at ~0.45V.

III. N-Curve Methodology to Determine Noise Margins

The traditional *SNM* method of analysing the SRAM cell stability is having some limitations. First, the *SNM* does not provide a simple means of its inline measurement. Secondly, as it involves only the voltage measurements, it does not provide any information on the cell currents during the cell access and hold states. Third, it fails to provide the dynamic characteristics of the cell, related to the read and write access times. Finally, the *SNM* method is not suitable for measuring large data required for statistical analysis of the SRAM cell characteristics [5, 6, 9].

The definition of read margin and write margin for the 6T SRAM cell (Fig. 1(a)) based on the *NC* method, is suitable for inline tester measurements. The *NC* provides both the current and voltage information, unlike the *SNM* which provides only the voltage information. In this paper the use of *NC* to understand 6T SRAM cell characteristic follows the analysis and interpretation of *NC* by Evelyn Grossar *et al* [6].

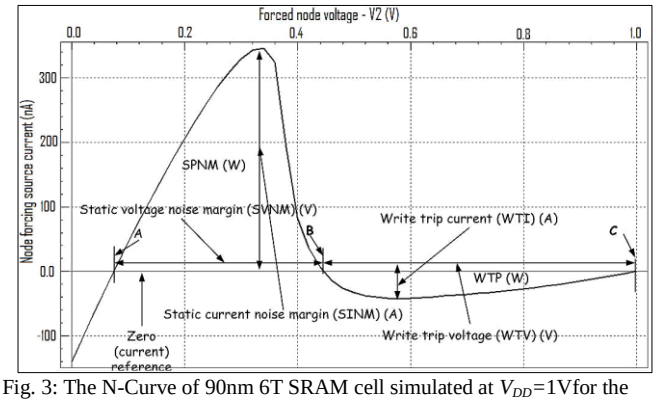


Fig. 3: The N-Curve of 90nm 6T SRAM cell simulated at V_{DD}=1Vfor the circuit of Fig. 1(a).

Fig. 3 shows a *NC* simulated for 90nm 6T SRAM cell with high V_T transistors, at V_{DD}=1V. For plotting the *NC* for the cell structure of Fig. 1(a), the bias conditions are: the *BL*, *BLB* and *WL* are all clamped at V_{DD} to configure the cell in read operation mode. The cell is connected to a variable voltage source V_2 delivering current $i(V_2)$, shown dotted in Fig. 1(a). The V_2 is swept from *0V* to *1V*. The current that is sourced from or sunk into V_2 during the sweep operation results in an *I-V* relation in the form of *NC*, as shown in Fig. 3

In three points A, B and C of the N-curve in Fig. 3 the current injected into the storage node is zero. The A and C points correspond to the two stable points of the butterfly curve of Fig. 2, and the point B corresponds to the separatrix (≈0.45V). When the points A and B are very close, the cell is at the edge of destructive read. The voltage difference between points A and B is called 'static voltage noise margin' *SVNM* indicates the maximum tolerable DC noise voltage by the cell before its contents flip (i.e. the static read margin). The peak cell current between the points A and B is the maximum current the cell conducts before flipping, is called 'static current noise margin' *SINM*. By using the combined *SVNM* and *SINM* metrics, the read stability criterion for the cell is defined properly. The area under the *NC* between the point A and B is called the 'static power noise margin' *SPNM*, which signifies the power consumed during read operation.

The region of *NC* between the points B and C in Fig. 3, defines the write-margin of the SRAM cell. The voltage difference between the points B and C is called the 'write trip voltage' *WTV*. The value of *WTV* indicates static write margin. The maximum magnitude of the negative current between the points B and C is called the 'write trip current' *WTI*. The area under the *NC* between the points B and C is called the write trip power *WTP*, which signifies the power consumed during the write operation.

IV. Results and Discussion

We have performed power analysis of 6T SRAM cell (Fig. 1(a)), in terms of *SPNM* and *WTP* both as functions of various cell transistor widths. This study is performed using SmartSpice circuit simulator of SimuCad EDA tool from Silvaco. For all the circuit simulations (at V_{DD}=*1V*), we have used generic 90nm process design kit (PDK). For power analysis, we have used *NC* method which involves extraction of *NC* parameters: *SVNM*, *SINM*, *WTV* and *WTI* (as defined earlier). Using the *NC* parameters we calculate the *SPNM* and *WTP*, as a measure of read and write power margins, respectively. Calculation of *SPNM* and *WTP* is done by evaluating the area under *NC* between the points A and B, and B and C, respectively as shown in Fig. 3.

Fig. 4 shows two sets of *NCs* corresponding to two different values of the pull up and access transistor widths W_{pu} and W_{ac}, respectively, with W_{pu}=W_{ac} in both cases. For W_{pu}=W_{ac}=0.4µm, W_{dn} is varied from 0.4µm to 2µm, in steps of 0.4µm, resulting in 5 *NCs* labelled 'Case-1' in Fig. 4. A second set of *NC*s labelled 'Case-2' are obtained with W_{pu}=W_{ac}=2µm, with W_{dn} varied over the same range and step size as in Case-1. In Case-1 it is noticed that 3 out of 5, *NCs* have well defined *NC* parameters with 2 curves not showing positive peaks, and hence we cannot extract *SVNM* and *SINM* for them. In Case-2 we have all the 5 *NCs* showing well defined positive and negative peaks for which we have extracted all the *NC* parameters. The gate length L_g=*90nm* for all the cell transistors in both the cases.

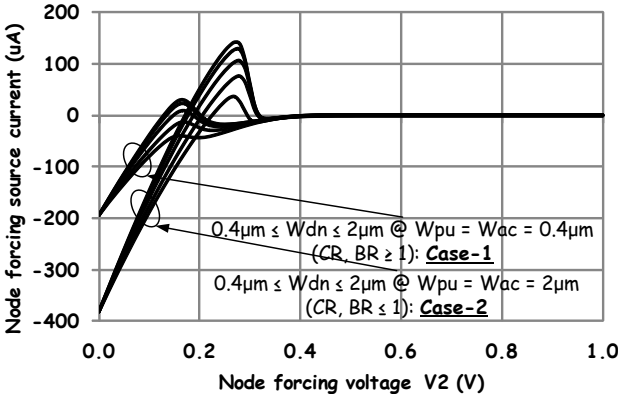


Fig. 4: Two sets of N-curves corresponding to two values of the width of pull up and access transistor. Each set is obtained by varying the width of the pull down transistor from 0.4µm to 2µm in steps of 0.4µm.

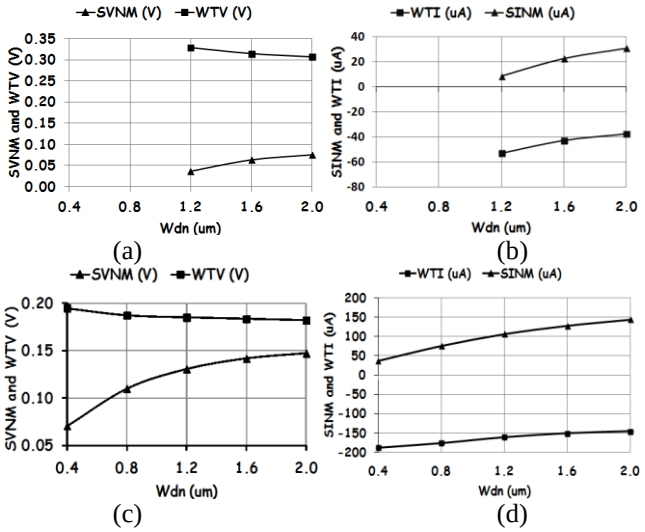


Fig. 5: The parameters extracted for two sets of *NCs* labelled: Case-1 and Case-2 (Fig. 4) plotted as a function of pull down transistor width. (a) Plots of *SVNM* and *WTV* for Case-1, (b) Plots of *SINM* and *WTI* for Case-1, (c) Plots of *SVNM* and *WTV* for Case-2, and (d) Plots of *SINM* and *WTI* for Case-2.

In Fig. 5 we have plotted the *NC* parameters extracted from the two sets of *NCs* labelled Case-1 and Case-2 in Fig. 4 as a function of pull down transistor (*M1* in Fig. 1) width W_{dn}. Fig. 5(a) shows the plots of *SVNM* and *WTV* for Case-1, Fig. 5(b) shows plots of *SINM* and *WTI* for Case-1, again. Fig. 5(c) shows the plots of *SVNM* and *WTV* for Case-2, and in Fig. 5(d) *SINM* and *WTI* are plotted for Case-2. From this graph, it is seen that as *SVNM* increases from relatively smaller value, *WTV* decreases with W_{dn}. This trend explains the fact that, as the static read margin increases the static write margin decreases.

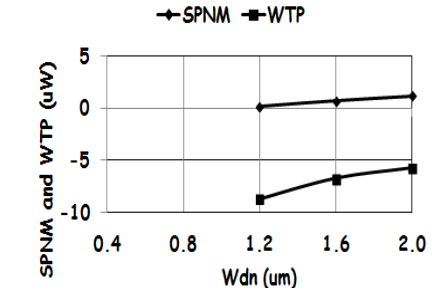
In Fig. 5(c) and (d), trends similar to Fig. 5(a) and (b) are noticed in the plots of *SVNM*, *WTV*, *SINM*, and *WTI*, but the currents in this case are proportionately high due to larger transistor widths (with W_{pu}=W_{ac}=2µm), with W_{dn} again in the same range i.e. 0.4µm≤W_{dn}≤2µm and same step size of 0.4µm. This study would provide a basis in balancing the static read and write margins of 6T SRAM cells.

Important point to note from Fig. 5 is that the *SVNM* and *WTV* are relatively higher, and *SINM* and *WTI* are relatively lower for Case-1, when compared with that in Case-2.

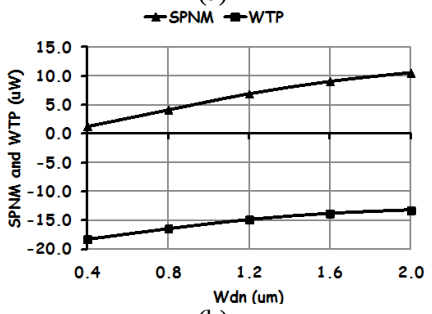
Fig. 6 is the plot of *SPNM* and *WTP* as a function of W_{dn}, with $0.4\mu m \leq W_{dn} \leq 2\mu m$. Fig. 6(a) corresponds to Case-1 and Fig. 6(b) corresponding to Case-2. An important point to note from Fig. 6 is that, as the widths of the transistors are increased the cell power consumption is increasing.

From Fig. 6 we have calculated the average sensitivity of *SPNM* to W_{dn} which is $1.3\mu W/\mu m$ and $5.5\mu W/\mu m$ when $W_{ac}=W_{pu}=0.4\mu m$ and $2\mu m$ respectively. The average sensitivity of *WTP* to W_{dn} is $3.7\mu W/\mu m$ and $3\mu W/\mu m$, when again $W_{ac}=W_{pu}=0.4\mu m$ and $2\mu m$, respectively.

The above *NC* technique can also be applied to 8T and 9T SRAM cells that are discussed in earlier section, in a similar manner.



(a)



(b)

Fig. 6: The static power noise margin *SPNM* and the write trip power *WTP* for the two sets of N-curves labelled Case-1 and Case-2 in Fig. 4 are plotted as a function of W_{dn}. (a) *SPNM* and *WTP* versus W_{dn} for Case-1, and (b) *SPNM* and *WTP* versus W_{dn} for Case-2.

V. Conclusions

We have performed the extraction of *NC* parameters (i.e. *SVNM*, *SINM*, *WTV*, and *WTI*) for 90nm, 6T SRAM cell. The *NC* based 'static power noise margin' *SPNM* and 'static write trip power' *WTP* are considered as metrics to determine the read and write access powers. For 6T SRAM, the sensitivity of *SPNM* to W_{dn} is $1.3\mu W/\mu m$ and $5.5\mu W/\mu m$ when $W_{ac}=W_{pu}=0.4\mu m$ and $2\mu m$, respectively. The sensitivity of *WTP* to W_{dn} is $3.7\mu W/\mu m$ and $3\mu W/\mu m$, again when $W_{ac}=W_{pu}=0.4\mu m$ and $2\mu m$, respectively. These sensitivities highlight the efforts required to determine the right transistor widths to balance and minimize the cell *SPNM* and *WTP*, simultaneously. The *SPNM* and *WTP* parameters determined in this work, have given a deep insight into the order of worst case power dissipation in the 90nm SRAM cells. We have also reviewed dual port 8T and 9T SRAM cells [3, 6], qualitatively. The qualitative analysis of these two cell architectures has provided a deep insight into their low power capabilities, especially with a highlight on deep subthreshold operational capability of 9T SRAM cell.

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