Study of Different Types of Analog Comparator Topologies in CMOS Technology

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***Abstract*- Comparator is one of the most important analog circuits required in many analog ICs. It is mainly used for the comparison between two dissimilar or same electrical signals. The design of comparator comes to bean important issue when technology is scaled down. Due to the non-linear etiquette of threshold voltage (VT) when technology is reduced, performance of Comparator is afflicted. Many versions of comparator are proposed to achieve desirable output in sub-micron and deep sub-micron technologies. The preference of particular design is dependent upon the requirements and application. In this we will simulate all types mentioned types of comparators and analyze them on the basis of different characteristics of comparator like: power dissipation, offset voltage, delay, speed and no. of transistor used. The simulation will be in HSPICE. The proposed comparator will be low power comparator compared to all comparator mentioned here.**

Keywords- Double tail latch type comparator, dynamic comparator , pre amplifier based comparator , dual tail double rail type comparator, power dissipation, offset voltage, delay, speed, no. of transistors used, low power analogue design.

I. INTRODUCTION

In electronics, Operational amplifier is designed to be used with negative feedback. It can be also used as comparator in open loop configuration. On the other hand, Comparator is especially designed for open loop configuration without any feedback. Hence it is the second most widely used device in electronic circuits after Opamp. Comparators are mostly used in analog-to-digital converter (ADCs). In the conversion process, first the input signal is sampled. Then the sampled signal is applied to a number of comparators to determine the digital equivalent of the analog value. Apart from that, comparators are used in peak detectors, zero crossing detectors, BLDC operating motors, switching power regulators

A. Definition :

Comparators are the device that compares two analogue voltages or currents and switches it output to indicate which one is larger.

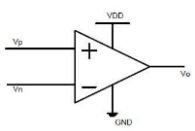

Figure 1 Opamp based comparator

If VP is at a greater potential than VP, then the output Vo of the comparator is logic 1 and when VP is at a potential less than Vn, then the output is at logic 0.

If we apply a pulse voltage at VP and a DC reference voltage at Vn, the output is logic 1 when the pulse amplitude is greater than the reference voltage. The figure is shown below. Thus a comparator compares two input analog value and gives binary output. In ideal case, binary signals can have two values at any point. But actually there is a transition region between the two binary states. For a comparator, it is important to pass quickly through that transition region. Basically comparators can be divided into two types. First are the Open loop comparators, which are nothing but OPamps. The second type is regenerative comparators. Regenerative comparators use positive feedback for the comparison of magnitude between two signals

Nowadays, where demand for portable battery operated devices is increasing, a major importance is given towards low power methodologies for high speed applications. Also we have to minimize the power consumption by using smaller feature size processes. However when we move towards power consumption minimization, the process variations and other parameters will greatly affect the overall performance of the device. Now comparators are used in ADCs and ADCs.

In this project paper .preparing a table of comparators which give information of all types of comparator, which can help designer to choose better comparator for their design‘s parameter and there requirements. The different parameter has compared as per information collected and along with comparing the comparator, the designing of low power comparator will be designed in HSPICE.

Comparator is one of the most important analog circuits required in many analog ICs. It is mainly used for the comparison between two dissimilaror same electrical signals. The design of Comparator becomes an important issue when technology is reduced. Due to the non-linear etiquette of threshold voltage (VT) when technology is reduced, performance of Comparator is afflicted. Many versions of comparator are proposed to achieve desirable output in sub-micron and deep sub-micron technologies. The preference of particular design is dependent upon the requirements and uses. This paper shows the implementation of dissimilar topologies in 0.5 µm technology using the different Tool. We

have performed Direct current, Alternated current and transient analysis. We have calculated output impedance too. We have prepared a comparative analysis about them.

Basic comparator the most basic version of the Comparator is the source follower. It is a common drain amplifier circuit with unity voltage gain.The input at the gate is followed by output at the source terminal. The figure.1 shows the schematic of the circuit. It is designed with the N type MOS, P type MOS and ideal source of current. We can use current mirror in place of sourceof current too. Because of constant current flow is not allowed through source terminal that's why comparator can be not designed with a resistor connected between source and supply. Because of thisoutput becomes nonlinear and we can't achieve unity voltage gain many times. Ithas high output impedance too. So,configuration in which resistor is applied can be not used. We can use P type MOS or N typeMOS as a load. But, the implementation in which current mirror is used gives better results.

II. CHARACTERISTICS OF COMPARATOR

A. *Static Characteristics:*

Static characteristics comprises of gain, output high (VOH) and low states (VOL), InputResolution, Offset and Noise

1) ***Gain*****:** Gain of comparator can be written as:

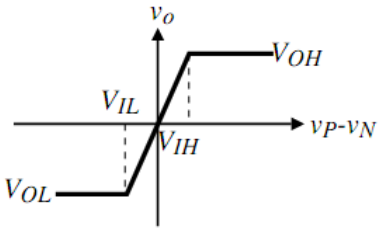

Figure 2.1 First-Order Model of Comparator

$$\text{Gain} = A_v = \lim_{\Delta V \to 0} \frac{V_{OH}-V_{OL}}{\Delta V}$$ where ΔV is the input voltage change

2) *Input Offset Current:*The offset current at input is the difference between theseparate currents entering the input terminals of a balanced amplifier.

3) *Input Offset Voltage****:*** The input offset voltage is that voltage which must beapplied between the input terminals ,So the amplifier is to be balanced

4) ***Noise*****:** Noise of a comparator is modelled as if the comparator were biased in thetransition region. Noise increases to an uncertainty in the transition region which causes jitter.

B. *Dynamic Characteristics:*

Dynamic characteristics of the comparator consist of Propagation delay and Gain.

1) *Propagation delay :*

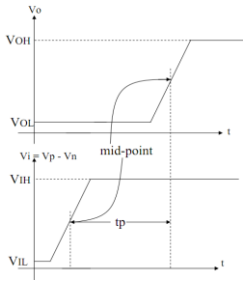

Figure 2.2 Propagation Delay Time of Comparator.

Propagation time delay= (Rising Propagation Delay time +Falling Propagation Delay Time) /2

2) *Slew Rate****:***

Slew rate can be defined as the rate of change of output voltage with respect to time.

SR= dVout/dt

III DIFFERENT COMPARTATOR

A. *Pre amplifier based comparator*

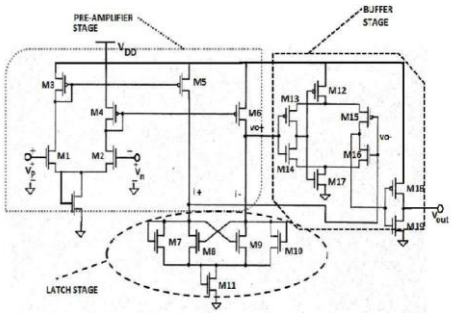

Figure 3.1 Pre amplifier based comparator

Operation: The figure shows the preamplifier based comparator. The comparator consists of three stages: the input preamplifier stage, a latch stage, and an output buffer stage (it is basically a self-biased differential amplifier followed by an inverter which gives the digital output.The preamplifier stage is basically a differential amplifier with active loads . The Pre amp stage (or stages) amplifies the input signal to improve the comparator sensitivity (i.e., increases the minimum input signal with which the comparator can make a decision) and isolates the input of the comparator from switching noise (often called kickback noise) coming from the positive feedback stage . It also can reduce input referred latch offset voltage. The sizes of Ml and M2 are set by considering the diff-amp transconductance and the capacitance of input. The transconductance sets the gain of the stage, while the size of Mland M2 determines the input capacitance of the comparator. Here gm1= gm2. The positive feedback latch stage is used to determine which of the input signals is larger and extremely amplifies their difference . It takes positive feedback from the cross gate connection of M8 and M9. Consider i+ >> i- so that M7 and M9 are ON and M8 and transistor M10 are OFF. Here also βa= β7=β10 and βb= β8=β9 for which vo- is ~ 0V and v0+ is If we start to increase i- and decrease i+, when drain to source voltage of transistor M9 is equivalent to the threshold voltage, Vth of M8, switching occurs. At this time M8 takes current away

from transistor M7 which decreases drain to source voltage of M7 and M9 turns off. If we assume that maximum value of v+ or v- is equal to 2Vth, then under these circumstances M8 and M9 operate under cut-off or triode region under steady state conditions . Then voltage across M9 becomes Vth and M9 enters into saturation and current of M9 is This is the point at which switching takes place; i.e. M9 shuts off and M8 turns on. If βa= βb , then switching takes place when the currents, i+ and i-, are equal. A similar analysis of increasing i+ and decreasing i- results in , the final component (output buffer) of our comparator, converts the output of the latch stage into a full scale digital level output (logic 0 or logic

B. Double-Tail Latch Type Comparator:

The figure shows \the schematic of the Double-Tail Latch type Voltage SA. Double-Tail derived from the fact that the comparator uses one tail for input stage and another for latching stage. It has less stacking and can therefore workwhen supply voltages are lower. Large size of the Transistor M14 enables large current at latching stage which is independent of common mode voltages at inputs and small size of M1 offers lower supply voltages resulting lower offset.

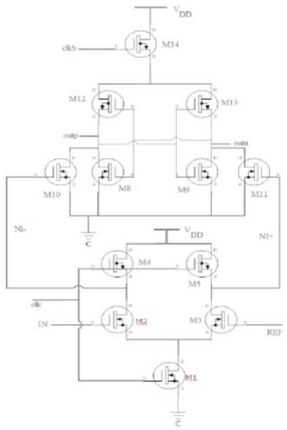

Figure 3.2 Double-Tail Latch Type Comparator:

Operation: During rest phase (clk=0V), M4 and M5 charges to VDD which in turn charges Ni nodes to VDD. Hence M10 and M11 turns on and discharges output nodes to GND. During evaluation phase (clk=VDD), the tail current transistors M1 and M14 turns ON. On Ni nodes common mode voltage decreases and one input dependent differential mode voltage generates. M10 and M11 pass this differential mode voltage to latch stage. The inverters start to regenerate the voltage difference as soon as the common-mode voltage at the Dinodes is no longer high enough for M10 and M11 to clamp the outputs to ground. M10 and M11 also provide additional shielding between the input and output which in turn reduces kickback noise.

D. Dynamic Comparator

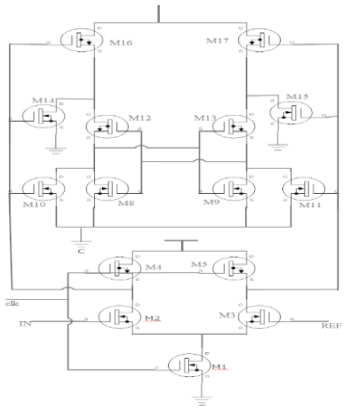

Figure3.3 Dynamic Comparator

Operation: The figure shows the Self-Calibrating Dynamic Comparator. This comparator resolved the above said problem by replacing clkb signal with Ni nodes. But it results in increased delay since transistor M16/M17 use Ni node voltages as their input signal which shows a slow exponential decay shape and hence the current drivability of the output node decreases. The input referred latch offset is also reduced in this circuit due to the fact that output latch stage takes load from the M10/M11 and M16/M17. Maximum drive current of the output node also decreased to half since the supply voltage VDD has been divided into two transistors.

D. Double-Tail Dual-Rail Dynamic Latched Comparator

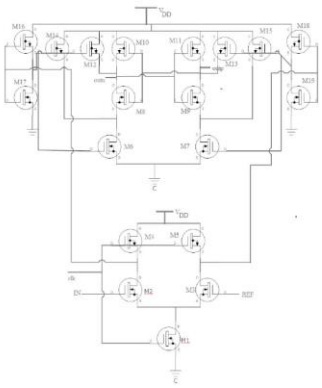

Figure 3.4 Double-Tail Dual-Rail Dynamic Latched Comparator

Operations: The figure shows the schematic of the Double-Tail Dual-Rail Dynamic Comparator .This comparator eliminated the weakened Ni nodes by inserting an inverter between input and output stages. Due to inverter, weak signal of Ni node is regenerated and fed to the output stage. This comparator shows faster operation and lesser power dissipation than the previous comparators.

III. COMPARATIVE ANALYSIS

Number of Transistor Used In Circuit

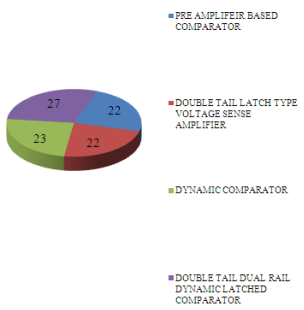

Figure 4.1 Number of Transistor Used In Circuit

Dynamic Power Dissipation

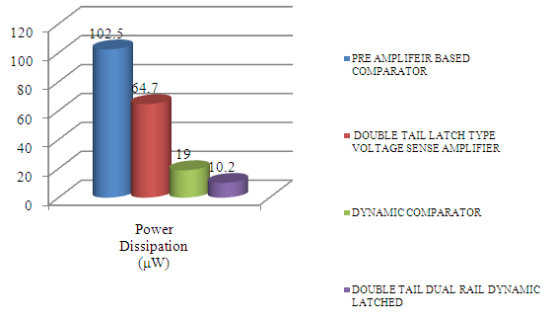

Figure 4.2 Dynamic Power Dissipation

Delay *(ps)*

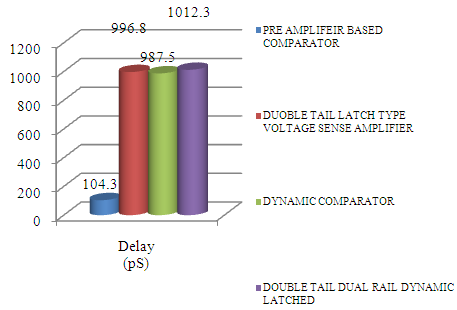

Figure 4.3 Delay *(ps)*

Speed

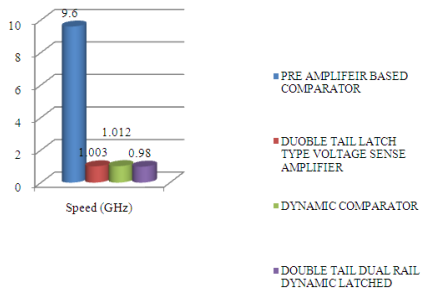

Figure 4.4 Speed

Input Offset Voltage (mV)

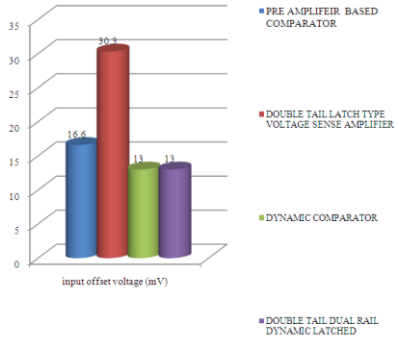

Figure 4.5 Input Offset Voltage (mV)

TABLE I - SUMMARY RESULT

Topology	Parameter of comparator				
	No. of transistor	Power dissipation (µW)	Delay (ps)	Speed (GHz)	Input offset Voltage (mV)
Pre amplifier based comparator	20	102.5	104.3	9.6	16.6
Double Tail Latch Type Voltage Sense Amplifier	22	64.7	996.8	1.003	30.3
Dynamic comparator	23	19	987.5	1.012	13
Double tail dual rail comparator	27	10.2	1012.3	.98	13

IV. CONCLUSION

This paper explains operation of different comparators and its design. It help designer to analyses. It give brief information of different characteristics of comparator and comparative analysis of comparator on the basis of this parameter which will be simulated in HSPICE .The proposed comparator will be low power comparator as compare to all comparator mentioned here.

REFERENCES

[1] Phillip E. Allen,Dougles R. Holberg "CMOS Analog Circuit Design" second edition OXFORD UNIVERSITY PRESS
[2] B. Razavi, "Principle of data conversion system design" IEEE PRESS
[3] Aalay Kapadia, Prof. Vijay Savani "Analysis And Characterization of Different Comparator Topologies", International Journal of Scientific & Technology Research Volume 1, issue 11, December 2012
[4] Pedro M.Figueiredo, Joao C.Vital, "Kickback Noise Reduction Techniques for CMOS Latched Comparator", IEEE Transactions on Circuits and Systems, vol.53, no.7, pp.541-545, July 2006.
[5] B. Murmann et al., "Impact of scaling on analog performance and associated modeling needs," IEEE Trans. Electron Devices, vol. 53, no. 9, pp. 2160-2167, Sep. 2006.
[6] Jun He, Sanyi Zhan, Degang Chen, and R.L. Geiger, "Analyses of Static and Dynamic Random Offset Voltages in Dynamic Comparators," IEEE Trans. Circuits Syst. I: Reg. Papers, vol. 56, pp. 911-919, May 2009.
[7] M. Miyahara, Y. Asada, P. Daehwa and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," in Proc. A-SSCC, pp. 269-272, Nov. 2008.
[8] Johns D., Martin K., Analog Integrated Circuit Design, Wiley India Pvt. Ltd., 2008
[9] Cadence Online Documentation. Avilable: http://www.cadence.com
[10] Amin Nikoozadeh, Student Member, IEEE, and Boris Murmann, Member, IEEE" An Analysis of Latch Comparator Offset Due to Load Capacitor

Mismatch" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 53, NO. 12, DECEMBER 20

[11] Apisak Worapishet "Speed and Accuracy Enhancement Techniques for High-PerformanceSwitched-Current Comparators" IEEE Journal of Solid-State Circuits, Vol. 36, No. 4,

[12] Randall White"Analysis of Errors in a Comparator-Based Switched-Capacitor Biquad Filter" IEEE Transactions on Circuits and Systems—Ii: Express Briefs, Vol. 56, No. 9, September 2009

[13] Bernhard Goll "A Comparator with Reduced Delay Time in 65-nm CMOS for Supply Voltages Down to 0.65 V" IEEE transactions on circuits and systems—ii: express briefs, vol. 56, no. 11, november 2009

[14] Jaeha Kim, Member, IEEE, Brian S. Leibowitz, Member, IEEE, Jihong Ren, Member, IEEE, and

[15] Chris J. Madden, Member, IEE E " Simulation and Analysis of Random Decision Errors in Clocked Comparators" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 56, NO. 8, AUGUST 2009

[16] Todd Sepke, Member, IEEE, Peter Holloway, Charles G. Sodini, Fellow, IEEE, and Hae-Seung Lee, Fellow, IEEE "Noise Analysis for Comparator-Based Circuits" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 56, NO. 3, MARCH 2009

[17] John K. Fiorenza, Student Member, IEEE, Todd Sepke, Student Member, IEEE, Peter Holloway,

[18] Charles G. Sodini, Fellow, IEEE, and Hae-Seung Lee, Fellow, IEEE "Comparator-Based Switched-Capacitor Circuits for Scaled CMOS Technologies" IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 41, NO. 12, DECEMBER 2006

[19] Samaneh Babayan-Mashhadi, Student Member, IEEE, and Reza Lotfi, Member, IEEE" Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator" IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 22, NO. 2, FEBRUARY 2014

[20] Bernhard Goll, Member, IEEE, and Horst Zimmermann, Senior Member, IEEE" A Comparator With Reduced Delay Time in 65-nm CMOS for Supply Voltages Down to 0.65 V" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 56, NO. 11, NOVEMBER 2009

[21] Monica Rose Joy, 2Thangamani M. " Design and Analysis of Low Power Comparator Using Switching Transistors " IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 4, Issue 2, Ver. III (Mar-Apr. 2014)