Study and Implementation of Phase Frequency Detector and Frequency Divider 45nm using CMOS Technology

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*Abstract--*This work describes the designs for Phase Frequency Detector (PFD) and Frequency divider (FD) respectively using 45nm CMOS Technology. The paper presents detailed introduction to PFD and FD networks and also provides the corresponding simulation results. PFD measure the Difference in phase and frequency between the reference and feedback signal. FD divide the clock signal, The working platform is LTSpice. The power supply to the active elements is 1 volt. The design can be used in High Speed and Low Power consumption applications.

Keywords: CMOS, PFD (Phase Frequency Detector), Frequency Divider

I. INTRODUCTION

In high speed communication systems, to make sure clock recover and synchronization by PLL is a most important factor of the systems, while in digital signal processing circuit, frequency synthesizer consisting of digital.

Phase-locked loop has become a key part which is used for system clock inside chips. Phase locked loops (PLLs) are widely used in microprocessors and digital systems for clock generation and as a frequency synthesizers in communication systems for clock extraction and generation of a low phase noise local oscillator. A phase-locked loop is a feedback control circuit. As the name suggests, the phase locked loop operates by trying to lock to the phase of an input signal through the use of a negative feedback path. A basic form of a PLL consists of three fundamental blocks, as shown in figure 1.[1]

The phase detector compares the phase of a periodic input signal against the phase of the VCO. Output of the PD is a measure of the phase difference between its two inputs. The difference voltage is then filtered by the loop filter and applied to the VCO.
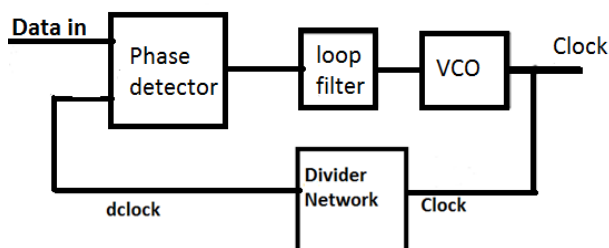

Figure 1. Block Diagram of DPLL[1]

- Phase frequency detector (PFD)
- Loop filter
- Voltage controlled oscillator (VCO)
- Divider network

The control voltage on the VCO changes the frequency in a direction that reduces the phase difference between the input signal and the local oscillator.

When the loop is locked, the control voltage is such that the frequency of the VCO is exactly equal to the average Frequency of the input signal. As long as the initial difference between the input signal and the VCO is not too big, the PLL eventually locks on to the input signal . This period of frequency acquisition, is referred as pull-in time, this can be very long or very short, depending on the bandwidth of the PLL. The bandwidth of a PLL depends on the characteristics of the phase detector, voltage controlled oscillator and on the loop filter.

II. PHASE FREQUENCY DETECTOR

The phase frequency detector, measures the difference in phase between the reference and feedback signals. If there is a phase difference between the two signals, it generates up or down synchronized signals to the charge pump/ low pass filter. To take care of these disadvantages, we implemented the Phase Frequency Detector, which can detect a difference in phase and frequency between the reference and feedback signals. Also, unlike the XOR gate PD, it responds to only rising edges of the two inputs and it is free from false locking to harmonics.

The PFD design uses two flip flops with reset features. The inputs to the two clocks are the reference and feedback signals. The D inputs are connected to VDD always remaining high. The outputs are either UP or DOWN pulses. These outputs are both connected to an AND gate to the reset of the D-FF's. When both UP and DOWN are high, the output.

The control voltage for tri-state output logic, VPDtri , is given by Through the AND gate is high, which resets the flip flops. Thus both signals cannot be high at the same time. This means that the output of the PFD is either an up or down pulse but not both. The difference in phase is

measured by whichever rising edge occurs first. As shown in figure 2 the implementation of Phase Frequency Detector in 45nm CMOS technology which is used in PLL to lock the phase and frequency of the feedback signals with reference clock signal .The phase difference between the dclock and data is given by.

$$\Delta\varphi = \varphi\, data - \varphi\, dclock = (\Delta t / Tdclock)*2\pi \text{ (radians)}$$
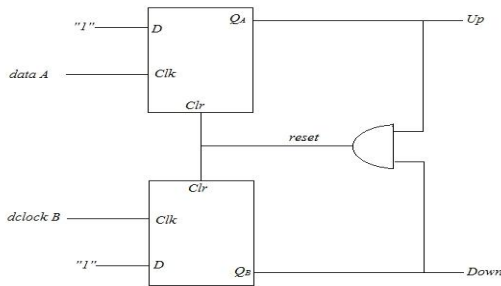
Now, The relation With PFD, Configure fig.[1]
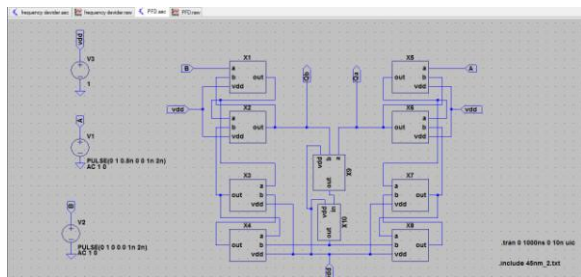
Figure 2. Basic Phase Frequency Detector[6]

The control voltage for tri-state output logic, VPDtri , is given by

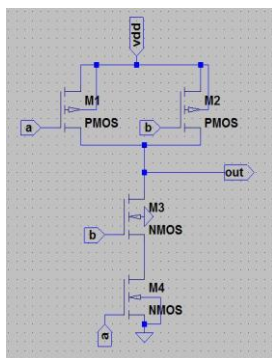$$VPDtri = VDD - 0/ 2\pi - (-2\pi) * \cdot \Delta\varphi$$

$$VPDtri = \overline{VDD} / 4\pi * \cdot \Delta\varphi$$

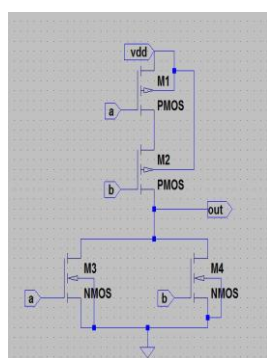Where the gain of the PFD with tri-state output logic is given by.

$$KPDtri = \overline{VDD} / 4\pi \text{ (volts / radian)}$$

(a)

(b)

(c)

Figure 3. (a)Design Phase Frequency Detector
(b)NANDgate (c) NOR gate

Above This Figure for Design of Phase Frequency Detector (PFD) contains Eight NOR gate (X1,...,X8), NAND gate (X9) and NOT gate (X10).

III. LOOP FILTER

The function of the loop filter is to convert the output signal of phase frequency detector to control voltage and also to filter out any high frequency noise introduced by the PFD. The loop filter used with this type of PFD is a simple RC low-pass filter. Since the output of the PFD is oscillating, the output of the loop filter will show a ripple as well, even when the loop is locked. This modulates the clock frequency, an unwanted characteristic of a DPLL using PFD. A ripple on the output of the loop filter with a frequency equal to the clock frequency will modulate the control voltage of the VCO.

IV. VOLTAGE CONTROL OSCILLATOR (VCO)

A PLL system is composed of a phase detector, low pass filter and a voltage-controlled oscillator. The Voltage-Controlled Oscillator (VCO) is the most crucial element in a Phase-Locked Loop (PLL) circuit. A Voltage-Controlled Oscillator (VCO) is an oscillator, where the control voltage controls the oscillator output frequency. Today's wireless communication systems high frequency Voltage-Controlled Oscillators (VCOs) are required. Applications of VCOs range from clock generation in microprocessors to carrier synthesis in cellular telephones, requiring vastly different oscillator topologies and performance parameters. A VCO is a Voltage Controlled Oscillator, whose output frequency is, ideally, a linear function of its control voltage, which is generated by the phase detector.

Consider the typical characteristics of voltage controlled oscillator shown in figure 3 The frequency of the square wave output of the voltage controlled oscillator is fcenter when Vin (= Vcenter) is VDD/2 (typically). The other two frequencies of interest are the minimum and maximum oscillator frequencies. fmin and fmax possible, with input voltage Vmin and Vmax, respectively.

If frequencies are not equal, the control voltage will oscillate, causing the clock to move, in time, around some other point than centre of the data.
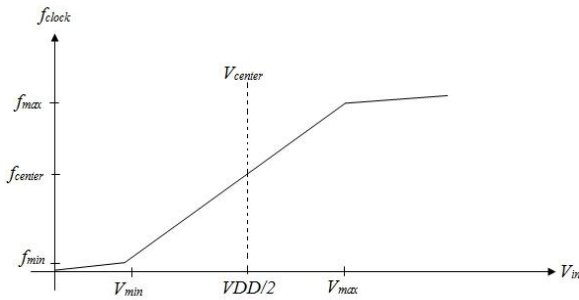
Figure 4. Output frequency of VCO versus Input Control voltage

This minimizes the time it takes the DPLL to lock. It is important that the Voltage Controlled Oscillator duty cycle be 50 percent. If this is not the case, the DPLL will have problems locking.
The gain of the VCO is simply the slope of the curve given in figure-4
This gain can be written as
K VCO = 2 π (f max – f min/ V max – V min) (radians/ S.V)

V. DIVIDER NETWORK

The divider network is feedback given to the phase frequency detector. Here we used divide by 2 network, we can vary the divider network for synthesis of different frequencies. It divide the clock signal of VCO and generate dclock , than applied to phase frequency detector which compare it with input data.
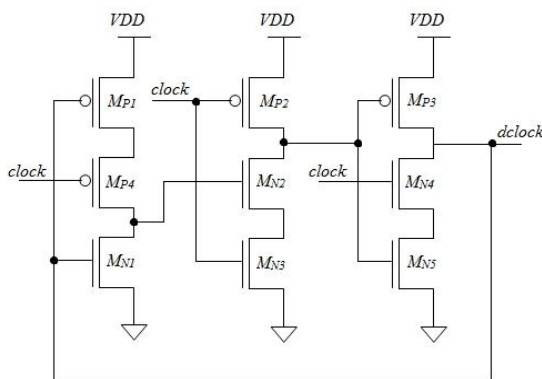

Figure 5. Divider Network by Two Circuit

The circuit consists of three parts. The first part is a gated inverter that consists of M_{P1}, M_{P4} and M_{N1}, which passes the divider output to the following stage when clock goes low. The second part is a latch stage that consists of M_{P2}, M_{P3}, M_{N2}, M_{N3}, M_{N4} and M_{N5}. This circuit will be activated and store the output of the gated inverter when clock is high

VI. CALCULATION OF ASPECT RATIO

The drain current of a short channel MOSFET
$$I_D = W \cdot v_{sat} \cdot C'_{ox} \cdot (V_{GS} - V_{THN} - V_{DS,sat})$$
From this equation we can write the equation for the width of NMOS, which is given by:

$$Wn = \frac{I_D}{[Vsat \cdot Cox \cdot (Vgs - Vthn - Vds, sat)]}$$

By putting the values of these parameters in the equation of Wn, we get the value Wn in 45nm technology, which is given by:

$$Wn = 180nm$$
For the Ratio of W/L,

$$(W/L) p = 2.5(W/L) n$$
Now, we know that the values of L for NMOS and PMOS are same in 45 nm technology, so we get

$$Lp = Ln = 45nm$$

Table 1[6]
MOSFET model parameters for 45nm CMOS Technology

Short-Channel MOSFET parameters VDD=1V and a scale factor of 45 nm		
Parameter	NMOS	PMOS
Bias Current, ID	10μA	10μA
VDS,sat and VSD,sat	50 mV	50 mV
VGS and VSG	350 mV	350 mV
VTHN and VTHP	280 mV	280 mV
vsatn and vsatp	110×103 m/s	90×103 m/s
Tox	14Å	14Å
C'ox	25 f F/μm2	25 f F/μm2

VII. SIMULATION RESULTS

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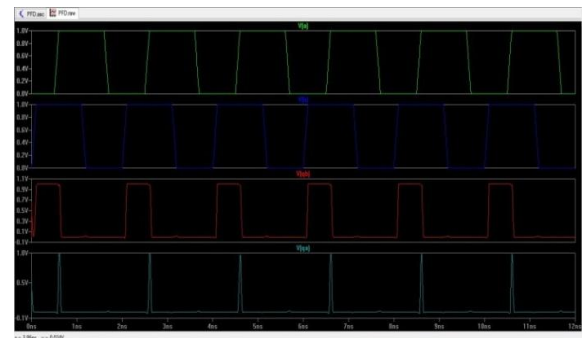
A. Simulation Result of PFD

Figure 6. Simulation Result of Propsed PFD with Delay

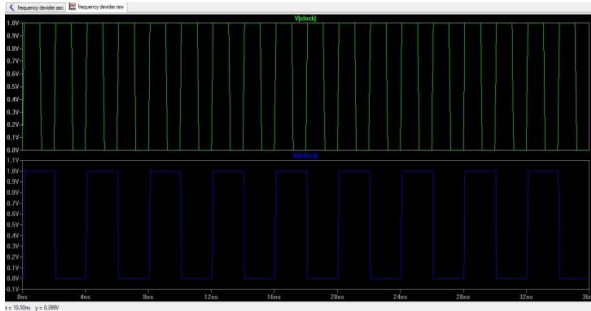*B.   Simulation Result of Frequency Divider by two*

Figure 7. Frequency Divide by Two

VIII.   CONCLUSION

The paper present simulation and implementation of PFD and Frequency Divider Network using 45nm CMOS Technology in LT-spice software with low power supply.

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