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Study and Analysis of Level Converters under Various Load Condition

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Abstract

The use of multiple supply voltage systems, which employs level converter between two voltage islands, is one of the most effective ways to reduce power consumption. The design of an efficient level converter with a little power and delay overheads is one of the major design challenge. In this paper, analysis of different level converters for Dual-Supply Systems under various load condition using Mentor Graphics Design Architect at tsmc 0.18 µm process technology has been done. The simulation results shows that Keeper Pass Gate Level Converter exhibits up to 60% delay reduction and saves power up to 50% as compared to Standard DCVS Level Converter.

Index Terms— Low Power, Voltage Island, Level Converters, Multiple Supply Systems.

1. Introduction

Today, as we are aware with the fact that life is next to impossible without mobile phones, PCs and many more electronic gadgets which we use everyday. The whole world has become dependent on technology. This has imposed the requirement of portable, economical and minimum power consuming devices. The gadgets that we were using earlier were more bulky, expensive and consume much more power then that we are using today. This is because earlier the circuits that we were using is made up of discrete components which occupies very large area but now it is possible to design large complex circuits in a small chip area. All this is possible only because of advancement in Very Large Scale Integration (VLSI) Technology. However, this requirement for portability has put number of restrictions on the size, weight, and battery life of such devices. Hence, power dissipation is one of the fundamental design concerns that current day VLSI design engineers have to cope with while dealing with integrated circuit designs. Power minimization is not only essential for portable devices but also necessary for improving reliability of high-end microprocessors and data processing. Significant research progress has been made during recent years to reduce the power dissipation of an integrated circuit.

Due to quadratic relations between voltage and power consumption, reducing the supply voltage is very efficient in decreasing power consumption. However, it is at the expense of the circuit delay. In order to lower the supply voltage without system performance degradation, Clustered Voltage Scaling (CVS) has been developed in which critical and non-critical paths of the circuit are clustered [1]. In the CVS Scheme, by using low voltage (V_{DDL}) in the non-critical paths and using high supply voltage (V_{DDH}) in speed sensitive paths, the whole system power consumption could be reduced without degrading the performance. Whenever an output from a low V_{DD} cluster has to drive an input to a high V_{DD} cluster, Level Conversion is required at the interface. The reason is that the output from a low swing voltage (V_{DDL}) block cannot connect to a PMOS in a high swing voltage (V_{DDH}) block directly, since the PMOS cannot shut off with low voltage V_{DDL}. One of the main challenges in the CVS Scheme is to design Level Converters (LCs) with less power and delay overhead to interface low voltage (V_{DDL}) blocks with high voltage (V_{DDH}) blocks [2].

In this paper, three different level converters based on a multi voltage CMOS technology are presented. Unlike the standard DCVS level converter techniques based on cross-coupled mechanism, the Pass Gate level converters eliminate the contention at the points of connection of the cross-coupled pair and the pull-down NMOS network. The effectiveness of the Pass Gate Level Converter circuits for reducing power consumption and propagation delay is evaluated at scaled supply voltages.

This paper is organized as follows: Section II discusses the understanding of Basic Principles regarding the power consumption and delay of the circuits and section III refers to State-of-the-art. In section IV, we analyzed and implemented different

level Converters. Section V shows the simulation results and Section VI concludes the paper.

2. BASIC PRINCIPLES

Before making any attempt to reduce the power consumption, one must understand various sources of power dissipations in any VLSI circuit.

There are 3 major sources of power dissipation in a CMOS circuit [3]:

$$\mathbf{P = P_{Switching} + P_{Short\text{-}Circuit} + P_{Leakage}} \quad (1)$$

Where, $P_{Switching}$, called switching power, is due to charging and discharging of capacitors driven by the circuit, $P_{Short\text{-}Circuit}$ called short-circuit power, is caused by the short circuit currents that arise when pair of PMOS/NMOS transistors conducts simultaneously, and $P_{Leakage}$, called leakage power, originates from substrate injection and sub threshold conduction. Design for low-power implies the ability to reduce all three components of power consumption in CMOS circuits during the development of a low power electronic product. However, most of the power consumption of the circuits depends on the dynamic factors i.e. switching power. Switching power for a CMOS gate working in a synchronous environment is modeled by the equation (2) [2]:

$$\mathbf{P_{Switching} = C_L V_{DD}^2 f_{Clock} ESW} \quad (2)$$

Where, $\mathbf{C_L}$ is the output load of the gate, $\mathbf{V_{DD}}$ is the supply voltage, $\mathbf{f_{Clock}}$ is the clock frequency and, **ESW** is the switching activity of the gate, defined as the probability of the gate's output to make a logic transition during one clock cycle. Reductions of $P_{Switching}$ are achievable by combining minimization of the parameters in the eq. (2).

Historically, supply voltage scaling has been the most adopted approach to power optimization, since it normally yields considerable power savings thanks to the quadratic dependence of $P_{Switching}$ on V_{DD}. The major short-coming of this solution, however, is that lowering the supply voltage affects circuit speed. As circuit latency is given by the relation [4]:

$$\textbf{Propagation Delay, } \mathbf{Tpd} = \frac{\mathbf{C_{charge}\, V_{DD}}}{\mathbf{k*(V_{DD}-V_{th})^2}} \quad (3)$$

Where, C_{charge} is Capacitance of the circuit that needs to be charged or discharged in a single clock cycle, V_{th} is the threshold value of the MOS transistor used, k is a constant, depends on the physical parameters of the transistors used.

Thus, reducing supply voltage, V_{DD} results in increasing the latency of the circuit which affects circuit speed and hence, performance badly. As a consequence, both design and technological solutions must be applied in order to compensate the decrease in circuit performance introduced by reduced voltage. In other words, speed optimization is applied first, followed by supply voltage scaling, which brings the design back to its original timing, but with a lower power requirement.

3. RELATED RESEARCH WORK

A. Research in Multi Voltage Systems

As discussed in Section I, the most commonly used efficient method for power reduction, is by using a multi-voltage supply system which make use of level converters. The idea behind this technique is to use multiple supply voltages for a single chip by dividing the integrated circuit into regions, called voltage islands, operating at different voltages. The circuits which are on the critical path are supplied higher voltage level (V_{DDH}) and the circuits which are off the critical path are made to run at a lower voltage level (V_{DDL}) [10]. For designing such systems algorithms like clustered voltage scaling (CVS) and Extended Clustered Voltage Scaling (ECVS) are widely used. Authors in [8], [9], [10] discuss in details about multi voltage supply systems and various algorithms followed for assignment of V_{DD} to cells. These algorithms mainly decide where and what type of level converters should be used in the circuit. In [10], the authors have studied the CVS structure in detail and proposed a novel architecture called the extended CVS (ECVS) and they have also proposed a synthesis technique of the structure. This architecture allows inserting a level converter where ever there is a large slack (the difference between the required time and the arrival time of the signal at the gate) between the gates. The authors have proposed an in-house tool called power slimmer [9] which controls the level converter insertion by synthesizing the ECVS structure from a gate-level mapped netlist. ECVS scheme allows asynchronous level conversion which allows inserting a level converter anywhere in the circuit. In [9], the authors proposed a technique where in it reduces the number of interface level converters leading to a clustered voltage scaling. In [7], authors describe gate level power minimization using dual

supply voltages. The concept that the authors have proposed is that all the gates and flip flops which are off the critical path are made to run at a reduced supply voltage to save power. This is done by performing static timing analysis for a given circuits with a single V_{DD} and extracting the gates which are not on the critical path and assigning V_{DDL} to them.

B. Research in Level Converters

A lot of level converters has been designed and developed by researchers from time to time. Here we tried to brief all the research done on Level Converters. In [6], key properties and design metrics of a level converter for dual-V_{DD} systems are examined. The authors have studied the traditional level converter circuits like cross coupled level converter (CCLC), single supply diode voltage limited buffer level converter (SSLC), pass transistor half latch (PHL) and pre-charged circuit. In [7], [13], [14] the authors have studied a conventional level converter circuit known as differential cascode voltage switch (DCVS). The DCVS circuit is a small circuit which consists of a PMOS pair connected back to back which act as a differential pair. Each of the above referenced papers proposes new level converter designs considering DCVS as a baseline design.

In [14], authors propose a new level converter circuit based on the keeper transistor concept in pass transistor logic. The keeper transistor is used as a level restorer in the pass transistor logic. Then the authors have compared the performance of the proposed circuit and the traditional DCVS by calculating the delay, power and energy-delay product. In [11], a new level converting circuit called symmetrical dual cascode switch (SDCVS) is proposed. The authors have addressed to the contention problem of DCVS and provided a solution for the same in this paper. The authors state that the contention problem will give rise to increased delay time and power consumption. Two additional NMOS are added to the DCVS design to eliminate the contention problem. In [12], novel high-speed and low-power bootstrapped level converter is proposed. This proposed level converter uses a voltage bootstrapping to increase current driving capability and to reduce contention problem. Simulation results in a 0.13-µm CMOS process indicated that the proposed level converter reduces the propagation delay up to 64% and the power-delay product up to 49% as compared to conventional level converters.

4. IMPLEMENTATION OF LEVEL CONVERTERS

In this section, we analyzed and implemented two important topologies of level converter: (1) Differential Cascode Voltage Switched (DCVS) topology, (2) Pass Gate LC topology. To have better understanding of the Design, Circuits are verified under different load Capacitance in terms of power consumption and circuit delay.

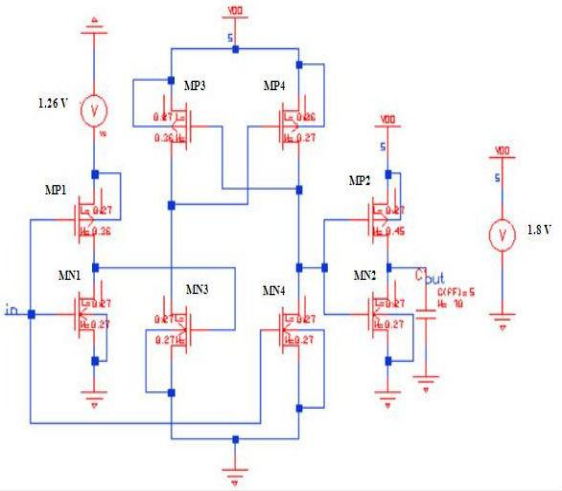


Fig 1: Schematic of Standard DCVS Level Converter

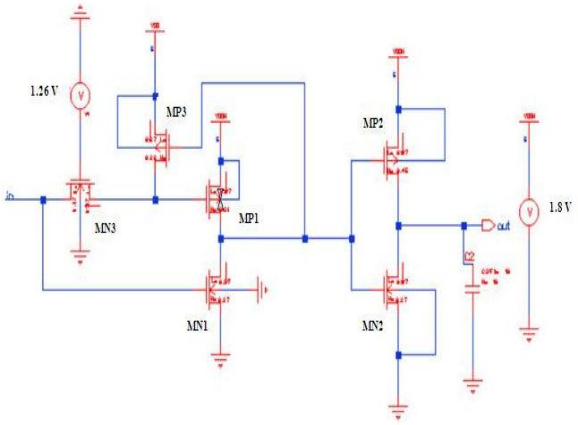


Fig 2: Schematic of Standard Pass Gate Level Converter

Figure 1 shows the first of the designed Level Converter, DCVS logic circuit. In this level Shifting Scheme, low voltage swing logic (V_{DDL}) and its inverted version is applied to NMOS transistors MN4 and MN3, respectively and is up-converted to V_{DDH} through the cross coupled PMOS pair formed by

transistors MP3 and MP4. Transistor sizing is done in such a way to achieve the optimum results. This circuit consumes significant power due to contention at the points of connection of the cross coupled pair and the pull down NMOS network formed by MN3 and MN4 [5].

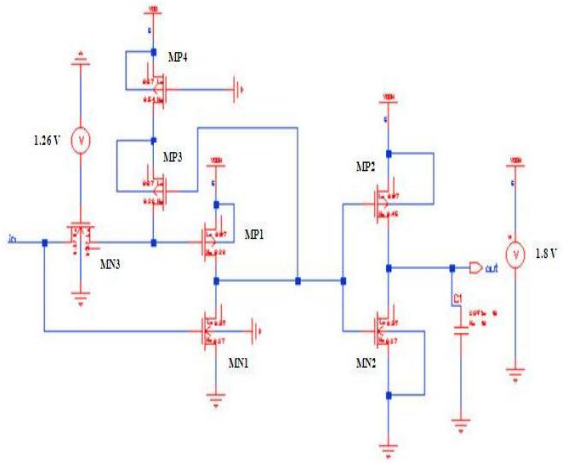
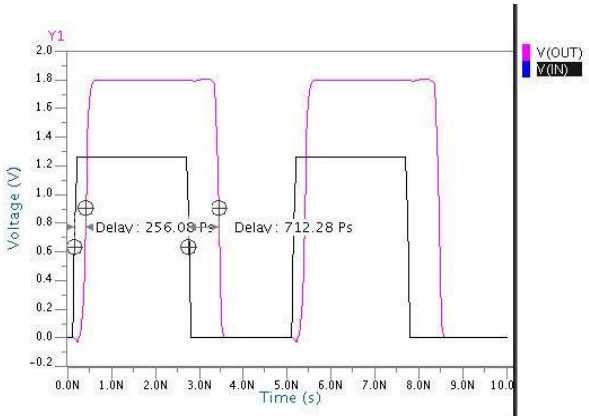


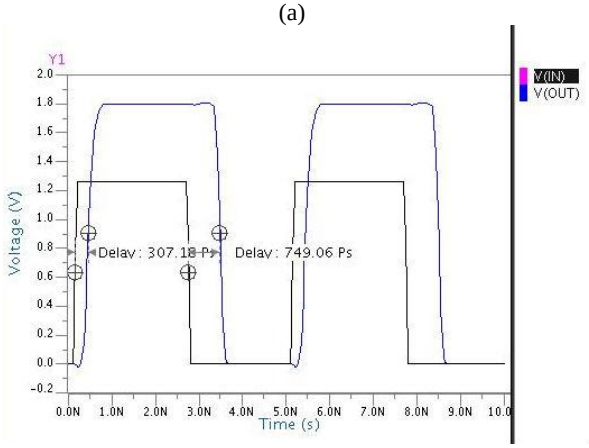
Fig 3: Schematic of Keeper Pass Gate Level Converter

Thus, in attempt to compensate the overhead caused by DCVS LC, another level converter is designed called Pass Gate Level Converter. Figure 2 illustrates the schematic design of Standard Pass Gate LC. As seen from the schematic, number of transistors used in Standard Pass Gate LC reduces to six over eight in standard DCVS structure. This level converter is based on a weak feedback pull-up device (MP3) and an NMOS pass gate (MN3). The purpose of the pass gate device is to isolate the input of the PMOS MP1 from the previous logic stage [5]. The feedback device MP3 can then pull-up the internal node without consequence to the prior logic that is running at V_{DDL}. The low swing input at node 'in' is applied to the pass transistor MN3, which results in $V_{DDL}- V_{thMN3}$ swing at intermediate node. However, due to feedback PMOS MP3 this intermediate node swings to high value V_{DDH}. Thus, level conversion takes place by transistors MP1 and MN1 resulting in high voltage swing at 'out' node. This level converter consumes less energy than the Standard DCVS level converter due to its fewer devices and reduced contention.

To further attain power and delay improvement, Keeper Pass Gate LC has been designed which is just the improvement in Standard Pass Gate LC. The Schematic design of Keeper Pass Gate LC is shown in figure 3. Here, the feedback transistor MP3 from figure 2 is split into two transistors MP3 and MP4. This is known as high-performance dynamic design technique [5]. The advantage of this change is to reduce the capacitive load i.e. gate capacitance of the Keeper device, MP3 on the immediate node after the transistors MN1 and MP1 which are responsible for level conversion. Thus, reducing the load on transistors MN1 and MP1 by the keeper result in significant reduction in power consumption.



(a)



(b)

Fig 4: Simulation Results of Standard DCVS Level Converter at Load Capacitance of: **(a)** 5 fF, **(b)** 10 fF

5. Comparative Simulation Results and Discussion

The simulation results were obtained from Mentor Graphics ELDO simulator in tsmc 0.18 µm CMOS technology. We studied the performance of these circuits with the value of V_{DDH} set to 1.8 V and V_{DDL} = V_{DDH} x 70% = 1.26 V (the optimum V_{DDL} to V_{DDH} ratio is 60% to 70% to yield the best power consumption [6]). In order to observe the circuit

performance under different load condition, the circuits are simulated at load capacitance of 5 fF and 10 fF.

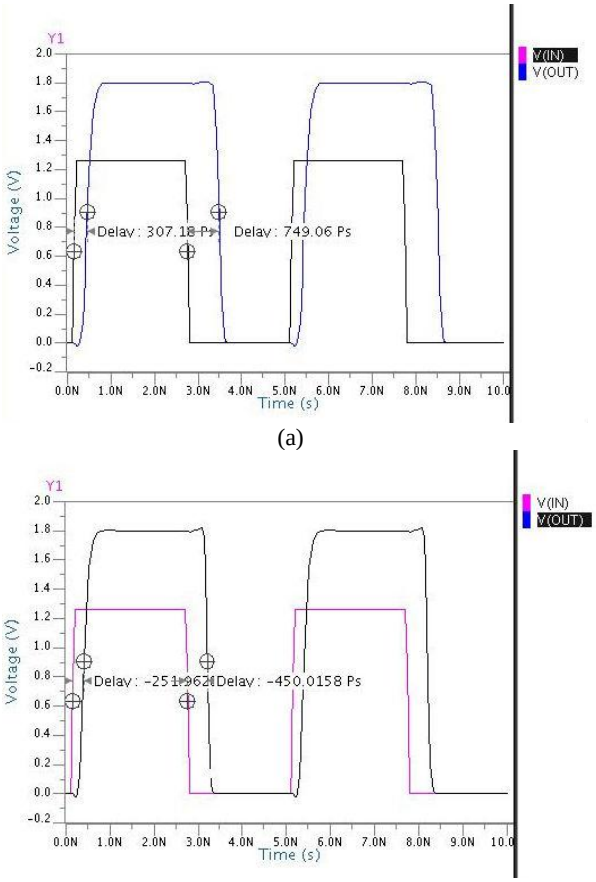


Fig 5: Simulation Results of Standard Pass Gate LC at Load Capacitance of : **(a)** 5fF, **(b)** 10fF

Standard DCVS LC suffers from the contention problem, therefore simulation results shows maximum power and delay overhead. On the other hand, Pass Gate Level Converters uses few transistors in its operation as compared to DCVS Level Converter which results in significant reduction in delay and power. Hence, Keeper Pass Gate LC shows improvement of about 50% in power consumption as compared to Standard DCVS level Converter.

Figure 4, figure 5, and figure 6 shows simulation waveform of the LCs. From the simulation results, it is proved that the delay and the power consumption in Pass Gate type Level Converters is very less as compared to that in the Standard DCVS Level Converter. It is also observed that falling delay in case of Keeper Pass Gate LC is much less in comparison to Standard Pass Gate due to the introduction of Keeper PMOS which helps in reducing the load Capacitance. Thus, there is reduction of about 18%-20% in rising delay and around 60% in falling delay in Keeper Pass Gate LC as compared to Standard DCVS LC. It is important to note that with the introduction of keeper transistor in standard Pass Gate topology the falling delay reduces to 40% while the rising delay remains almost constant. This is because during High-to-Low transition, resistive path of pull down network (which remains same) and, load and parasitic capacitance of pull up network (reduces due to keeper transistor) is responsible for overall falling delay, whereas during Low-to-High transition, resistive network (remains same) of pull up and, load and parasitic Capacitance of pull down network (remains same) is responsible for overall rising delay.

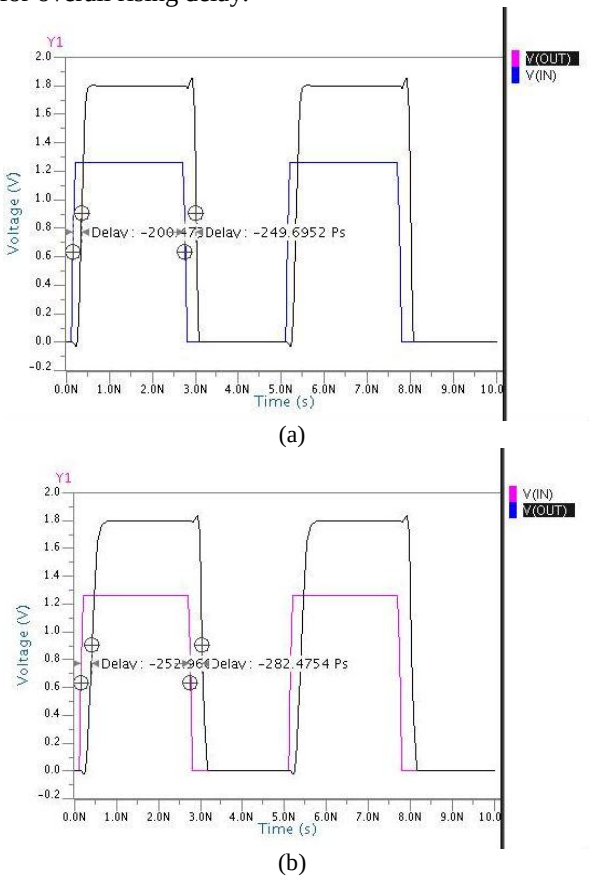


Fig. 6. Simulation Results of Keeper Pass Gate LC at Load Capacitance of : (a) 5fF, (b) 10 fF

Thus among the analyzed Level Converters, Pass Gate LC topology with the introduction of keeper is best in terms of power as well as delay. Comparison of delay and power consumption of various Level Converters is shown in table I.

Table 1: Comparison of delay and power dissipation of various Level Converters

Level Converters	Load Capacitance, CL= 5 fF			Load Capacitance, CL = 10 fF		
	Delay (ps)		Dynamic Power Dissipation (µw)	Delay (ps)		Dynamic Power Dissipation (µw)
	Rising	Falling		Rising	Falling	
DCVS	256.08	712.28	23.853	307.18	749.06	27.060
Standard Pass Gate	199.28	457.64	16.924	251.96	450.02	19.098
Keeper Pass Gate	200.47	249.69	11.256	252.96	282.47	14.568

6. CONCLUSION

In this paper, we investigated two different level converter topologies for use in SoCs that rely on dual supply voltage. The power analysis results prove that Keeper pass gate LC is about 50% power efficient as compared to standard DCVS LC. Also, there is reduction of about 18%-20% in rising delay and around 60% in falling delay in Keeper Pass Gate LC as compared to DCVS LC. Thus we can conclude that among the analyzed Level Converters, Pass Gate Level Converter topology with the introduction of keeper transistor is best in terms of power as well as delay. The tool used for simulation is Mentor Graphics ELDO at 0.18 µm technology and the practical observations has been tabled.

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