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Study and Analysis of 15 Level MLI using 12 Power Mosfet Switches

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***Abstract*— A new single-phase 15-level inverter with twelve MOSFET switches and a reduced number of components for various applications is proposed for this topic. There are different types of multilevel inverters. Among these Cascaded multilevel inverters have a great range of advantages in the power industry since their main motive is to have reduced size components. As the number of levels increases the harmonic content of the output voltage waveform decreases, the proposed inverter aids to generate fifteen stepped output voltage levels with lower THD. The proposed inverter can improve productivity and reduce losses, cost, and difficulty in system construction. The proposed inverter is tested experimentally using the Arduino controller along with MATLAB/Simulink. The experiment presents results not only to show its efficiency but also the effectiveness under different conditions of linear and non-linear loads. The inverter is well balanced during the non-linear loads. Mainly, the losses that occurred due to switching can be eliminated by using the minimal number of power switches.)**

Keywords—THD,MLI,PMW,CHB

1.

I. INTRODUCTION

The number of power converter applications is increasing day by day and different types of multilevel inverters are being invented. Out of these inverters, only those with higher efficiency and low total harmonic distortion are being utilized. so, it is evident that the one with low THD is have greater influence in today's inverter markets. The harmonic contents in the AC power are reduced to their minimum amount by generating a high number of levels in the output sinusoidal waveform. So, with increasing the levels in the output the harmonic components are reduced. This can be achieved by increasing the number of power switches utilized in the inverter but it also affects the efficiency by increasing switching power loss. So there must be a reasonable balance between the number of power switches utilized and switching power losses.

The figure(1) shows the multiple stages that an inverter should have before obtaining 15 level Sinusoidal output. Hence, making it a 15 level MLI. The block diagram shows that the input introduced into circuit is taken from solar PV module which can replaced by battery of same voltage during practical application.

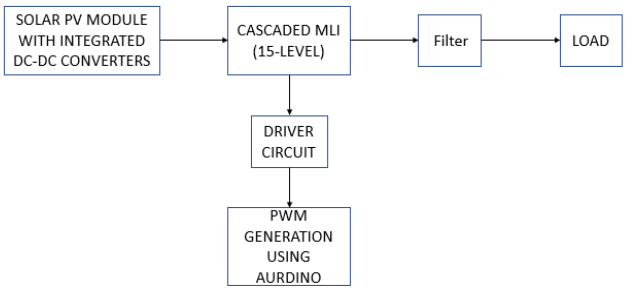

Fig (1) Block Diagram of 15 level MLI using Arduino Controller

In general, there are three different Multilevel inverters topologies:

1. Diode clamped multilevel inverter
2. Flying capacitors multilevel inverter
3. Cascaded H- bridge multilevel inverter

Diode clamped multilevel inverter

The idea behind this inverter is to utilize diodes that generate multiple voltage levels in the output waveform through the different phases to the capacitor banks which are connected in series. The original concept can be extended by increasing the number of capacitors that are connected in series [1]. The main drawback of this inverter is that the maximum AC output is 50% of the input DC. This can be resolved by increasing the number of diodes, capacitors, and switches which again might give rise to the switching power losses because of increased components. Due to this imbalance of components, this inverter is limited to 3 level inverters.

Flying capacitors multilevel inverter

The flying capacitor multilevel converter is developed in the year 2003 converter topology assuring a flexible control. However, the flying capacitor multilevel converter requires balanced DC voltage distribution. This can be realized by using special control leading to natural balancing or by measuring the voltages and selecting the appropriate switching state. The balancing is mostly influenced by three factors, namely the harmonics, the switching frequency and the load impedance.

Cascaded H- bridge multilevel inverter

The combination of capacitors and switches pair is called an H-bridge and gives the separate input DC voltage for

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each H-bridge. It consists of H-bridge cells and each cell can provide the three different voltages like zero, positive DC, and negative DC voltages. One of the basic and well-known topologies among all multilevel inverters is Cascaded H-Bridge Multilevel Inverter. It can be used for both single and three phase conversion. It uses H-Bridge including switches and diodes.

At least three voltage levels are required for a multilevel inverter. This can be accomplished by a single H-Bridge unit in Cascaded H-Bridge Multilevel Inverter. This H-Bridge topology is utilized in this project

II. EXISTING SYSTEM

In the existing system H-bridge Multi Level Inverter is used to achieve the Total Harmonic Reduction without using voltage balancing technique. The number of switches used in the system is high compare with proposed system In the symmetric topology, the values of all of the dc voltage sources are equal. This characteristic gives the topology good modularity. However, the number of the switching devices rapidly increases by increasing the number of output voltage level [2].

In order to increase the number of output voltage level, the values of the dc voltage sources are selected to be different, these topologies are called asymmetric.

In normal fifteen level cascaded inverter is required for 28 switches to produce the fifteen-level1 output. And also required for 7 sources. If 28 switch means the PWM pulses are generates complicated. So, this 15-level inverter is used to less number of power switches [2].

III. PROPOSED SYSTEM

The CHB includes full-bridge single-phase inverter as a cell that generates three voltage levels ($+V_{dc}$, 0, $-V_{dc}$). Using more cells in each phase or using unequal DC sources in each cell produce more voltage levels at the output which reduce the voltage harmonics. If the number of cells is m, the inverter level would be 2m+1 in case of using equal DC sources in every cell, and it would be more if using unequal DC sources.

The inverter is a five level one with two equal DC sources and the output voltage is as the following:

$$V_{an}=V_1+V_2 \quad (1)$$

Equation(1.1) Output Voltage of five level Inverter

Where, the V1 and V2 are the output voltages of each cell. Van is the phase voltage. This multilevel inverter has three DC sources and six switches that can generate five-level voltage at Van while using three equal sources as: Vdc1=Vdc2=Vdc3=n (volts).

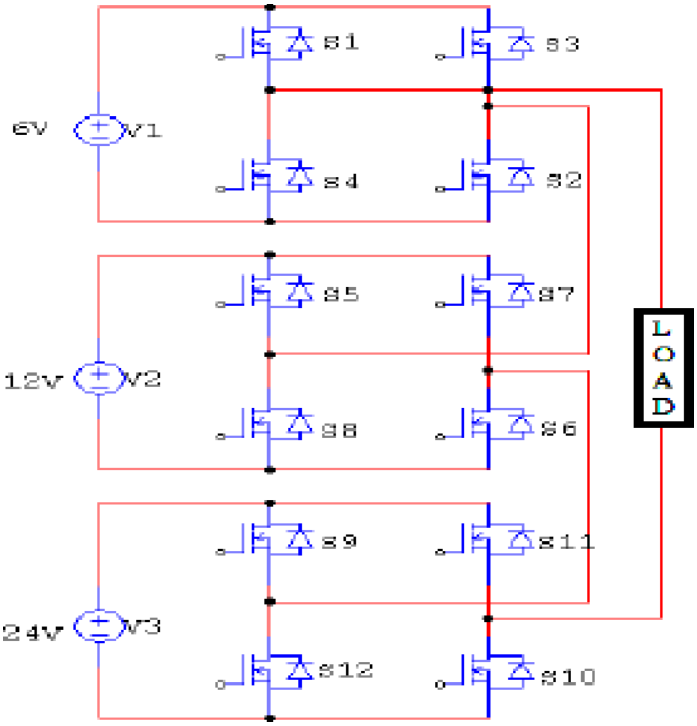

fig (2): Circuit Diagram For Proposed 15 level MLI

By considering the voltage sharing of the half-bridge cell it is clear that in each switching cycle, one of the DC sources are connected to the output and the other is remained unconnected. Therefore, one DC source with two series capacitors can be used as DC source of the half-bridge cell. The middle point of the capacitors is connected to the next cell and the designed switching technique deals with balancing the voltage[3,4].

Switching Mode of Operation For 15 Level Proposed Inverter

Output Voltage	Switching States											
	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12
$7V_{dc}$	1	1	0	0	1	1	0	0	1	1	0	0
$6\ V_{dc}$	0	1	0	1	1	1	0	0	1	1	0	0
$5\ V_{dc}$	1	1	0	0	0	1	0	1	1	1	0	0
$4\ V_{dc}$	0	1	0	1	0	1	0	1	1	1	0	0
$3\ V_{dc}$	1	1	0	0	1	1	0	0	0	1	0	1
$2\ V_{dc}$	0	1	0	1	1	1	0	0	0	1	0	1
$1\ V_{dc}$	0	0	1	1	1	1	0	0	0	1	0	1
$0\ V_{dc}$	0	1	0	1	0	1	0	1	0	1	0	1
$-1\ V_{dc}$	1	1	0	0	0	0	1	1	0	1	0	1
$-2\ V_{dc}$	0	1	0	1	0	0	1	1	0	1	0	1
$-3\ V_{dc}$	0	0	1	1	0	0	1	1	0	1	0	1
$-4\ V_{dc}$	0	1	0	1	0	1	0	1	0	0	1	1
$-5\ V_{dc}$	0	0	1	1	0	1	0	1	0	0	1	1
$-6\ V_{dc}$	0	1	0	1	0	0	1	1	0	0	1	1
$-7\ V_{dc}$	0	0	1	1	0	0	1	1	0	0	1	1

Table(1) Switching states of the 15-level Cascaded inverter

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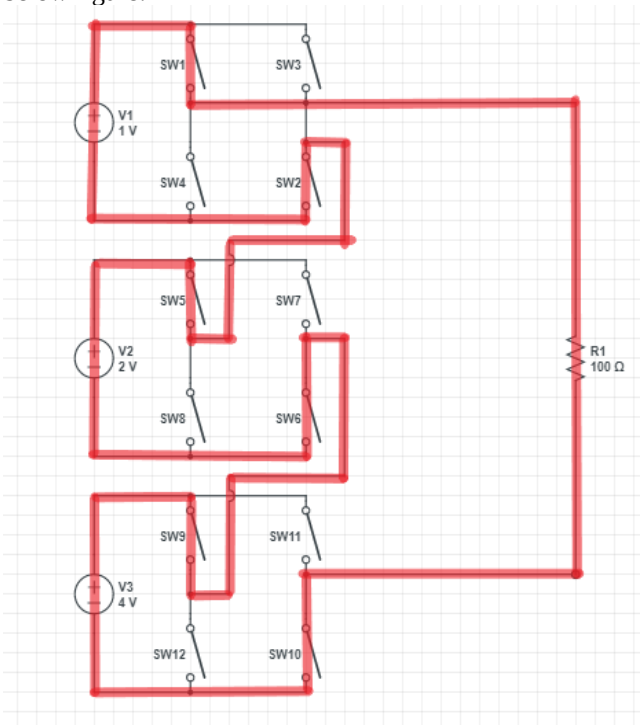
IV. 15 MODES OF OPERATION

Mode1: Maximum Positive output Voltage (7_{Vdc}):

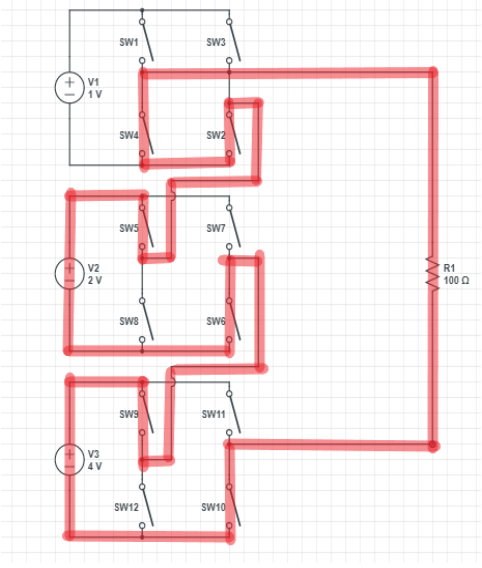
When MOSFET switches SW_1, SW_2,SW_5, SW_6, SW_9 and SW_{10} are turned in to ON-State and switches SW_4, SW_3, SW_7, SW_8, SW_{11} and SW_{12} are turned in to OFF-State, the maximum voltage i.e., positive 7_{th} level voltage is see across resistor load. The current flow direction is given in below figure:



Fig(3) Maximum Positive output Voltage (7_{Vdc})

Mode 2: Positive output voltage (6Vdc/7)

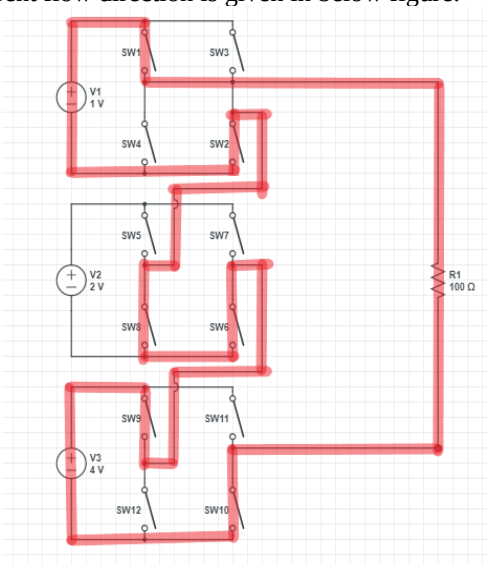
When MOSFET switches SW_4, SW_2,SW_5, SW_6, SW_9 and SW_{10} are turned in to ON-State and switches SW_1, SW_3, SW_7, SW_8, SW_{11} and SW_{12} are turned in to OFF-State, the positive 6_{th} level voltage is see across resistor load. The current flow direction is given in below figure:



Fig(4) Output Voltage level Vo = 6_{Vdc}

Mode 2: Positive output voltage (5Vdc/7)

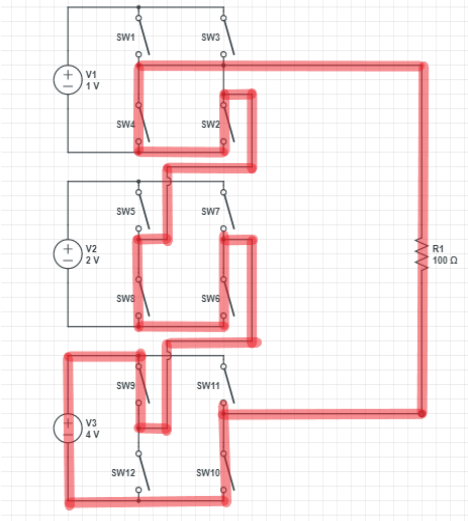
When MOSFET switches SW_1, SW_2,SW_8, SW_6, SW_9 and SW_{10} are turned in to ON-State and switches SW_4, SW_3, SW_7, SW_5, SW_{11} and SW_{12} are turned in to OFF-State, the positive 5_{th} level voltage is see across resistor load. The current flow direction is given in below figure:



Fig(5) . Output Voltage level $V_0 = 5_{Vdc}$

Mode 4: Positive output voltage (4Vdc/7)

When MOSFET switches SW_4, SW_2,SW_8, SW_6, SW_9 and SW_{10} are turned in to ON-State and switches SW_1, SW_3, SW_7, SW_5, SW_{11} and SW_{12} are turned in to OFF-State, the positive 4_{th} level voltage is see across resistor load. The current flow direction is given in below figure:



Fig(6) Output Voltage level $V_0 = 4_{Vdc}$

Mode 5: Positive output voltage (3Vdc/7):

When MOSFET switches SW_1, SW_2,SW_5, SW_6, SW_{12} and SW_{10} are turned in to ON-State and switches SW_4, SW_3, SW_7, SW_8, SW_9 and SW_{11} are turned in to OFF-State, the positive 3_{rd} level voltage is see across resistor load. The current flow direction is given in below figure:

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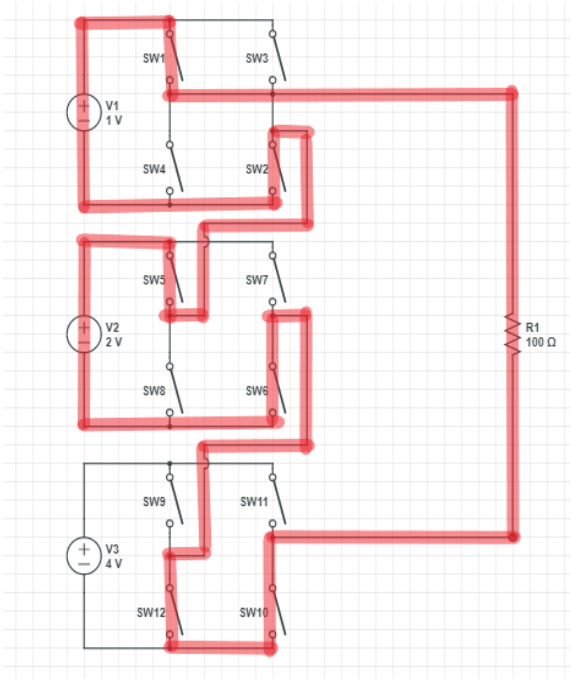
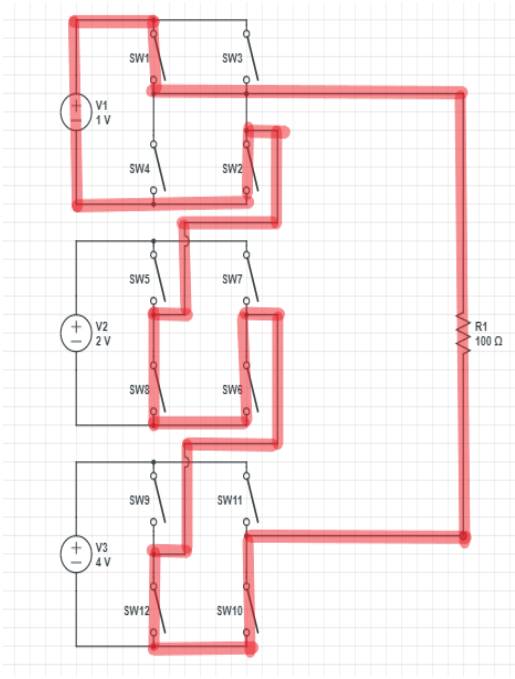


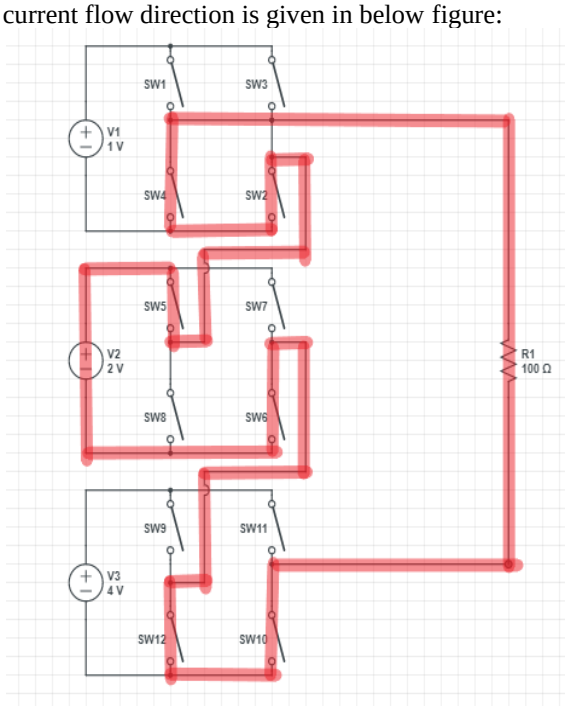
Fig(7)Output Voltage level $V_0 = 3_{Vdc}$



Fig(9) Output Voltage level $V_0 = 1_{Vdc}$

Mode 6: Positive output voltage (2Vdc/7)

When MOSFET switches SW_4, SW_2,SW_5, SW_6, SW_{12} and SW_{10} are turned in to ON-State and switches SW_1, SW_3, SW_7, SW_8, SW_{11} and SW_9 are turned in to OFF-State, the positive 2_{nd} level voltage is see across resistor load. The current flow direction is given in below figure:



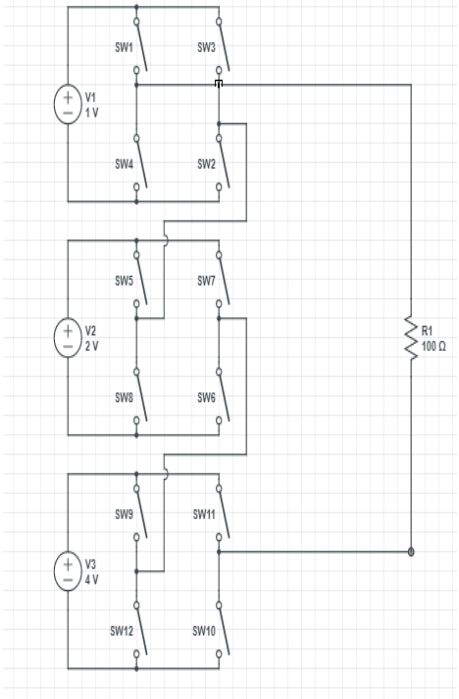
Fig(8) Output Voltage level $V_0 = 2_{Vdc}$

Mode 7: Positive output voltage (Vdc/7)

When MOSFET switches SW_1, SW_2,SW_8, SW_6, SW_{12} and SW_{10} are turned in to ON-State and switches SW_4, SW_3, SW_7, SW_5, SW_{11} and SW_9 are turned in to OFF-State, the positive 1_{st} level voltage is see across resistor load. The current flow direction is given in below figure:

Mode 8: Zero Output voltage (0Vdc)

When MOSFET switches SW_4, SW_2,SW_5, SW_6, SW_9 ,SW_{10} , SW_1, SW_3, SW_7, SW_8, SW_{11} and SW_{12} are turned in to OFF-State, the zero voltage i.e., 0_{th} level voltage is see across resistor load.



Fig(10) Output Voltage level $V_0 = 0_{Vdc}$

Mode 9: Negative Output voltage(-1Vdc/7)

When MOSFET switches SW_1, SW_2,SW_8, SW_6, SW_{12} and SW_{10} are turned in to ON-State and switches SW_4, SW_3, SW_7, SW_5, SW_{11} and SW_9 are turned in to OFF-State, the negative 1_{st} level voltage is see across resistor load. The current flow direction is given in below figure:

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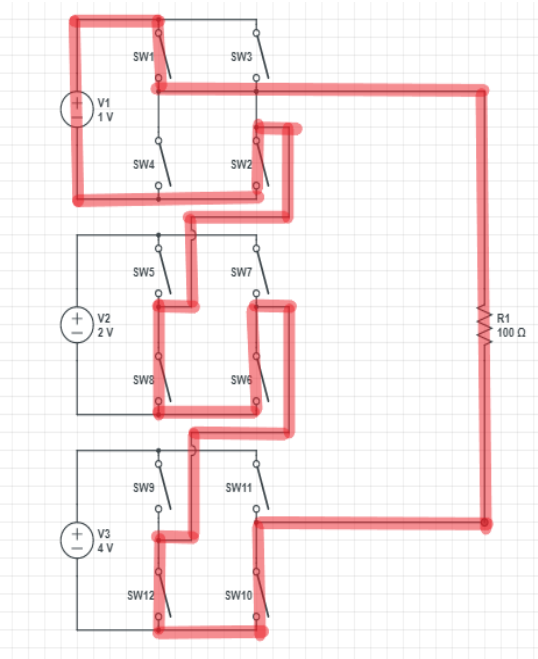


Fig (11) Output Voltage level V_{ab} = -1_{Vdc}

Mode 10: Negative Output voltage(-2Vdc/7)

When MOSFET switches SW_4, SW_2,SW_8, SW_7, SW_{12} and SW_{10} are turned in to ON-State and switches SW_1, SW_3, SW_6, SW_5, SW_{11} and SW_9 are turned in to OFF-State, the negative 2_{nd} level voltage is see across resistor load. The current flow direction is given in below figure:

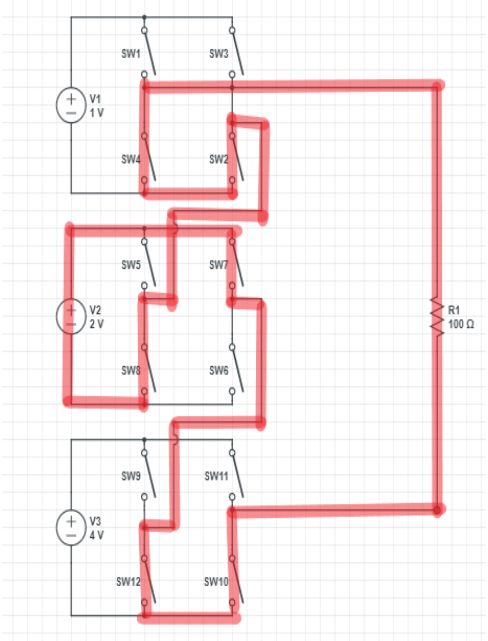


Fig (12) Output Voltage level V_{ab} = -2_{Vdc}

Mode 11: Negative Output voltage(-3Vdc/7):

When MOSFET switches SW_3, SW_4,SW_8, SW_7, SW_{12} and SW_{10} are turned in to ON-State and switches SW_1, SW_2, SW_6, SW_5, SW_{11} and SW_9 are turned in to OFF-State, the negative 3_{rd} level voltage is see across resistor load. The current flow direction is given in below figure:

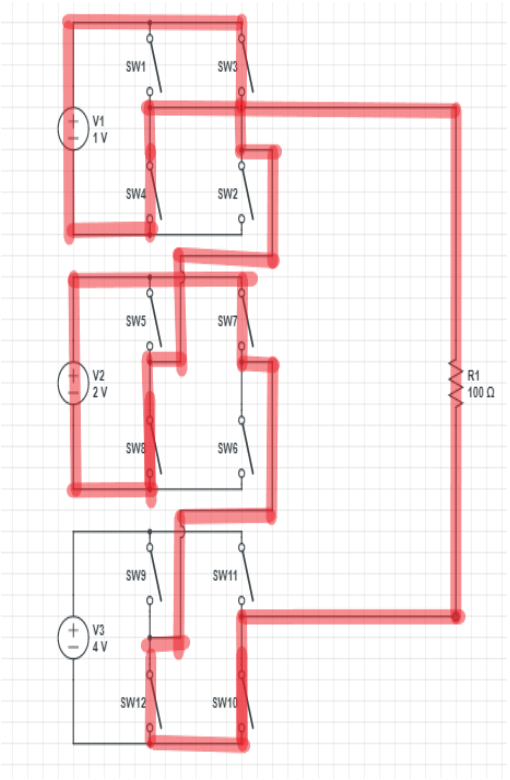
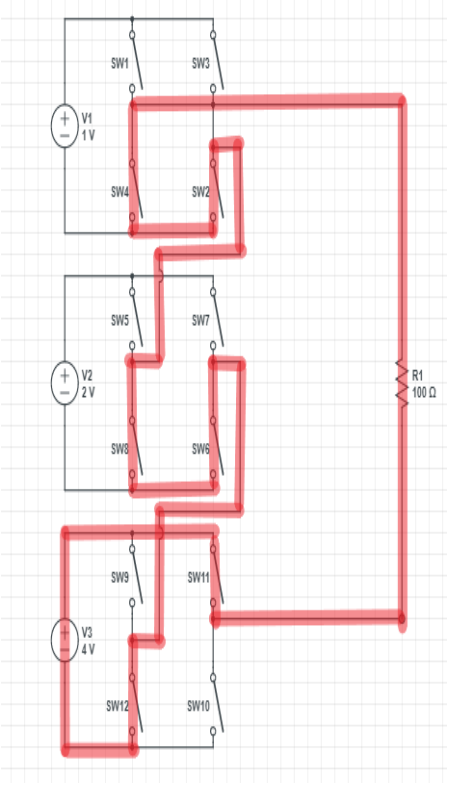


Fig (13) Output Voltage level V_{ab} = -3_{Vdc}

Mode 12: Negative Output voltage(-4Vdc/7)

When MOSFET switches SW_4, SW_2,SW_8, SW_6, SW_{12} and SW_{11} are turned in to ON-State and switches SW_1, SW_3, SW_7, SW_5, SW_{10} and SW_9 are turned in to OFF-State, the negative 4_{th} level voltage is see across resistor load. The current flow direction is given in below figure:



Fig(14) Output Voltage level V_{ab} = -4_{Vdc}

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Mode 13: Negative Output voltage(-5Vdc/7)

When MOSFET switches SW_4, SW_3,SW_8, SW_6, SW_{12} and SW_{11} are turned in to ON-State and switches SW_1, SW_2, SW_7, SW_5, SW_{10} and SW_9 are turned in to OFF-State, the negative 5_{th} level voltage is see across resistor load. The current flow direction is given in below figure:

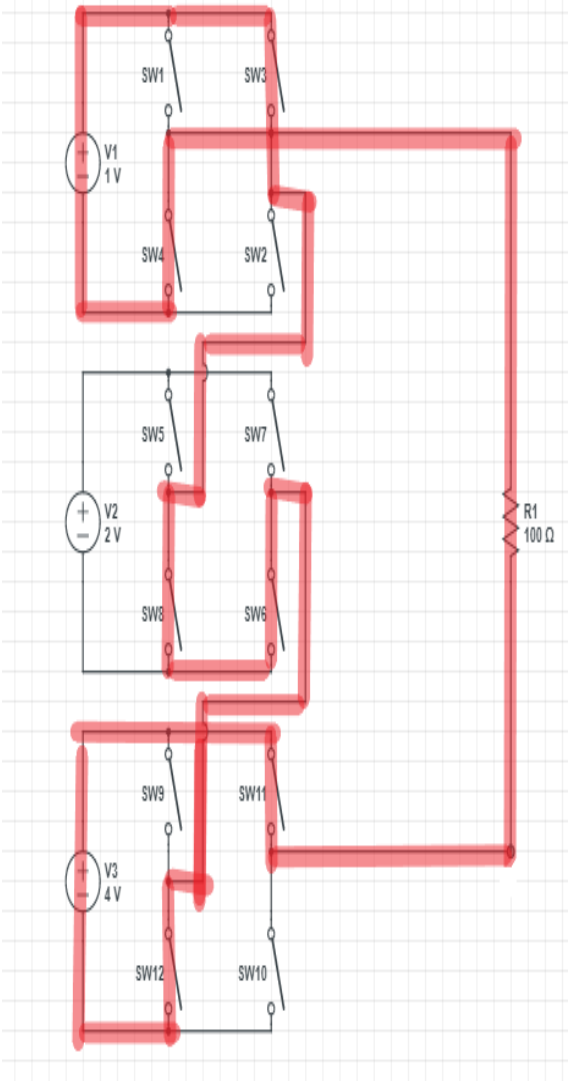

Fig (15) Output Voltage level $V_{ab} = -5_{Vdc}$

Mode 14: Negative Output voltage(-6Vdc/7)

When MOSFET switches SW_4, SW_2,SW_8, SW_7, SW_{12} and SW_{11} are turned in to ON-State and switches SW_1, SW_3, SW_6, SW_5, SW_{10} and SW_9 are turned in to OFF-State, the negative 6_{th} level voltage is see across resistor load. The current flow direction is given in below figure:

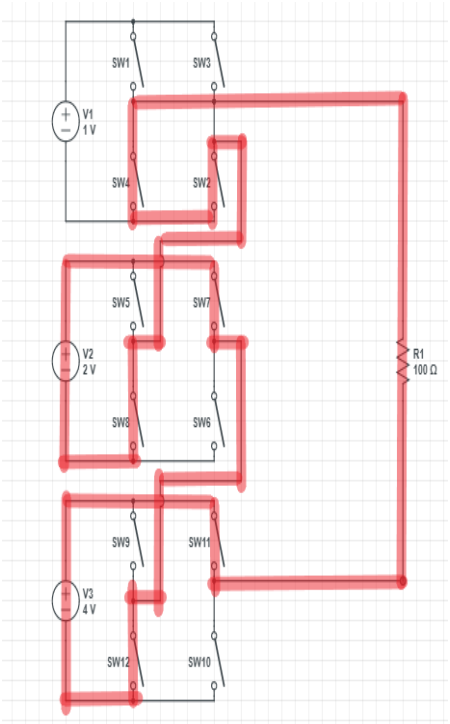

Fig (16) Output Voltage level $V_{ab} = -6_{Vdc}$

Mode 15: Negative Output voltage(-Vdc)

When MOSFET switches SW_4, SW_3,SW_8, SW_7, SW_{12} and SW_{11} are turned in to ON-State and switches SW_1, SW_2, SW_6, SW_5, SW_1 and SW_9 are turned in to OFF-State, the negative 7_{th} level voltage is see across resistor load. The current flow direction is given in below figure:

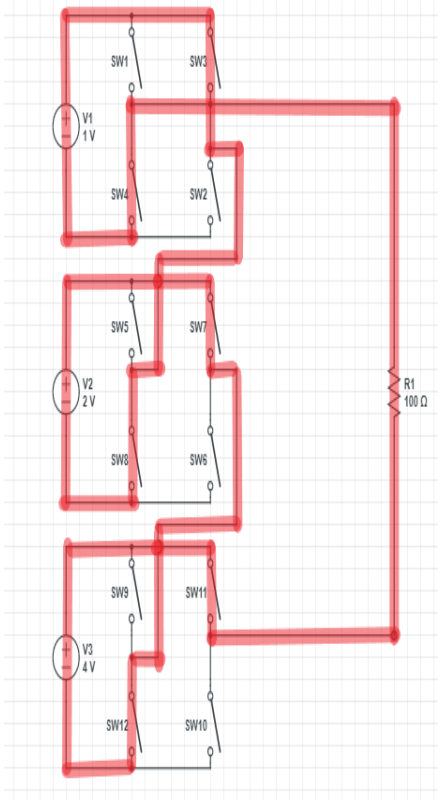

Fig (17) Output Voltage level $V_{ab} = -7_{Vdc}$

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V. SIMULATION AND EXPERIMENTAL SETUP

Simulation Circuit

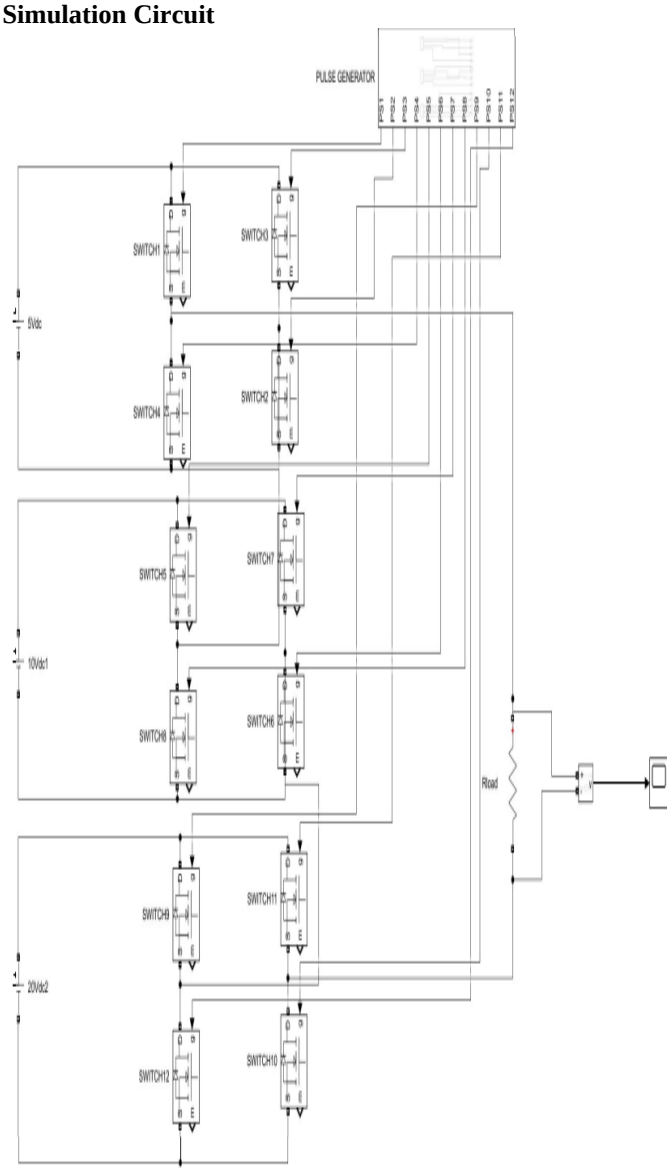


Fig (18) Simulation Circuit Of Proposed System

Pulse Generator Circuits for Different Power Switches

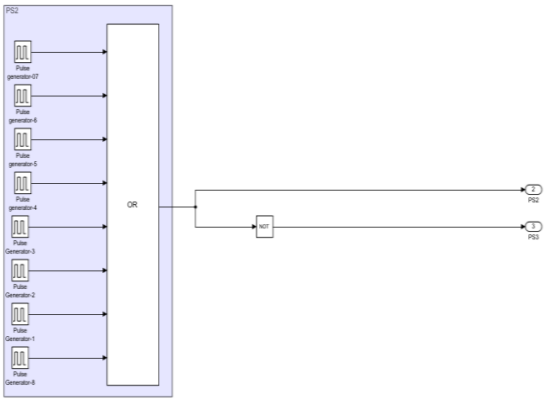


Fig (19) Pulse Generator Circuit For S_{w2} and S_{w3}

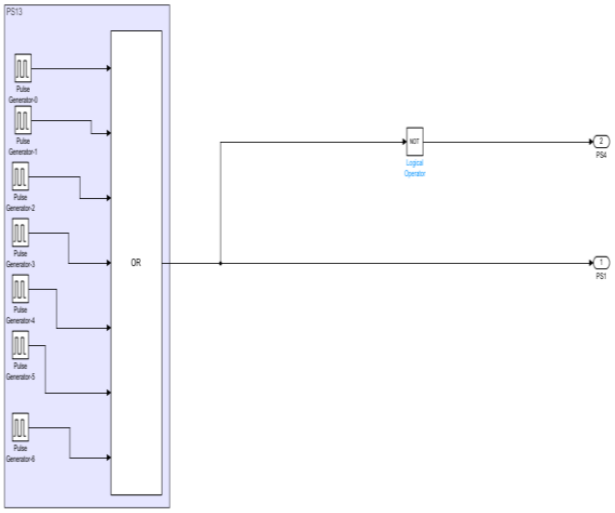


Fig (4.3) Pulse Generator Circuit For S_{w1} and S_{w4}

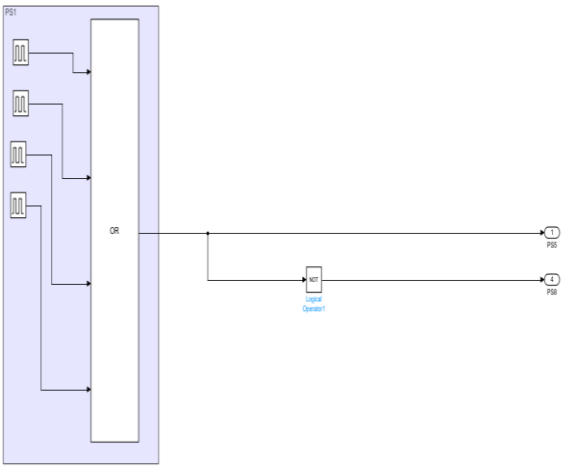
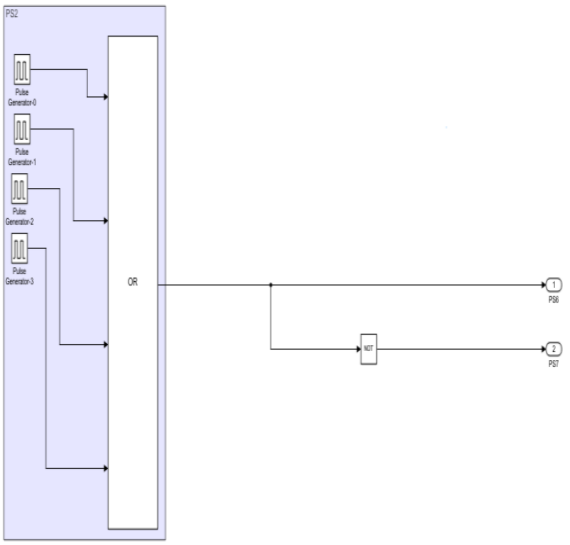


Fig (20) Pulse Generator Circuit For S_{w5} and S_{w8}



Fig(21) Pulse Generator Circuit For S_{w7} and S_{w6}

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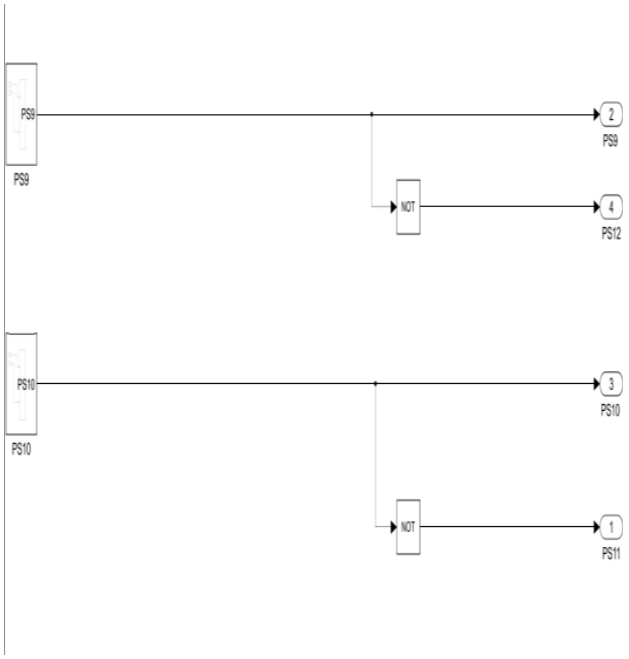
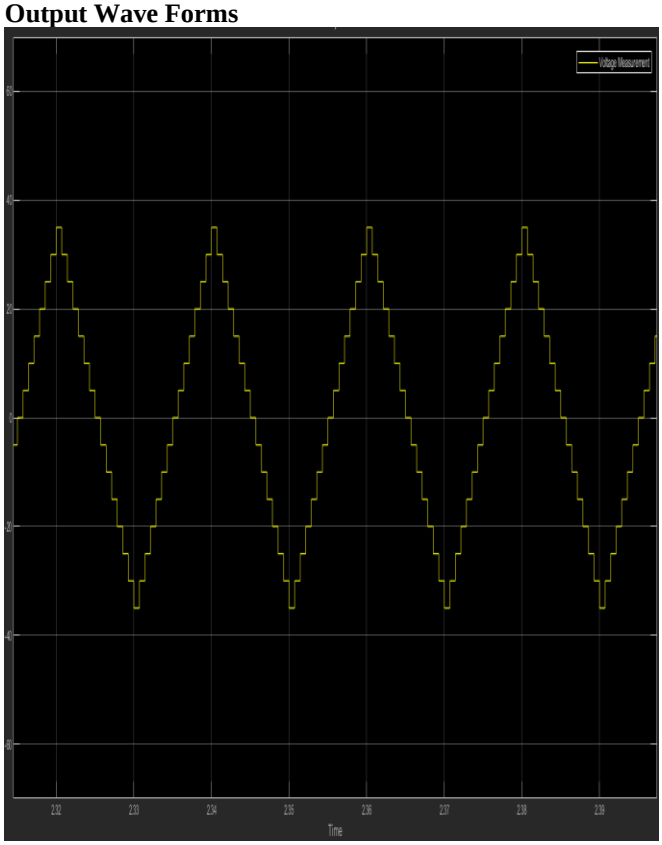
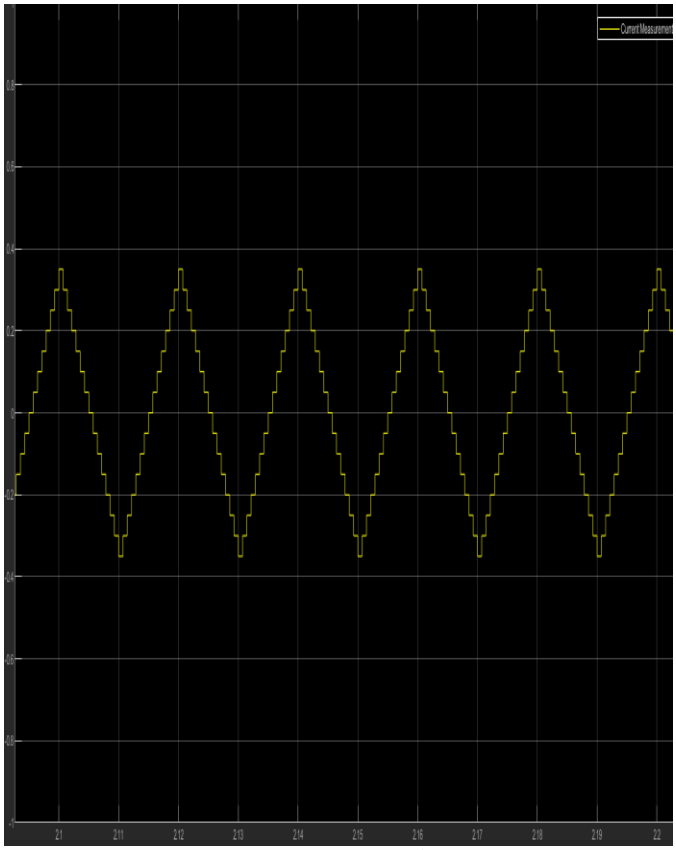


Fig (22) Pulse Generator Circuit For S_{w9},S_{w12},$S_{w10}$and S_{w11}

Output Wave Forms

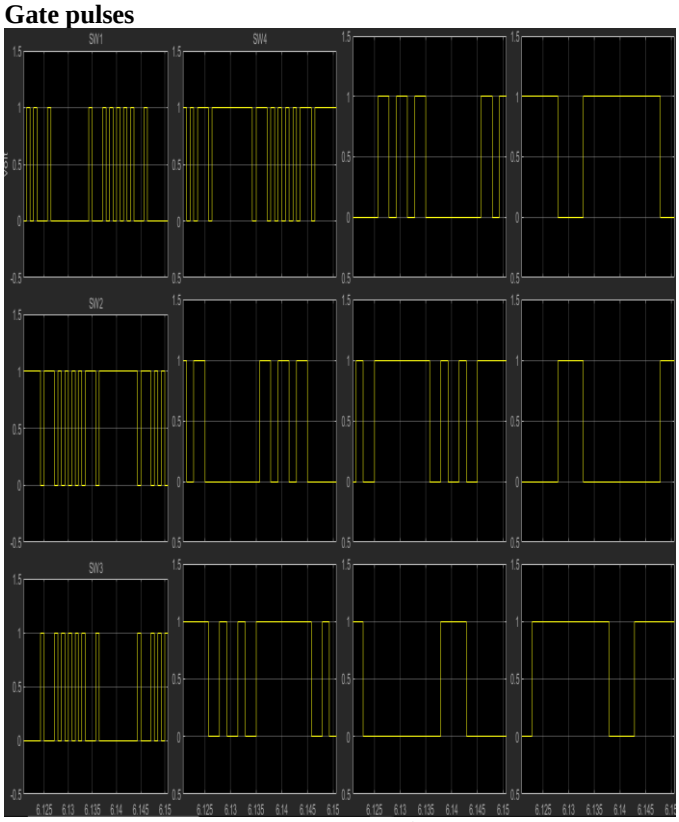


Fig(23):Output Voltage Waveform



Fig(24):Ouput current Waveform

Gate pulses



Fig(25):Gate Pulses Waveform

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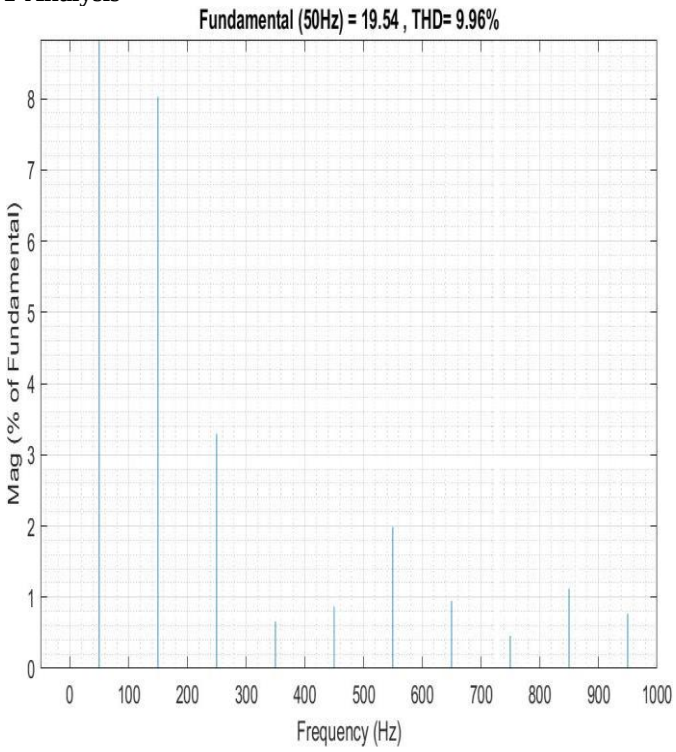
FFT Analysis



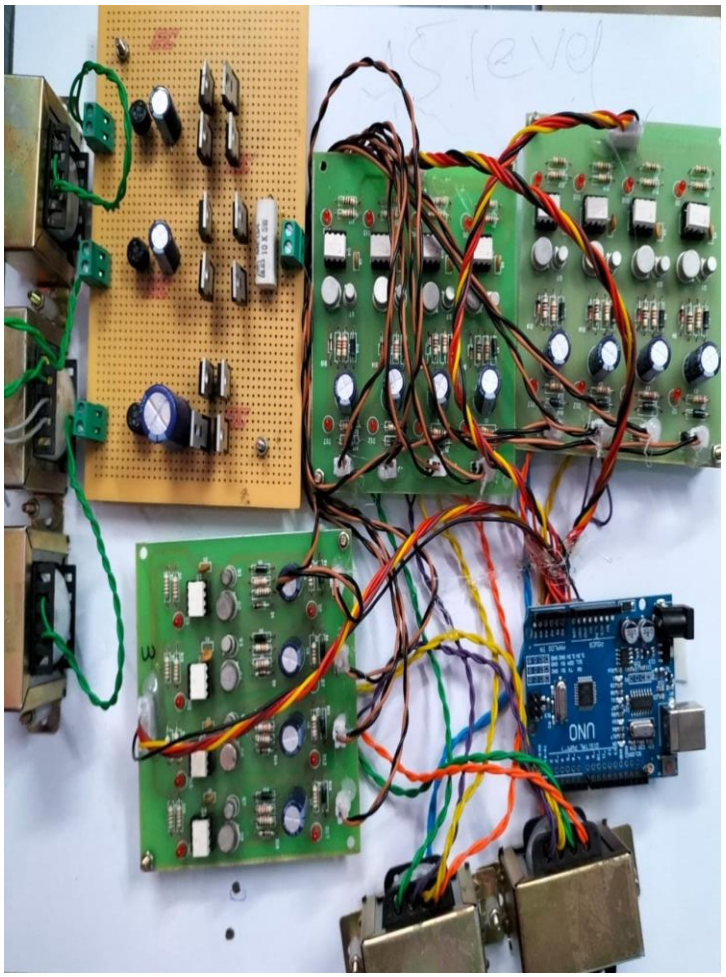
Fig(26):FFT Analysis

6 IMPLEMENTATION OF 15 LEVEL MLI USING ARDUINO CONTROLLER FOR EXPERIMENTAL RESULTS

This section describes the experimental results for reduced switch asymmetric multilevel to examine 15-level output voltage using the ARDUINO ATMEGA 228 system. ARDUINO was used for real-time implementation, which usually includes an on-chip PWM controller to reduce the complexity of PWM signal generation. Multi-carrier PWM strategies with a unipolar trapezoidal reference were used for generating the PWM signal to the selected topology and this technique is show in this paper [x]. The simulation part was implemented in MATLAB/Simulink (2020a) ((PWM signal generation)) and converted into an input signal of ARDUINO through the Xilinx software (compiled and converted into bits and then downloaded into ARDUINO for execution in the real-time process). The below Figure depicts the laboratory-based experimental setup for reduced switch AMLI. The experimental setup consists of power converter module MLI and gate terminals are trigger through FPGA digital processor and is programmed through Xilinx software. The hardware parameters include the voltage value of the DC sources Vdc1= 6 V, V_{dc2}=12V and V_{dc3}= 24V the R load value is 10kΩ, and the switching carrier frequency (fc) as 2000 Hz.

Additionally, to the main circuit there is a secondary circuit called driver circuit. This driver circuit is used amplify the GATE pulses for MOSFET switch.

Fig(4.11):Driver Circuit



Fig(4.12):Experimental Setup of 15 level MLI

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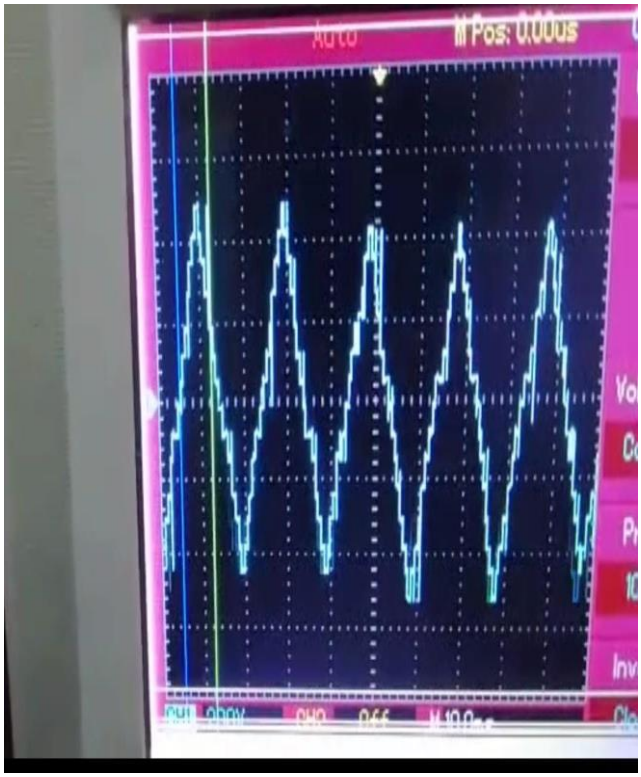

Fig(4.13):Output 15 level Sinusoidal waveform

VI. CONCLUSION

This work has covered the simulation and experiment of 15-level multilevel inverter and closed loop multilevel inverter fed drives using MATLAB/SIMULINK software and Arduino controller. The simulation work suggest that this is the easy way to get desired output voltage with minimum THD and most importantly this work is mainly focused on reducing THD percentage. In this paper a the modelling of 15 level multilevel inverter using cascaded inverters with separated DC source has been modelled. Simulation and Experiment results are obtained from various operations done by using 1 kHz switching frequency and a passive load. The proposed control algorithm used in the 15 level inverter can be easily applied to multilevel inverters. The total harmonic distortion is very low compared to that symmetrical 15 Level MLI. The simulation and experiment results show that the harmonics have been diminished considerably. The Experiment and simulation outcomes are in line with the forecasted values.

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