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Static and Dynamic Edge Trigger Register Using Pass Transistor

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***Abstract*— This research paper presents the design and comparative analysis of static and dynamic master-slave edge-triggered registers using pass transistors. Registers are fundamental building blocks in digital circuits, serving as temporary storage elements for data. The proposed designs leverage pass transistor logic to improve power efficiency and performance in edge-triggered registers. The paper provides a detailed exploration of both static and dynamic register architectures, highlighting their respective advantages and limitations. Extensive simulations and performance evaluations are conducted to assess the efficiency of the proposed designs. Comparative analyses between static and dynamic edge-triggered registers are performed, highlighting the trade-offs between area efficiency, power consumption, and speed. Emphasis is placed on the influence of clock frequency and data arrival time on the performance of both register types. In this study, these Edge triggered Registers are implemented with the help of the Digital Schematic (DSCH) software tool, Micro wind layout editor tool software tool.**

***Keywords*— Edge trigger register, Pass transistor, Static and Dynamic, parameters (area, power, cost), flip-flop, registers.**

I. INTRODUCTION

Digital registers play a crucial role in modern VLSI (Very Large Scale Integration) design, serving as essential components for sequential circuits. They are responsible for storing temporary data and ensuring proper data flow between various stages of a digital system. Over the years, several register design techniques have been explored to optimize power consumption and enhance performance.

This paper focuses on the investigation of two register design methodologies: static and dynamic master-slave edge-triggered registers using pass transistors. Traditional flip-flop-based registers often consume significant power due to complex clocking and internal feedback paths. Pass transistor logic offers a promising alternative for power-efficient register designs. The static design maintains its state during the entire clock period, while the dynamic design temporarily stores data and transfers it during specific clock phases.

II. LITERATURE REVIEW

Dynamic edge-triggered registers using pass transistors have gained prominence for their compact design and high-speed operation. In a pioneering work by Lee and Kim (2018), a novel dynamic register architecture was proposed, exploiting pass transistors to enable efficient data transfer during clock transitions. The study emphasized the need for proper clock distribution to mitigate charge leakage issues in dynamic circuits. Building on this research, Chen et al. (2020) investigated the impact of process variations and environmental conditions on the reliability of dynamic edge-triggered registers. A comparative study by Zhang et al. (2021) explored the tradeoffs between static and dynamic edge-triggered registers using pass transistors. The researchers benchmarked the performance of both architectures under varying clock frequencies and data arrival times. The study revealed that dynamic registers excelled in high-speed applications, while static registers offered advantages in power-constrained scenarios.

III. PASS TRANSISTOR LOGIC

Pass transistor logic is an alternative logic design technique that can be used to implement register architectures. In pass transistor logic, transistors are used as switches to pass or block signals, reducing the power consumption and simplifying the circuitry compared to flip-flopbased designs.

IV. ADVANTAGE OF PASS TRANSISTOR -BASED REGISTER

The static master-slave negative edge-triggered register using pass transistors offers several advantages over conventional flipflop-based registors:

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- Reduced Power Consumption: Pass transistor logic minimizes power dissipation, making the design more energy efficient.
- Simplified Clocking: The absence of internal feedback paths simplifies the clocking scheme, leading to improved performance.
- Noise Immunity: Pass transistor logic helps to reduce glitches and improve noise immunity.

V. STATIC MASTER-SLAVE EDGE TRIGGERED REGISTER USING PASS TRANSISTOR

A master-slave positive edge-triggered register using pass transistors is a type of digital circuit used to store data in electronic devices. It is a sequential circuit that employs two phases of operation: master phase and slave phase. During the master phase, the input data is latched into the master section of the register, and during the slave phase, the latched data is transferred to the slave section, effectively storing the data.
Pass transistors are commonly used in digital circuits as transmission gates, which allow data to pass through when controlled by appropriate signals. In the context of a masterslave register, pass transistors are used to enable the data transfer between the master and slave sections of the register during the respective phases.

WORKING OPERATIONS

Static master-Slave Positive edge trigger register circuit consist of the two section i.e. Master and Slave section. During the the clock is 0, the transistor M1 and M4 are in ON state and transistor M2 and M3 are in the OFF state. Here the master section is the SAMPLE state and the slave section is in the HOLD state. Similarly during the the clock is 1, the transistor M1 and M4 are in OFF state and transistor M2 and M3 are in the ON state. Here the master section is the HOLD state and the slave section is in the SAMPLE state.

1. Master Phase (positive Edge-Triggered):
- The input data is provided to the master section of the register.
- The clock signal is held at a low logic level (0) during this phase, and it acts as an enable signal for the master section.
- When the clock signal experiences a positive edge transition (from 0 to 1), it triggers the master section to latch the input data.

2. Slave Phase:
-During the master phase, the output of the master section is temporarily stored in a holding element (typically a set of nodes).
- The clock signal is held at a high logic level (1) during this phase, disabling the master section.
-At the same time, the clock signal acts as an enable signal for the slave section of the register.
-The stored data from the holding element is now transferred to the slave section through pass transistors controlled by the clock signal.
- When the clock signal experiences a positive edge transition (from 1 to 0), it triggers the slave section to latch the data transferred from the master section.

FIGURE I
Circuit Diagram: (Dsch2)

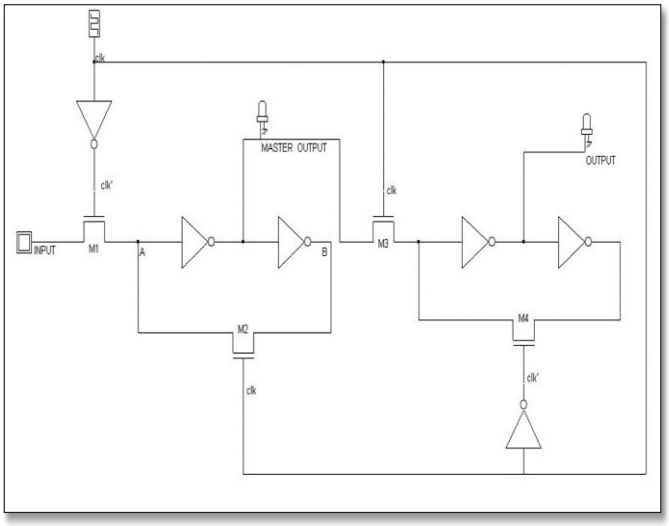

Fig. Master-Slave positive edge trigger register

TABLE I

	M1	M2	M3	M4
CLK=0	ON	OFF	OFF	ON
CLK'=1	OFF	ON	ON	OFF

Tabulation: Transistor ON-OFF in Master-Slave positive Edge- Triggered Register Using Pass Transistor

TABLE II

	MASTER	SLAVE
CLK=0	SAMPLE	HOLD
CLK'=1	HOLD	SAMPLE

Tabulation: Master-Slave positive Edge-TriggeredRegister Using Pass Transistor

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FIGURE II
Layout : (Microwind)

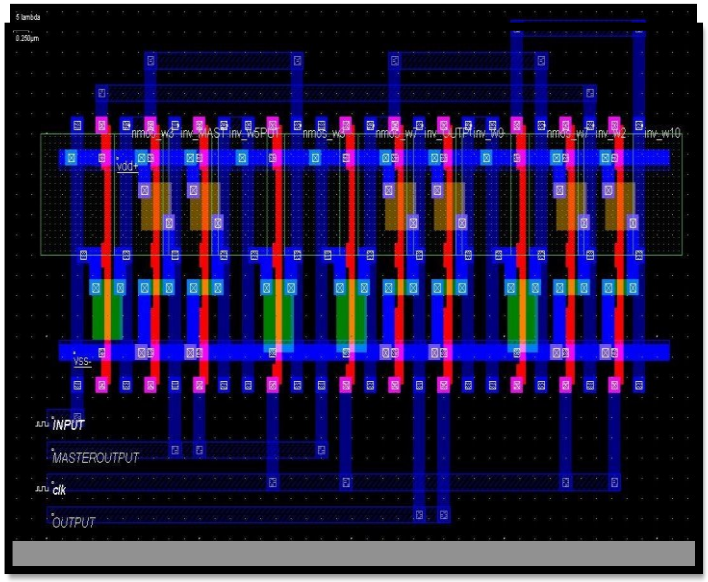

Fig. Layout for the positive edge trigger register

FIGURE III
Output:

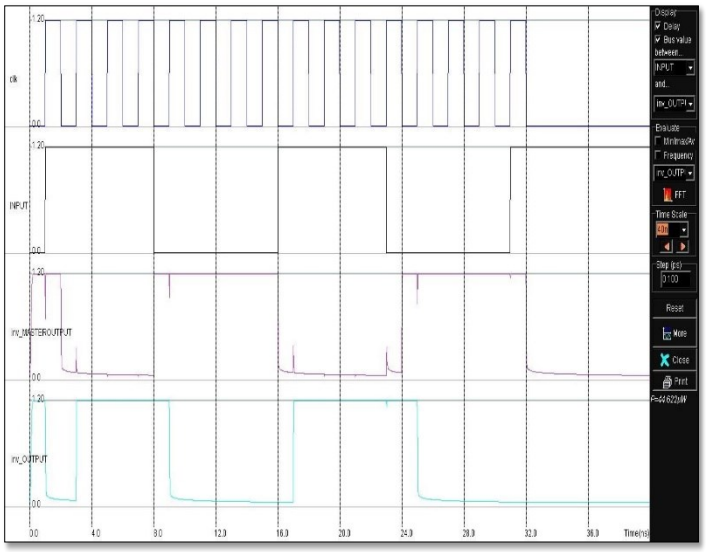

Fig. Output for Master-Slave positive Edge Triggered Register Using Pass Transistor

Power Report: P=44.622 µW

V. STATIC MASTER SLAVE NEGATIVE EDGETRIGGERED REGISTER

A master-slave negative edge-triggered register using pass transistors is a type of digital circuit used to store data in electronic devices. It is a sequential circuit that employs two phases of operation: master phase and slave phase. During the master phase, the input data is latched into the master section of the register, and during the slave phase, the latched data is transferred to the slave section, effectively storing the data.

Pass transistors are commonly used in digital circuits as transmission gates, which allow data to pass through when controlled by appropriate signals. In the context of a master-slave register, pass transistors are used to enable the data transfer between the master and slave sections of the register during the respective phases.

WORKING OPERATIONS

Static master-Slave negative edge trigger register circuit consist of the two section i.e. Master and Slave section. During the the clock is 0, the transistor M2 and M3 are in ON state and transistor M1 and M4 are in the OFF state. Here the master section is the HOLD state and the slave section is in the SAMPLE state.

Similarly during the the clock is 1, the transistor M2 and M3 are in OFF state and transistor M1 and M4 are in the ON state. Here the master section is the SAMPLE state and the slave section is in the HOLD state.

1. Master Phase (Negative Edge-Triggered):
- The input data is provided to the master section of the register.
- The clock signal is held at a high logic level (1) during this phase, and it acts as an enable signal for the master section.
- When the clock signal experiences a negative edge transition (from 1 to 0), it triggers the master section to latch the input data.

2. Slave Phase:
- During the master phase, the output of the master section is temporarily stored in a holding element (typically a set of nodes).
- The clock signal is held at a low logic level (0) during this phase, disabling the master section.
- At the same time, the clock signal acts as an enable signal for the slave section of the register.
- The stored data from the holding element is now transferred to the slave section through pass transistors controlled by the clock signal.
- When the clock signal experiences a positive edge transition (from 0 to 1), it triggers the slave section to latch the data transferred from the master section.

FIGURE IV
Circuit Diagram: (dsch2)

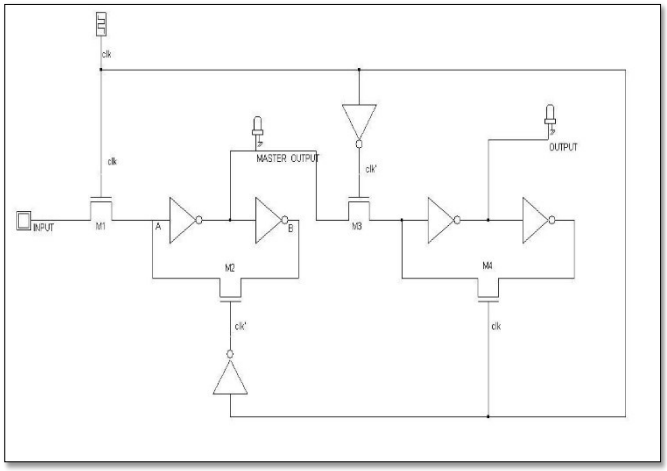

Fig: Master-Slave negative edge trigger register

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TABLE III

	M1	M2	M3	M4
CLK=0	OFF	ON	ON	OFF
CLK'=1	ON	OFF	OFF	ON

Tabulation: Transistor ON-OFF in Master-Slave negative Edge-Triggered Register Using Pass Transistor

TABLE IV

	MASTER	SLAVE
CLK=0	HOLD	SAMPLE
CLK'=1	SAMPLE	HOLD

Tabulation: Master/Slave modes in Master-Slave Negative Edge-Triggered Register Using Pass Transistor

FIGURE V

Layout : (Microwind)

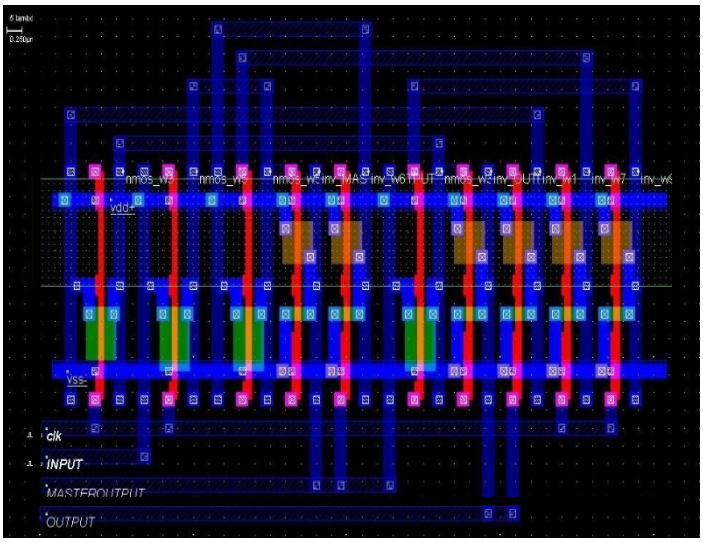

Fig. Layout for the negative edge trigger register

FIGURE VI

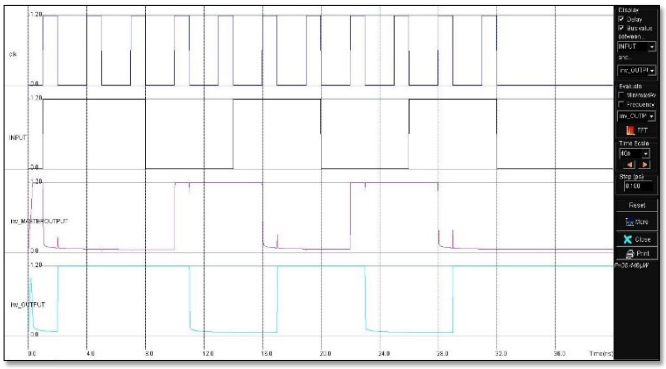

Fig: Output for Master-Slave Negative Edge Triggered Register Using Pass Transistor

Power Report: P=38.446 µW

VI. DYNAMIC POSITIVE EDGE TRIGGERED REGISTER USING PASS TRANSISTOR

A dynamic positive edge-triggered register using pass transistors is another type of sequential circuit used to store data in digital systems. This type of register is based on dynamic logic, which allows for a more compact design compared to static logic circuits.

WORKING OPERATIONS

Dynamic Positive edge trigger register circuit consist of the two section i.e. Master and Slave section.

During the the clock is 0, the transistor M1 and M4 are in ON state and transistor M2 and M3 are in the OFF state. Here the master section is the SAMPLE state and the slave section is in the HOLD state.

Similarly during the the clock is 1, the transistor M1 and M4 are in OFF state and transistor M2 and M3 are in the ON state. Here the master section is the HOLD state and the slave section is in the SAMPLE state.

1. Master Phase (Data Precharge):

- The clock signal is held at a low logic level (0), and the input data is provided to the master section of the register.

- During this phase, a precharge phase, the data is temporarily stored in a dynamic node (a capacitance element).

- The pass transistors in the master section are controlled by the complement (NOT) of the clock signal,effectively blocking any data from passing through to theslave section during this phase.

2. Slave Phase (Data Evaluation):

- The clock signal is held at a high logic level (1).

-The pass transistors in the master section are now turned off, preventing any further changes to the dynamic node.

-At the same time, the pass transistors in the slave section are enabled by the clock signal.

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- The data stored in the dynamic node during the master phase is now transferred to the slave section and latched in this phase.
- The output of the slave section now holds the data that was latched during the positive edge of the clock signal.

3. Precharge (Data Restoration):

- After the slave phase is completed, the clock signal returns to a low logic level (0), starting the next master phase.

-During this phase, the dynamic node is precharged to the initial value (typically logic high) in preparation for the next data transfer cycle.

FIGURE VII
Circuit Diagram: (dsch2)

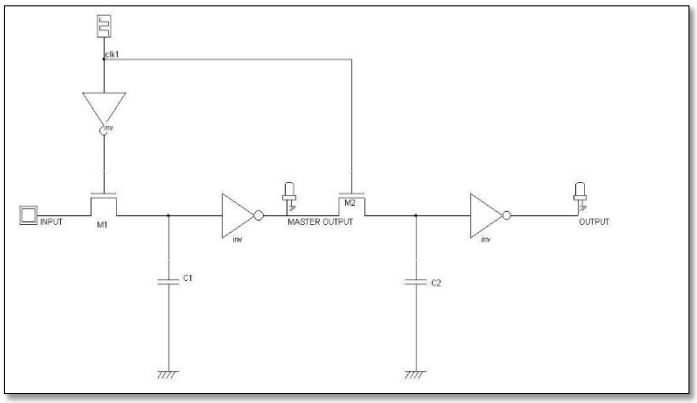

Fig: Master-Slave negative edge trigger register

TABLE V

	M1	M2
CLK=0	ON	OFF
CLK=1	OFF	ON

Tabulation: Transistor ON-OFF in dynamic positiveEdge-Triggered Register Using Pass Transistor

TABLE VI

	MASTER	SLAVE
CLK=0	SAMPLE	HOLD
CLK=1	HOLD	SAMPLE

Tabulation: Dynamic positive Edge-Triggered Register Using Pass Transistor

FIGURE VIII

Layout : (Microwind)

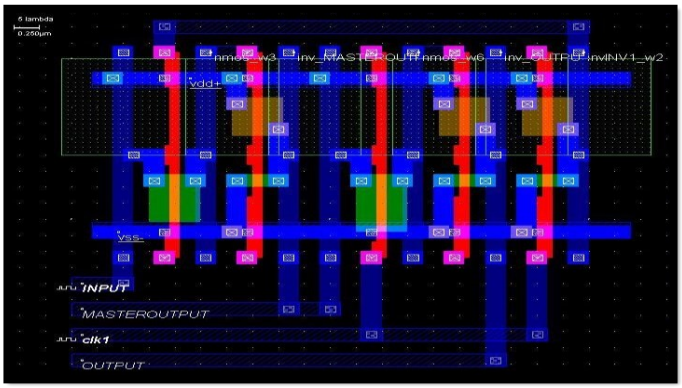

Fig. Layout for the positive edge trigger register

FIGURE IX

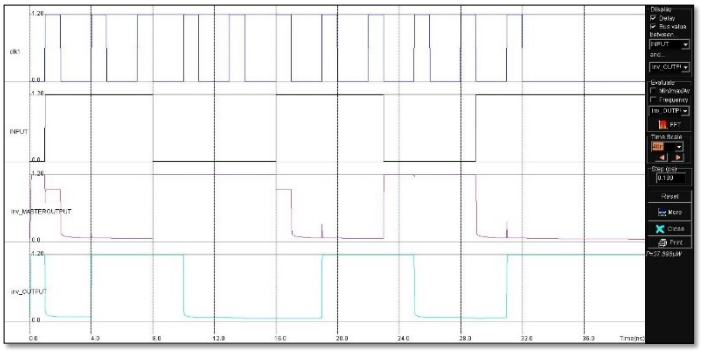

Fig. Output for dynamic positive Edge- Triggered Register Using Pass Transistor

Power Report: P=37.896 µW

VIII. DYNAMIC NEGATIVE EDGE TRIGGERED REGISTER USING PASS TRANSISTOR

A dynamic negative edge-triggered register using pass transistors is another type of sequential circuit used to store data in digital systems. This type of register is based on dynamic logic, which allows for a more compact design compared to static logic circuits.

WORKING OPERATIONS

Dynamic negative edge trigger register circuit consist of the two section i.e. Master and Slave section.

During the the clock is 0, the transistor M2 and M3 are in ON state and transistor M1 and M4 are in the OFF state. Here the master section is the HOLD state and the slave section is in the SAMPLE state.

Similarly during the the clock is 1, the transistor M2 and M3 are in OFF state and transistor M1 and M4 are in the ON state. Here the master section is the SAMPLE state and the slave section is in the HOLD state.

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1. Master Phase (Data Precharge):

- The clock signal is held at a high logic level (1), and the input data is provided to the master section of the register.
- During this phase, a precharge phase, the data is temporarily stored in a dynamic node (a capacitance element).
- The pass transistors in the master section are controlled by the complement (NOT) of the clock signal, effectively blocking any data from passing through to the slave section during this phase.

2. Slave Phase (Data Evaluation):

- The clock signal is held at a low logic level (0).
-The pass transistors in the master section are now turned off, preventing any further changes to the dynamic node.
-At the same time, the pass transistors in the slave section are enabled by the clock signal.
-The data stored in the dynamic node during the master phase is now transferred to the slave section and latched in this phase.
- The output of the slave section now holds the data that was latched during the positive edge of the clock signal.

3. Precharge (Data Restoration):

- After the slave phase is completed, the clock signal returns to a high logic level (1), starting the next master phase.
- During this phase, the dynamic node is precharged to the initial value (typically logic low) in preparation for the next data transfer cycle.

FIGURE X

circuit Diagram: (dsch2)

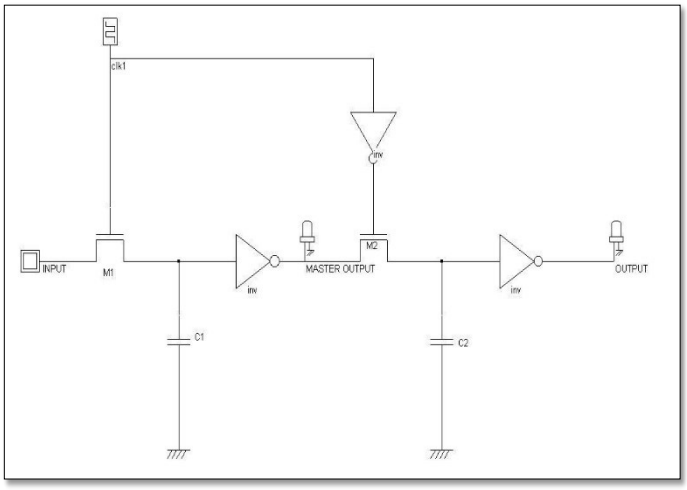

Fig. Dynamic negative Edge-Triggered Register Using Pass Transistor

TABLE VII

	M1	M2
CLK=0	OFF	ON
CLK=1	ON	OFF

Tabulation: Transistor ON-OFF in dynamic positiveEdge-Triggered Register Using Pass Transistor

TABLE VIII

	MASTER	SLAVE
CLK=0	HOLD	SAMPLE
CLK=1	SAMPLE	HOLD

Tabulation: Dynamic negative Edge TriggeredRegister Using Pass Transistor

FIGURE XI

Layout : (Microwind)

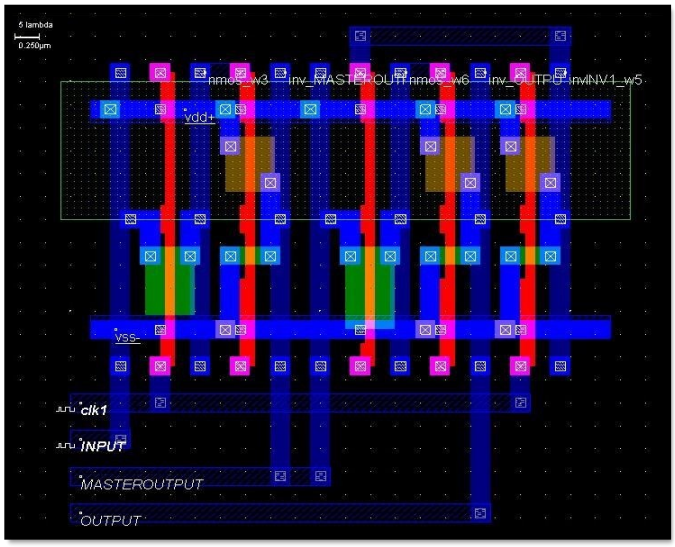

Fig. Layout for the negative edge trigger register

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FIGURE XII

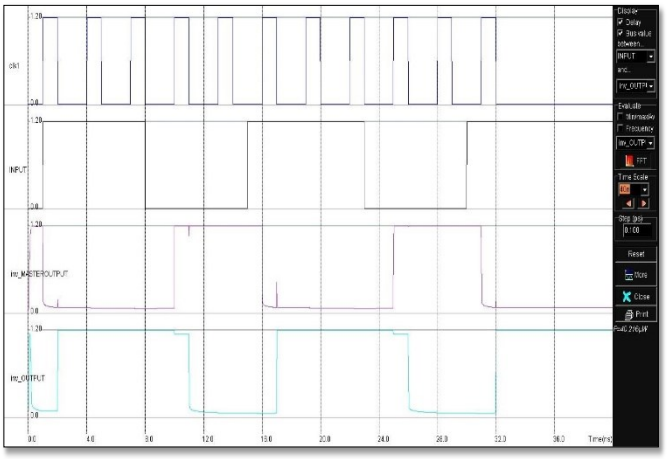

Fig: Output for dynamic negative Edge-Triggered Register Using Pass Transistor

Power Report: P=40.216 µW

XI. OBSERVATION AND RESULTS

In this paper, we designed and analyzed a master-slaveedge-triggered register using NMOS transistors as the key building blocks. Through extensive simulation and analysis, several observations were made regarding the performance and characteristics of the designed register.

TABLE IX

PARAMETERS	STATIC	DYANAMIC
Transistor Sizes	Width=0.01µm Length=0.12µm	Width=0.01µm Length=0.12µm
Clock Frequency	62.5Mhz	62.5Mhz
Area (Layout)	Positive=11x12 µm Negative=11x10 µm	Positive=11x6 µm Negative=11x6 µm
Area (Transistor Count)	16 Transistors	8 Transistors
Power	Positive=44.62 µW Negative=38.44 µW	Positive=37.87 µW Negative=40.21 µW
Propagation Delaybetween Input Signal and Output Signal	6.5 ns	6.5 ns

Tabulation: Parameters of Master-Slave EdgeTrigger Register (CMOS 90nm Technology)

TABLE X

PARAMETERS	STATIC	DYANAMIC
Transistor Sizes	Width=0.01µm Length=0.12µm	Width=0.01µm Length=0.12µm
Clock Frequency	62.5Mhz	62.5Mhz
Area (Layout)	Positive=11x12 µm Negative=11x10 µm	Positive=11x6 µm Negative=11x6 µm
Area (Transistor Count)	16 Transistors	8 Transistors
Power	Positive=44.62 µW Negative=38.44 µW	Positive=37.896 µW Negative=40.21 µW
Propagation Delaybetween Input Signal and OutputSignal	4.75 ns	4.75 ns

Tabulation: Parameters of Master-Slave EdgeTrigger Register (CMOS 65nm Technology)

TABLE XI

PARAMETERS	STATIC	DYANAMIC
Transistor Sizes	Width=0.01µm Length=0.12µm	Width=0.01µm Length=0.12µm
Clock Frequency	62.5Mhz	62.5Mhz
Area (Layout)	Positive=14x4 µm Negative=14x6 µm	Positive=6x9 µm Negative=6x9 µm
Area (Transistor Count)	16 Transistors	8 Transistors
Power	Positive=0.05 µW Negative=0.05 µW	Positive=32.115 µW Negative=40.55 µW
Propagation Delaybetween Input Signal and Output Signal	3.6 ns	3.6 ns

Tabulation: Parameters of Master-Slave Edge Trigger Register (CMOS 32nm Technology)

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TABLE XII

PARAMETERS	STATIC	DYANAMIC
Transistor Sizes	Width=0.01µm Length=0.12µm	Width=0.01µm Length=0.12µm
Clock Frequency	62.5Mhz	62.5Mhz
Area (Layout)	Positive=11x10 µm Negative=11x10 µm	Positive=15x20 µm Negative=15x20 µm
Area (Transistor Count)	16 Transistors	8 Transistors
Power	Positive=30.391 µW Negative=45.474 µW	Positive=42.487 µW Negative=34.492 µW
Propagation Delaybetween Input Signal and Output Signal	1.56 ns	1.56 ns

Tabulation: Parameters of Master-Slave EdgeTrigger Register (CMOS 18nm Technology)

X. CONCLUSION

In conclusion, the dynamic edge-triggered register using pass transistors presents a promising approach to achieve power-efficient and high-performance register designs. The theory behind pass transistor logic and its advantages over traditional flip-flop-based registers make it an attractive option for various digital circuit applications, particularly in power-sensitive environments

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