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Standard Cell Library Development

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Abstract: **A Standard Cell Library(SCL) is collection of cells that can be synthesized to a larger design, which is described with a hardware description language. We present the design of 1.8V High Density 9 track SCL in UMC180nm technology. Here we generate comprehensive library containing core number of necessary cells, providing detailed layout, schematic, symbol and abstract views, which are characterized for three process corners for timing and functional properties**.

Keywords— SCL; INVERTERS; BUFFERS;

I.INTRODUCTION:

The complexity of modern IC design and the market pressure to produce designs rapidly, has led to the extensive use of Semi custom design. Semi custom design is a methodology for making an integrated circuit in which a portion of the circuit function is predefined and unalterable, while other portions can be configured to meet the specifications. Designers can therefore design ASICs themselves, using SCL.

SCL is a collection of cells that can be synthesized to a larger design, which is described with a hardware description language. SCLs are used for a large range of applications. The use of a SCL drastically reduces the cost of designing a chip. It also reduces the time-to-market, which results in lower production cost, early sales, longer time in marked, etc. The economic and efficiency of an ASIC design depends heavily upon the choice of the library. Hence it is important to build library that full fills the design requirement.

In this work we present the development of high density SCL in UMC180nm technology. We generate a comprehensive library containing core number of necessary cells, providing detailed layout, schematic, symbol and abstract views, which are characterized for the three process corner. The electrical and physical characteristic of the SCL are provided in .LIB and LEF format respectively. The library is designed using Cadence tools. We have designed a high density SCL for the specifications as show in Table I.

Table I : Specifications

Parameters	High Density Library
Operating Frequency	50MHz
Operating Voltage	1.8V
Temperature Range	-40ºC to 125ºC
Min MOS length	0.18um
Min MOS width	0.24um

II.SYSTEM AND ARCHIETECTURE

In the present work we design a SCL which includes combinational, sequential and special cells of different drive strengths. The cell list is listed in Table II. The cells are designed for various drive strength so as to achieve maximum performance at minimum area. When the synthesizer compiles the design from a behavioral description into a collection of standard cells, often large nets are created, i.e. many gates connected to a single net. The greater the number of devices connected to a net, the greater drive strength required to sustain maximum clock speed. This also happens as the P&R tool wires in the standard cells. As a result, we need to design cells with a wide range of buffer drive strengths in the library, in order to support the synthesizer and P&R tool in the optimal buffering of large nets. Having different implementations of each cell improves the performance of the circuit that may achieve near full-custom performance designs. That happens because when the cell does not need to drive a big load, a small transistor version can be used, which leads to lower power consumption. On the other hand, for instances that need to drive a large load, a cell with larger transistors can be employed to improve performance. Therefore, an indispensable step for the design of a SCL is to define different output driving strengths.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 8 Issue 07, July-2019

CELLS	Drive strength	CELLS	Drive strength
and	X1,X2,X4	dff	X1,X2
aoi13	X1,X2	dffcz	X1,X2
aoi22	X1,X2	dffczpz	X1,X2
tristate buffer	X2	dffpz	X1,X2
buffer	X1,X2,X4,X8,X16	ndff	X1,X2
clkbuf	X2,X4,X7	ndffcz	X1,X2
clkinv	X2,X4,X7	ndffczpz	X1,X2
full_adder	X1,X2	ndffpz	X1,X2
half_adder	X1,X2	nsdff	X1,X2
tristate inverter	X2	nsdffcz	X1,X2
inv	X1,X2,X4,X8,X16	nsdffczpz	X1,X2
mux2	X1,X2,X4	nsdffpZ	X1,X2
nand2	X1,X2,X4	sdff	X1,X2
nor2	X1,X2,X4	sdffcz	X1,X2
oai13	X1,X2	sdffczpz	X1,X2
oai22	X1,X2	sdffpz	X1,X2
or2	X1,X2,X4	delay_1n	X4
xor2	X1,X2,X4	delay_2n	X4
cgn	X2,X4	delay_5n	X4
cgnt	X2,X4	filler	X1,X2,X4,X5
cgp	X2,X4	filler_decap	X3,X5,X8
cgpt	X2,X4	line_holder	X1
lath	X1,X2	tieoff	X1
latl	X1,X2		

The typical design flow of a SCL consists in designing a set of logical gates at the transistor level for a given technology process. Fig.1 shows an Overview of the steps required to design SCL and the tools used for the same. The design starts from a specification, defining logical and electrical parameters like propagation delay and power consumption. From these, the Schematic is designed to meet the required specifications. Then the layout is drawn for each of the cells designed. Once the layout is DRC and LVS clean, the extracted circuit is obtained through an automated extraction tool. This circuit contains not only the drawn transistors but also every parasitic generated from the physical layers. In this way, a more realistic view is obtained, and with it, simulations are performed to characterize the electrical behavior of the designed gate. The output of the characterization is store in .LIB format that can be used by the synthesizer. After the characterization if the required specification are not met then the layout is altered and again re-characterized. With this electrical characteristic of each gate, a circuit can be synthesized from a high level description. Once the cells are characterized an abstract view of the layout is generated by the abstract generator. With the abstract views the P&R tool can easily assemble the IC from these predesigned blocks. The physical characteristics of the cells are in the .LEF file.

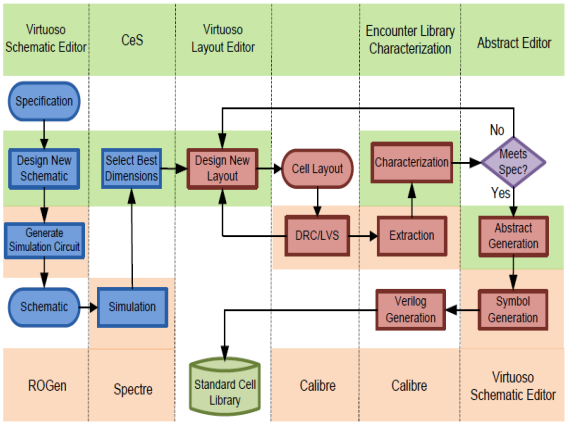

Fig.1 Design Flow of a Standard Cell Library and the Tools used.

III. ELECTRICAL AND PHYSICAL METHODOLOGY

A . Schematic design:

The design of the SCL begins with the sizing of the transistor so as to meet certain constraints. The constraint that has to be taken care while designing the combinational cells is that the average delay of the cell should be minimum. So, we set the beta ratio and stage ratio for the entire library such that the average delay is minimum for each cell. Once we fix the beta and the stage ratio the design of combinational cells is done. The constraint that has to be taken care while designing the sequential cells is that the timing of setup0 and setup1 should be same. And in clock inverter and clock buffer we should see that the rise delay and the fall delay are equal.

1. Beta Ratio Calculation:

Beta ratio is the ratio of PMOS width (Wp) to NMOS width (Wn) in the CMOS process. To calculate the beta we simulate the cell for all the possible values of the MOS widths in the real time scenario and tabulate the rise and fall delay. The real time scenario which we have used is FO3 chain. FO3 chain is arrangement of cells as shown in Fig.2. We calculate the delay at the middle of the chain. The significance of using the FO3 chain is that it eliminates the effect of the input slew after 4 to 5 stages. So the rise delay and fall delay are calculated at the 5^{Th} stage of the chain.

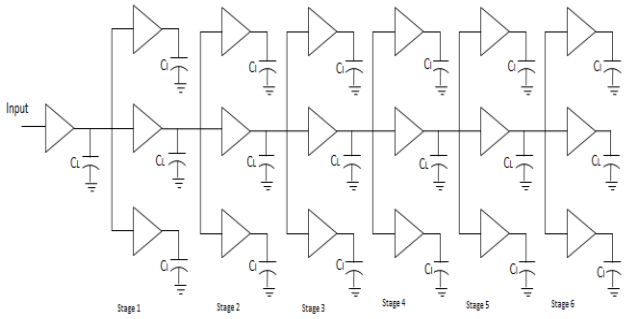

Fig.2: FO3 Chain of the INV

The Beta ratio is fixed for the library. The perl code is written to create the FO3 deck of the cell. The deck sweeps the value of the MOS widths and measures the rise delay and fall delay for each value of the MOS width. Then we calculate the average delay for all the values of the MOS width. The ratio of Wp to Wn at which the average delay is minimum is defined as the beta ratio for that cell. In order to obtain a more reliable Beta ratio for the entire library we consider the following cells: INV, NOR and NAND of different drive strengths. NAND and NOR cells are converted as an inverter and placed in the FO3 chain. Each of the cells will have different beta at which the performance loss is zero for that particular cell. Once the beta ratios of all the cells are calculated we tradeoff between the performances of the different cells to decide a single beta ratio for the library. The different beta ratio and the corresponding performance loss for different cells are as shown in the Table III. We should set the beta in such a way that the performance lose of all the cell must be feasible.

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Vol. 8 Issue 07, July-2019

TABLE III : Comparison of Performance loss for different Beta ratios of different

Cell/beta value	INV	Nand2	Nor2	Nor3
At 1.40	0%	5%	2%	6%
At 1.50	0%	2%	2%	4%
At 1.60	1%	3%	1%	3%
At 1.70	1%	4%	1%	3%
At 1.80	1%	6%	0%	2%

2. Stage ratio calculation:

In certain combinational cells like buffer there are 2 stages. In this the output stage should have the strength to drive the output load. But for the input stage it is sufficient if it has the strength to drive only the output stage and thus it can be sized smaller then the output stage. Doing this would reduce the power. Likewise if there are more number of stages, the transistors in the output stage are set as per the beta value and the previous stage transistors are sized only to drive the next stage. The ratio of the Wp of the output to the Wp of the previous stage is called the stage ratio. The stage ratio is also fixed for the library. Stage ratio calculation steps are same as that of the beta ratio calculation; the only change is the transistor whose value has to be varied. For stage ratio calculation we consider the following cells: BUFFER, AND and OR of different drive strengths. The MOS widths of the output stage are kept as per the beta set for the library and vary the MOS widths of the input stage. Stage ratio is set at which the performance loss is less and power gain is maximum. Comparison of performance loss and power gain for different stage ratios of different cells is as shown in the Table IV.

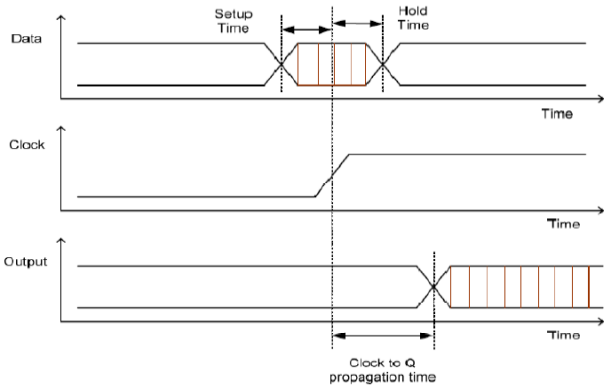
TABLE IV : Comparison of Performance loss and Power Gain for different Stage ratios of different cells.

Cell/Stage ratio	AND1 (PER Loss and power gain)		OR1 (PER Loss and power gain)		BUFFER1 (PER Loss and power gain)		AND2 (PER Loss and power gain)		OR2 (PER Loss and power gain)	
At 1.40	0	0	0.56	3.15	0.08	-1.82	0.01	0.16	0.42	2.31
At 1.60	0.46	2.29	1.89	7.73	0.2	1.55	0.93	6.09	1.38	5.7
At 1.80	1.44	5.12	3.41	10.21	0.9	4.1	2.09	9.08	3.71	9.81

3. Sequential cells:

In sequential circuit design the constraint on setup time and hold time is determined by delay tolerance-based binary search method that is the setup time should also be such that it does not degrade the Clock-Q propagation time beyond a pre-determined tolerance value. In library characterization, to ensure that set up time chosen is not so close to the switching point that the simulation fails, it performs a delay tolerance check by multiplying the delay from clock to the output Q by factor specified. As soon as the CK-Q delay is more than delay tolerance variable, the simulation is considered as fail. The setup time is the time during which the input data to the input of the sequential logic must remain stable prior to the arrival of the clock so that the correct value is latched at the output. Hold time is defined as the minimum time that an input signal must remain stable after the active clock signal to ensure that input value is correctly latched at the output.

Fig.3 Setup and Hold time constraints for a positive edge triggered flip-flop.

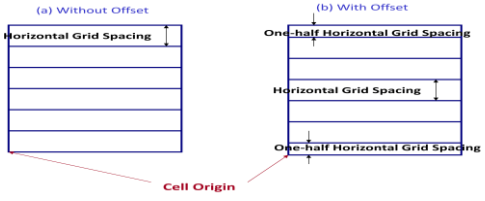


4 . Clock inverter and Buffers:

The clock signal is another very large net that regularly requires very high drive currents. These nets are broken down into simpler nets and designed as a tree. But, there are skew problems which are frequently made worse just by adding buffers. Skew is the time difference between the clock signals arriving at different clocked elements in a chip. The Place and Route tool automatically designs a balanced clock tree, and then adjusts the buffers depending on the load a particular clock net sees to partially compensate the skew differences. For this effort the library needs specific cells referred to as the clock buffers. Clock buffers have high drive strength and near equal rise and fall time.

B. Layout Architecture :

In layout architecture we first define the routing grids. Routing grids are used by CAD tools to route wires over the standard cells placed in the design. The PNR tools use these routing grids as a reference to place the cells. The grids are defined with respect to the cell origin. These grids can be offset from the origin however by exactly half the grid spacing as shown in Fig.4. The intersection of horizontal and vertical grids is called hit point. And the pins within the cell except for abutment type of pins i.e., power rail should be placed on the hit point. So that the P&R tool can easily have access to the pins. Using grid offset can increase the number of hit points as shown in Fig.5. The cell height must be a multiple of horizontal grid spacing and cell width is multiple of vertical grid spacing. Grid spacing must be defined for each routing layer. Grid spacing needs to be at least line-on-via, and are usually via-on-via.



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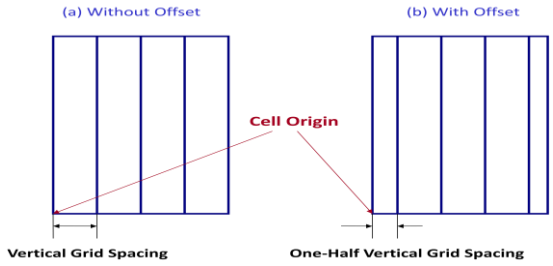


Fig.4: Vertical and Horizontal grids with and without Offset

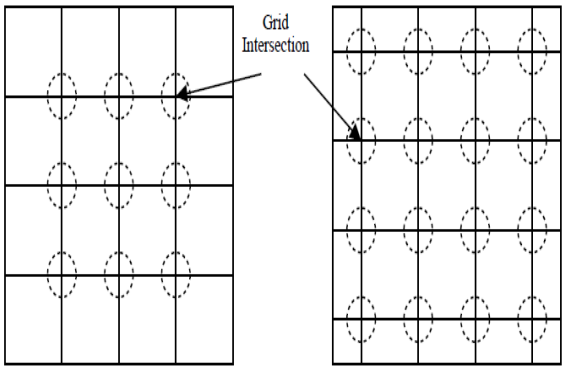


Fig.5: How Grid Offset Increases number of hit points.

There are three types of pitch at shown in Fig.6. We calculate the pitch for all the 3 types of pitch, with different orientations of via and then decide on the final pitch considering the pitch value, number of VIAs we can place and the height of the cell. Pitch calculation for different orientation are tabulated as shown in TABLE V.

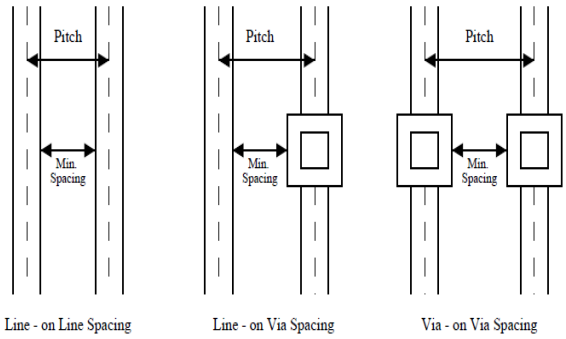
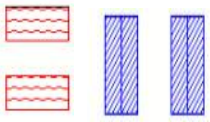
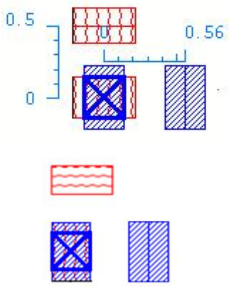
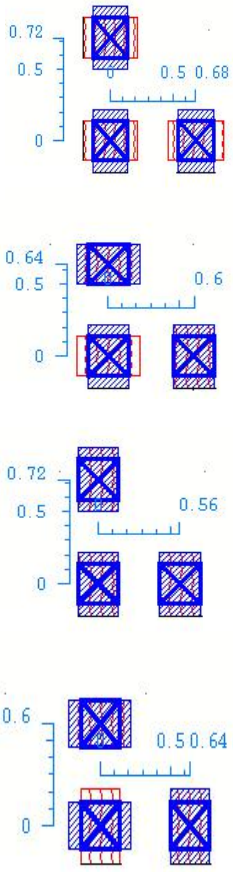


Fig.6: Types of Pitch

From the above table we can see that if we choose x-pitch =0.6 and y-pitch= 0.6 we can have more number of VIAs. Track is approximately the minimum spacing i.e., the pitch in the technology node. Track is generally used as a unit to define the height of the standard cell. A 12 track cell will be taller than a 9 track cell. A 12 track standard cell will be taller means more metal1 routing space is available within the cell, hence cells will be faster. Where as in a 9 track cell the cell will be compact but speed is less compared to 12 track. Once we decide the pitch and routing grids, the cell height is fixed with the following equation.

Cell height = Number of track * y-pitch
= 9*0.6 = 5.4

TABLE V : Pitch Calculation for different Orientation

Pitch	Orientation	X-Pitch	Y-Pitch
Line to Line		0.58	0.48
Line to VIA		0.56 0.56	0.50 0.58
VIA to VIA		0.68 0.60 0.56 0.64	0.72 0.64 0.72 0.60

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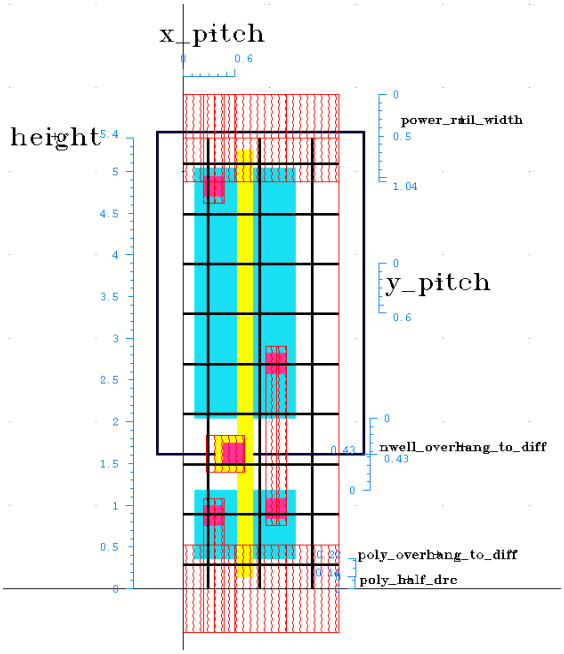

Fig.7: Layout Architecture

Then we calculate the power rail width. Once the layout architecture is decided we draw the layout for all the cells. And verifications are performed to ensure that each cell in the library passes Design Rule Check (DRC) and Layout Versus Schematic (LVS) checks. When the layouts are DRC and LVS clean a circuit extractor tool must be used to scan the different layers of the physical design and extract the parasitic elements in this geometrical description. The generated circuit contains not only the transistors that implement the logic of the gate, but also every parasitic element, like the capacitance between the gate and the bulk. This allows a more accurate simulation and analysis of the designed circuit.

IV.SYSTEM LEVEL DESIGN VALIDATION

A. Characterization:

Upon completion of the physical implementation, cell characterization is performed to generate timing models of the library that are used for synthesizing behavior codes of a design and also the timing optimization during the P&R step. Once the results of library characterization are obtained, it is verified whether the required specifications are met. If not changes are made in the layout and again the library is characterized. To obtain realistic manufacturing process characteristics, circuit simulation is performed for the three process corners at shown in TABLE VI for the range of input slew and output load capacitance. The characterization is done using an automatic cell characterization tool. After characterizing, the cells functional description and timing data are transformed to a standard industry file format, Synopsys Liberty format (or *.lib file). This data is used by other design tools like synthesizer and the P&R tool. The final requirement is a documentation that summaries the functionality and timing of each cell. The functionality is frequently described with truth table, and timing data is presented in a simple format in the datasheet.

TABLE VI : Voltage and Temperature for different Process corners

Process	TT	SS	FF
Voltage (volts)	1.8	1.62	1.98
Temperature(^{o}C)	25	125	-40

B . Conceptual

Along with the timing library, the P&R tool also requires a physical description of the library that includes definitions of blockages, information regarding routing layers, pin information and to avoid the generation of shorts among the cells when routing the cell interconnection. Once a cell is fully verified, an abstract view can be generated. Cadence Abstract generator is used to generate the physical description i.e., the abstract view and the Layout Exchange Format (LEF) file for all the cells. These are required for placing and routing of the final chip by the P&R tool.

V. RESULT

The work described in this document has produced a 1.8V Digital Standard Cell Library for UMC180nm CMOS process, operating at -40^{o}C to 125^{o}C temperature. In total this library has 104 cells which include logical cells, sequential cells and special cells which are listed in Table I. Each cell has the following views: schematic, symbol, layout and abstract. Results of AND2_x1 cell is as shown in figures below. For each standard cell, physical characteristics are given in a LEF file, which is used in the automation of the design of standard cell based ICs and is widely accepted among CAD tools. Each standard cell has its electrical characterization for three different process corners [TABLE VI], for a range of input slew and output load. This information is given in a LIB format as shown in Fig.9, which is used by synthesis tools to generate the net list of circuits. Fig.10 shows the rise delay, fall delay, rise transition and fall transition for different output capacitance and slew.

TABLE VII : Layout Architecture values

Parameters	Values
X-pitch	0.6 um
Y-pitch	0.6 um
Number of tracks	9
Cell Height	5.4um
Power rail width	1.04um

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Vol. 8 Issue 07, July-2019

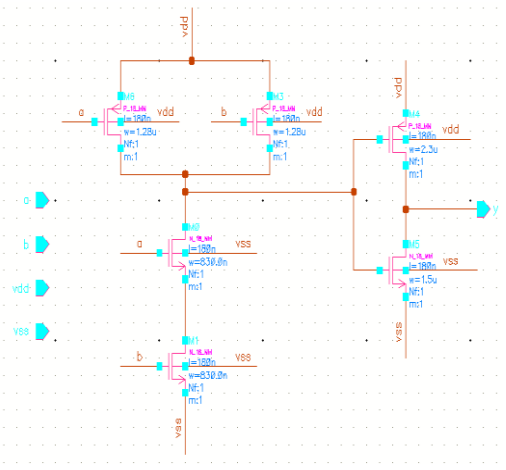

Fig.8 Schematic of AND2_x1

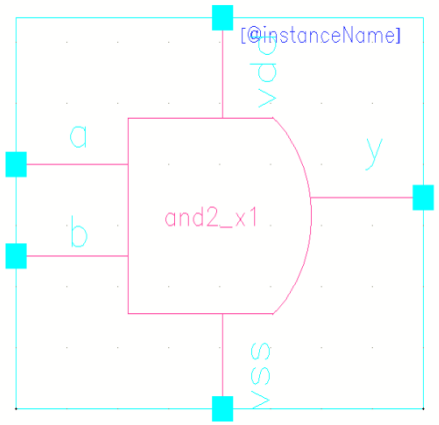

Fig.9 Symbol of AND2_x1

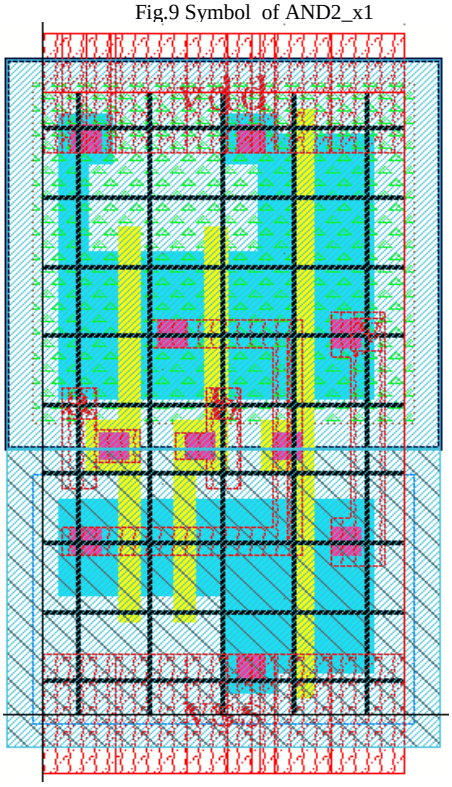

Fig.10 Layout of AND2_x1

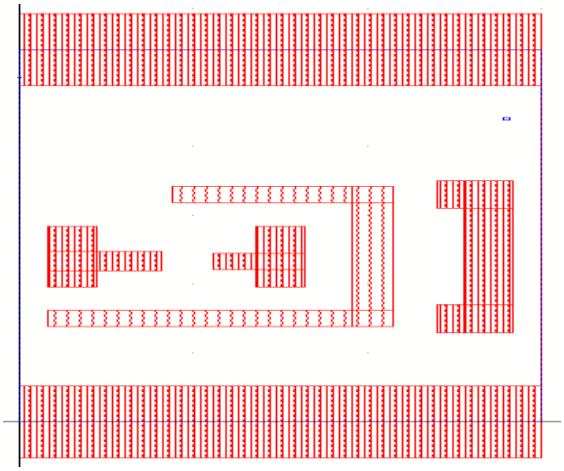

Fig.11 Abstract view of AND2_x1

Function

Pin Name	Function
y	a * b

Footprint:

Cell	Area
and2_x1	16.2000

Leakage

Leakage(nW)			
Cell	Min	Avg	Max
and2_x1	0.0264	0.0394	0.0484

Pin Capacitance

	Pin Cap(pf)		Max Cap(pf)
Cell	a	b	y
and2_x1	0.0043	0.0043	0.8000

Delay

Delays(ns) to y rising:

		Delay(ns)		
Cell	Timing Arc(Dir)	min	mid	max
and2_x1	a->y(RR)	0.0633	0.8205	1.5320
and2_x1	b->y(RR)	0.0695	0.8146	1.5184

Delays(ns) to y falling:

		Delay(ns)		
Cell	Timing Arc(Dir)	min	mid	max
and2_x1	a->y(FF)	0.0599	0.5803	1.0502
and2_x1	b->y(FF)	0.0707	0.6013	1.0800

Power

Internal switching power(pJ) to y rising:
Conditional

		Power(pJ)			
Cell	Input	min	mid	max	when
and2_x1	a	0.0296	1.3344	2.6447	b
and2_x1	b	0.0297	1.3325	2.6424	a

Internal switching power(pJ) to y falling:
Conditional

		Power(pJ)			
Cell	Input	min	mid	max	when
and2_x1	a	0.0401	0.0507	0.0657	b
and2_x1	b	0.0489	0.0587	0.0740	a

Fig.12 Datasheet of AND2_X1

International Journal of Engineering Research & Technology (IJERT)
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Rise delay:

Cap(pf)/slew	0.25	0.5	0.75	1.25	1.5
0.015	0.135287	0.214656	0.438663	0.774046	1.4445
0.05	0.148039	0.227189	0.451033	0.786271	1.45671
0.15	0.152874	0.233102	0.456401	0.791816	1.46246
0.3	0.150598	0.233973	0.458726	0.793753	1.46402
0.6	0.145957	0.231001	0.457122	0.792305	1.46275

Rise transition:

Cap(pf)/slew	0.25	0.5	0.75	1.25	1.5
0.015	0.0720135	0.182756	0.509556	1.00165	1.98594
0.05	0.0761426	0.184095	0.510367	1.00183	1.98574
0.15	0.0808604	0.186551	0.511102	1.00241	1.98581
0.3	.089543	0.193583	0.514194	1.00362	1.98654
0.6	0.093464	0.197233	0.516733	1.00488	1.9867

Fall delay:

Cap(pf)/slew	0.25	0.5	0.75	1.25	1.5
0.015	0.15489	0.202907	0.322662	0.500069	0.854708
0.05	0.204204	0.254525	0.375571	0.553101	0.907642
0.15	0.246207	0.299117	0.421367	0.599197	0.953725
0.3	0.318831	0.376994	0.503978	0.682469	1.03756
0.6	0.351752	0.41227	0.542038	0.721796	1.07679

Fall transition:

Cap(pf)/slew	0.25	0.5	0.75	1.25	1.5
0.015	0.0456471	0.0945102	0.243999	0.476497	0.943165
0.05	0.051692	0.0990183	0.246196	0.47715	0.943389
0.15	0.0576369	0.104007	0.248249	0.47815	0.943733
0.3	0.068494	0.114954	0.255109	0.481403	0.944711
0.6	0.073389	0.120181	0.259683	0.483908	0.945788

Fig.13. Rise delay, fall delay, rise transition and fall transition for different values of output capacitance and slew

VI . REFERENCE

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