

SRAM Memory Layout Design in 180nm Technology

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Abstract—This paper presents a full custom memory layout design of 1KB SRAM, followed by physical verification checks, such as DRC and LVS to validate the layouts implemented. The Layout design technique such as device matching, routing matching, half-cell and symmetry has been followed carefully. The layouts were implemented using CADENCE EDA, Virtuoso platform was used for schematic and layout design. Assura physical verification environment was used for validating the layout designs. Technology nodes used are gpdk 180nm and 45nm. The full custom layout of 1KB SRAM architecture was successfully designed.

Keywords—SRAM, 6T Bit cell, Core array, Sense amp, Row dec, leaf cells, tap cell, latchup, antenna, device matching, DRC, LVS.

I. INTRODUCTION

The name Static Random Access Memory is because it can hold the data statically as long as it is powered. Static Random Access Memories (SRAM) are the type of memories which store single bit of data (logic 1 or logic 0) using multiple transistors (Ex: 4T, 6T, 7T, 8T, 9T, 10T). The most commonly used type of SRAM is 6T (Six Transistor). SRAM's are usually placed as cache memories of the processors such as level 1 cache and level 2 cache memories, which operate in synchronous with a processor at high speed [6].

II. ARCHITECTURE OF 1KB SRAM MEMORY ARRAY.

Figure1 shows the typical SRAM Butterfly architecture. The Butterfly architecture is the type of SRAM memory architecture in which memory core array is distributed on LHS and RHS of the Row Decoder. So that the loading on the word lines reduces by 50% as compared to the single ended. Also the RC Delay of WL Signal reaching the corner bit-cells will be reduced by 50% [].

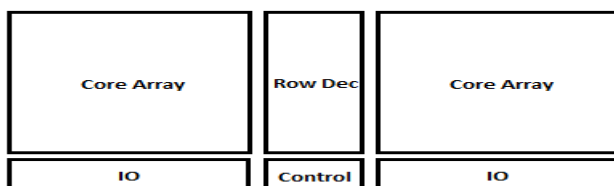


Figure 1: SRAM Butterfly Architecture

The following section explains 1KB SRAM Memory array Layout design in 180nm technology, using good layout design techniques.

A. 6T Bit Cell

6T Bit-cell is a commonly used industrial standard bit cell in SRAM cache memory design. In order to thoroughly understand the layout design of 6T Bit-cell, it is recommended to know the read and write operations of the 6T Bit-cell. With prior understanding of read write operations, one can decide the widths of the 6 transistors in the 6T Bit-cell and can design a smallest bit cell unit, which contributes for the total SRAM memory area on the chip. Figure 2 shows the 6T Bit-cell and Figure 3 is the respective Layout of the 6T Bit cell.

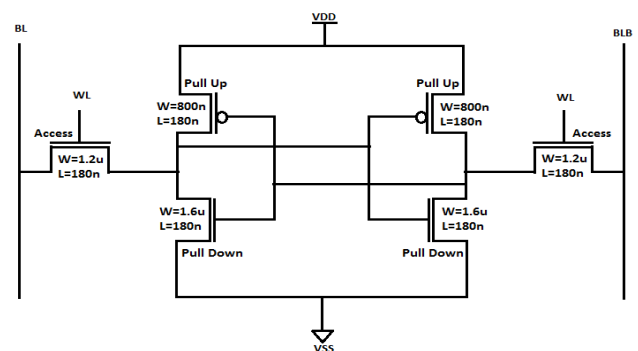


Figure 2: 6T Bit Cell

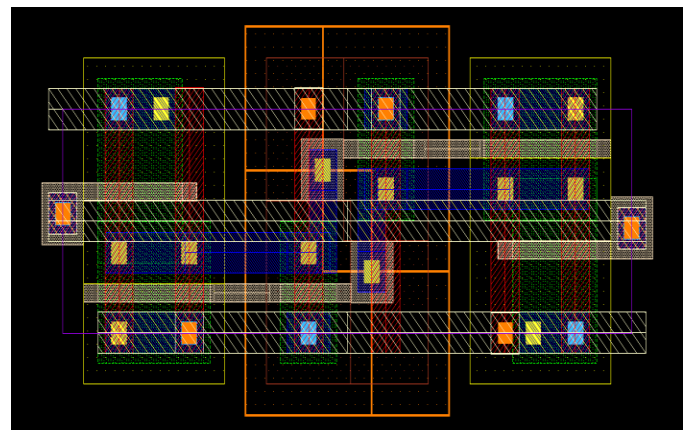


Figure 3: Layout of 6T Bit Cell

B. Tap Cell

Tap cell is the body/bulk connection for the bit cell in the core array, one of the primary reasons for using the tap cell is to avoid latch up and other reason is to reverse bias the body and active regions of both NMOS and PMOS transistors respectively. Figure 4 shows the Tap cell layout in 180nm. Since SRAM memories are capable of storing large number of bits starting from 1KB or more, the hierarchy of leaf cell such as 2x2, 4x2, 32x16 etc., along with one tap cell.

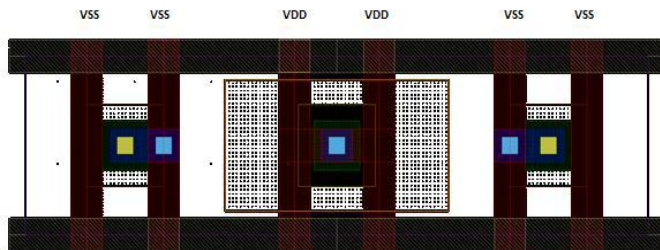


Figure 4: Tap Cell

C. 4x2 leaf cell with Tap cell

The base leaf cell 4x2 plus tap cell is used for designing the core array. Since the capacity of the SRAM Layout designed is 1KB, we need Sixty-four 4x2 leaf cells arranged horizontally and sixteen 4x2 leaf cells arranged vertically to make a total core array of one 64x128 leaf cell capable of storing 1024 bits, Figure 5 shows the 4x2 leaf cell plus tap cell layout.

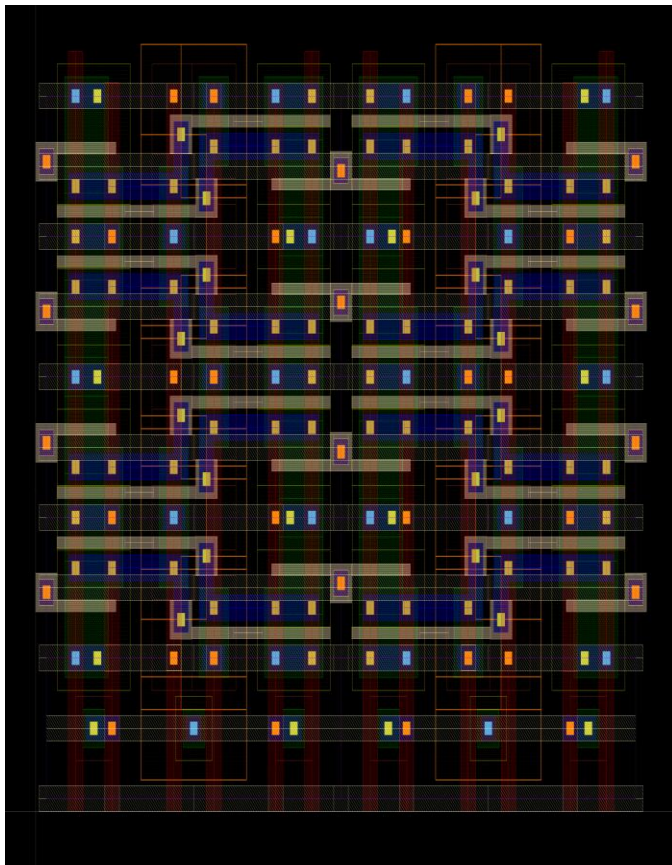


Figure 5: 4x2 leaf Cell plus Tap cell

D. Pre –Chage Circuit

Basically pre charge circuit shorts the Bit line and Bit line bar using one PMOS transistor at the centre and two remaining PMOS transistors equalizes both the bit lines to VDD. Figure 6 shows the PMOS Pre-charge circuit

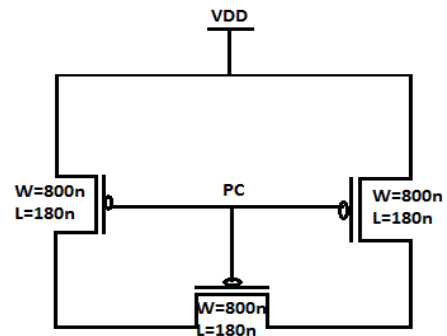


Figure 6: Pre Charge Circuit

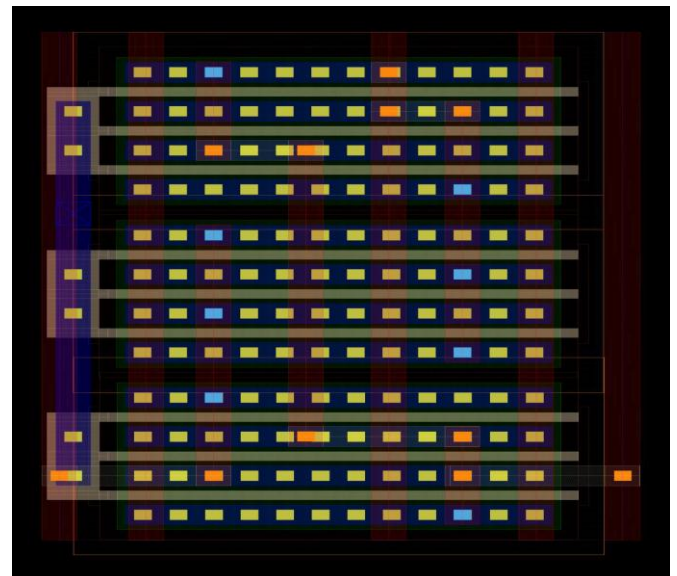


Figure 7: Pre-Charge Circuit layout

Figure 7 show the pre charge circuit Layout in 180nm technology

E. Sense Amplifier

Sense amplifier is the most important block in the SRAM memory IO block, which senses the data from the core array. Sense amplifier layout needs to be matched using layout technique such as common centroid. Latch based CMOS circuit sense amplifier is used as sense amplifier whose pull down transistors are critically matched which helps in quality sense / read of the SRAM core array, Figure 8 shows typical sense amplifier Layout with device matching for pull down transistors.

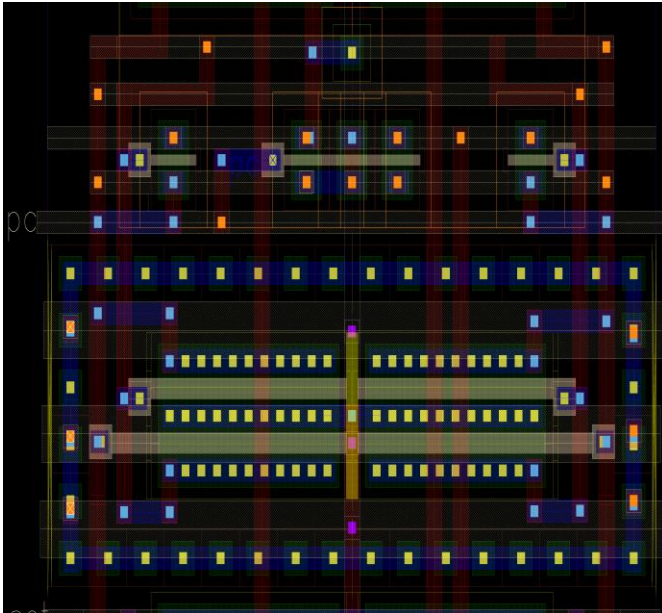


Figure 8: Sense Amplifier Layout

III. PHYSICAL VERIFICATION OF BIT CELL

Physical Verification is the methodology to validate the Layout drawn before passing the layout to the Place and Route (PNR) tool in the Physical Design Domain of the ASIC flow, Figure 9 and Figure 10 shows the DRC and the Layout Versus Schematic (LVS) physical verification schemes of the IC Layout design.

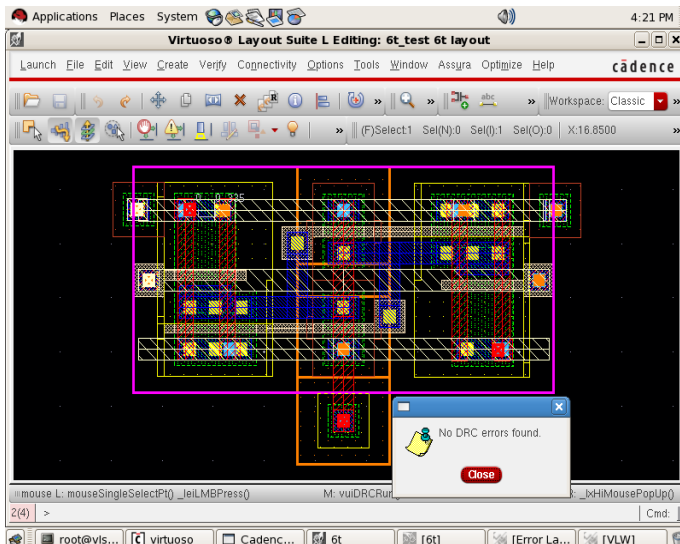


Figure 9: 6T Bit cell DRC Clean

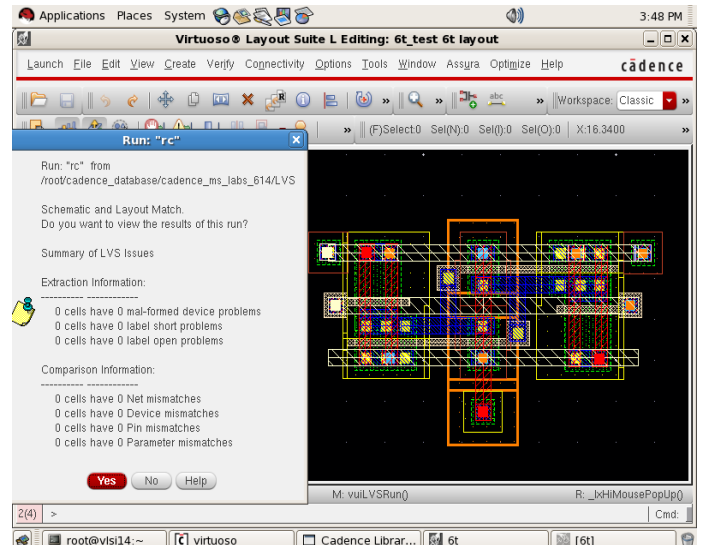


Figure 10: 6T Bit cell LVS Clean

IV RESULTS

Figure 11 shows the typical bit cell area (*width x length*), which decides the total area of the 64 x128 core array, which is calculated as:

$$\begin{aligned}\text{Bit Cell Area in 180nm} &= \text{Width} \times \text{Height} \\ &= 7.2 \times 2.3 \\ &= 16.56\mu\text{m}\end{aligned}$$

Tap Cell Placement by DRC = $10\mu\text{m}$

Leaf Cell Height = $2.3 \times 4 = 9.2\mu\text{m}$

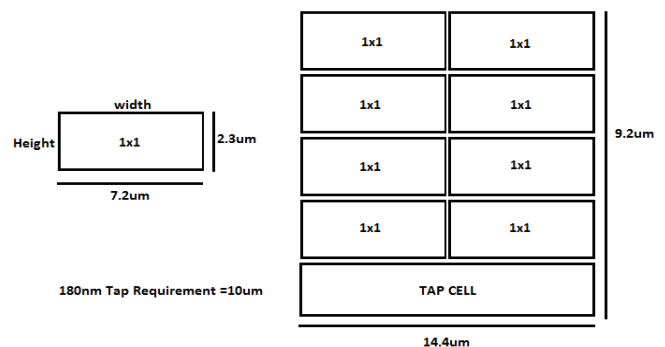


Figure 11: Area of 6T bit cell in 180nm and Tap cell Requirement

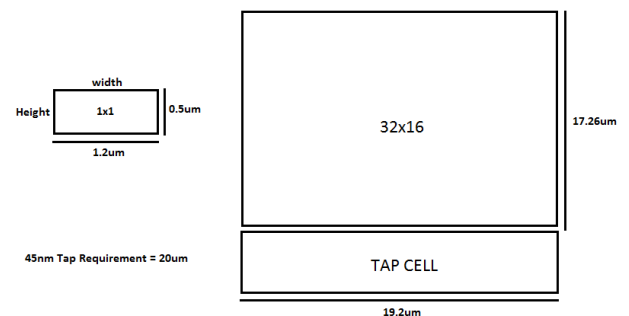


Figure 12: Area of 6T bit-cell in 180nm and Tap cell Requirement

From Figure 11 and Figure 12, we can conclude that the Moore's law defined by Gordon Moore, proved to be at a great extent moving from 180nm technology to 45nm technology, the aim of this paper was to show the bit cell layout design technique, with tap cell requirement and to compare between 180nm and 45nm technology nodes, proving Moore's law.

Figure 13 shows the implementation of typical top level layout of 64 x128 SRAM in 180nm technology

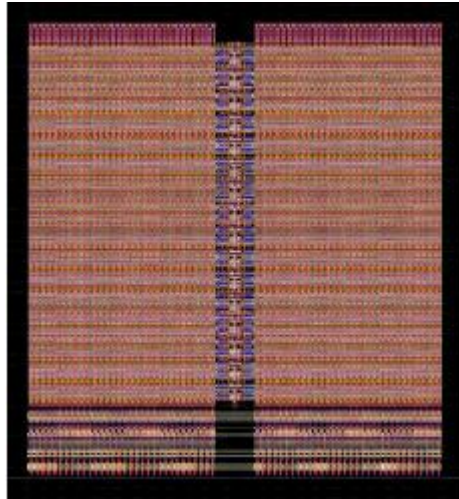


Figure 13: 64 x 128 SRAM Top Level Layouts

Layout design of 1KB SRAM Array is shown in Figure 14, is implemented in 45nm technology node. The leaf cell is of 32 x 16 to implement a core array of 64x128 meeting TAP cell requirements, in 45nm technology, figure 12 shows the 6T Bit cell Layout in 45nm technology

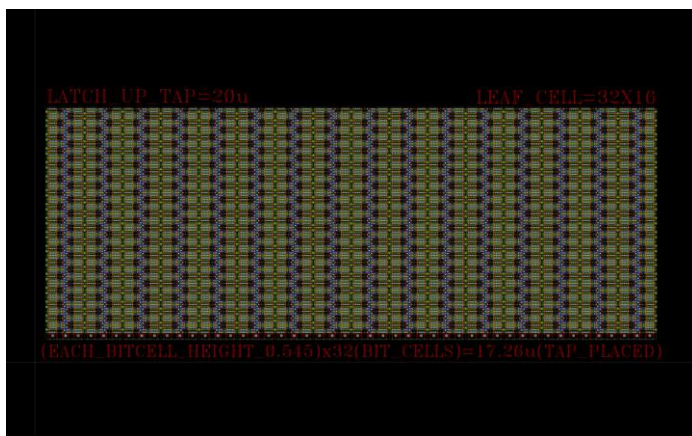


Figure 14: 16 x 32 leaves Cell Layout in 45nm technology node

The tap cell requirement in 45nm technology node was 10um which half the tap cell requirement in 180nm technology, and this proves the Moore's law of number transistors increases or doubles for every 18 months, figure 13 shows the 6T Bit cell layout in 45nm technology

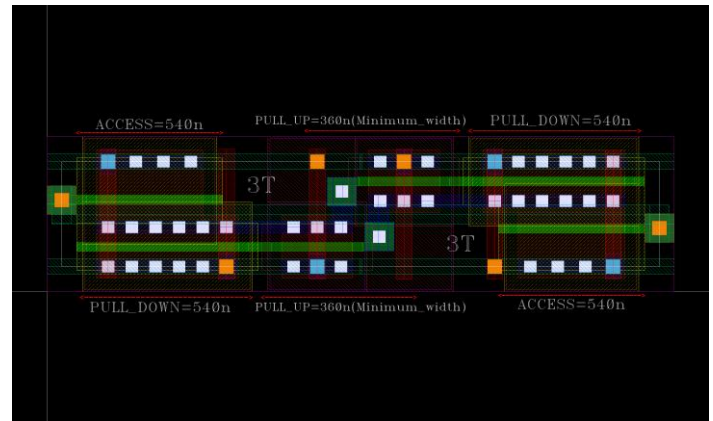


Figure 13: 6T SRAM Bit cell in 45nm technology node

Figure 14 below shows the typical TAP Cell layout, which will be placed in the core array to meet latch up and body effect requirements

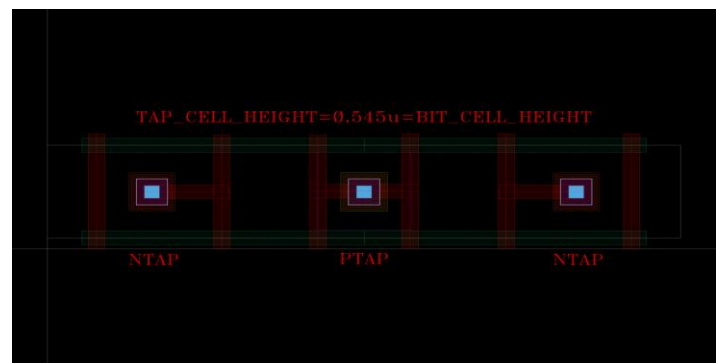


Figure 14: TAP Cell in 45nm Technology node

CONCLUSION

With pre-designed Schematics, the Layout Design of 1KB SRAM Memory Array was implemented successfully in CADENCE platform, using generic process design kit (gpd) 180nm as fabrication technology. The physical verification (DRC and LVS) of all the layouts drawn is done and fixed all violations. The 6T Bit cell layout was designed with minimum and without any DRC violations. Bit cell area played very important role in deciding total SARM Core array area and SRAM memory density. 4X2 leaf cell height was fixed meeting the TAP Requirements of the gpd 180nm DRM file. Finally the tap requirements in 180nm and 45nm showed that, as the technology shrinks more number of transistors can be accommodated in the smaller area.

ACKNOWLEDGEMENT

It is pleasure to thank Dr. B. G. Shivaleelavathi, Professor and HOD for the Department of Electronics and Communication Engineering, JSSATE for her kind support and guidance. Special thanks to my external guide Mr Ravi Siddhanath, Sr. Design Engineer, Avago Technologies, Bangalore

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