SRAM Design in Nanotechnology using CNTFET

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Abstract—**Carbon Nano Tube Field Effect Transistors (CNTFETs) are customarily examined as conceivable successors to silicon MOSFETs. The threshold voltage of CNTFET can be balanced by adjusting chilarity vector . Along these lines Design of SRAM Cell in light of CNTFET is critical for Low-control store memory. In this paper we have effectively built up a conservative model for MOSFET like CNTFET. This paper starts with the examination of the CNTFET. The Static Random Access Memory (SRAM) was made by utilizing the HSPICE programming. The circuit execution of SRAM will be acquired through HSPICE and the execution of circuit will be broke down in view of the waveform created in CosmosScope.**

*Keywords***:-SRAM, MOSFET, CNTFET, graphene, HSPICE.**

I. INTRODUCTION

For a long time, SRAM(Static Random Access Memory) architects have been utilizing metal-oxide semiconductor field-impact transistors (MOSFETs) as fundamental circuit components. The power utilization has turned into a critical thought on the VLSI framework plan and microchip as the interest for the versatile gadgets and implanted frameworks persistently expands .The on-chip reserves can decrease the speed crevice between the processor and the primary memory. These on-chip reserves are normally executed utilizing SRAM cells. The compose force of SRAM is typically bigger than the perused control because of huge power scattering in driving the phone bit lines to full swing. Numerous procedures have been proposed to diminish the compose control utilization by lessening the voltage swing level on the bit lines. Particularly for cutting edge VLSI processor plan, SRAM takes extensive piece of force utilization segment and area overhead. These fundamentals can be accomplished by lessening the measure of transistor, by a procedure known as scaling. The constant scaling of the circuit configuration offers ascend to issues like; short channel impact, control dissemination, spillage current and process variety. As an answer for right these weaknesses and accomplish comparable execution; the CNTFET is investigated. Static Random Access Memories (SRAMs), being a pivotal segment in the memory pecking order of current registering frameworks, should be quick open with low power utilization. In such manner SRAM Cell configuration utilizing CNTFET demonstrates valuable as CNTFET require less limit voltage. SRAM cell exhibitions are normally measured as far as static commotion edge and compose time. Executions of SRAM cell with various chirality [vector (n ,m)] for n-and p-CNTFET are made. CNT is made with a sheet of graphene rolled up into a cylindrical structure. The CNT can fill in as metal or semiconductor, in

light of how the sheet is rolled up. The graphene rolling is communicated by move vectors (n,m) values known as chirality vector. The CNT based FETs can accomplish the execution like customary MOSFET. CNTFET appears to be more doable in view of its CMOS-like structure. In this venture, we proposed an outline of CNTFET–based SRAM and contrasted it and the current MOSFET based SRAM.

II.CARBON NANO TUBE (CNT)

The mission to locate another option to mosfet innovation has prodded a lot of research into non-mosfet materials and circuit structures. Among the numerous gadgets, the great electrical properties of the carbon nanotube has made it a conceivable contender since its revelation in the mid 1990s . Tans et al. designed carbon nanotubes to carry on as a channel where the development of the lion's share bearers could be controlled by an electric field offering ascend to the carbon nanotube field impact transistors (CNTFETs).CNTs are graphene, which is a two-dimensional honeycomb cross section of carbon molecules, sheets moved up into cylinders.They demonstrate either metallic or semiconducting properties relying upon the course how CNT are moved up. Since the band hole of semiconducting CNTs is contrarily corresponding to their breadths, edge voltage can be effectively controlled.
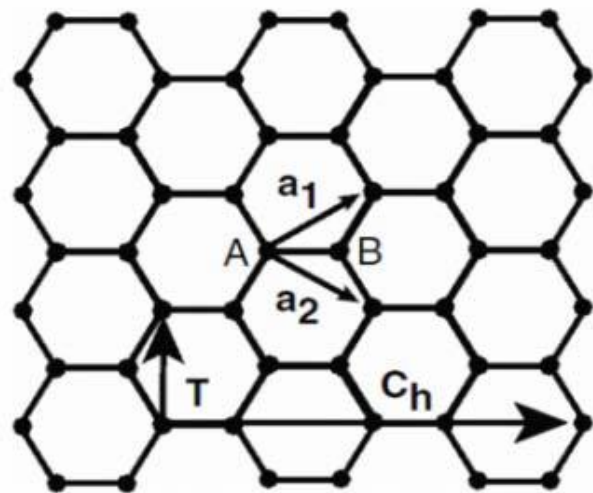

Fig1:- Graphene sheet rolling up to CNT

A CNT is depicted by its Chiral Vector: Ch = n â1 + m â2, ø = Chiral Angle concerning the crisscross hub, where â1 and â2 are cross segment preface vectors of graphene sheet and the chiral guide talks toward the edge that the center point of climbing sheet outlines with one of the commence vectors.

On the preface of chirality CNT can be assigned, jumble (ø = 0°), Chiral (0° < ø < 30°), or armchair (with ø = 30°).
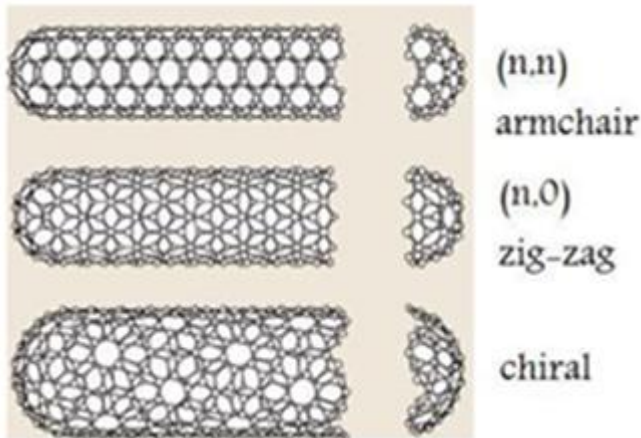

Fig2:- Metallic and semiconducting CNT

There are two types of carbon nano tubes: Single Walled CNT (SWCNT) and Multi Walled CNT (MWCNT).
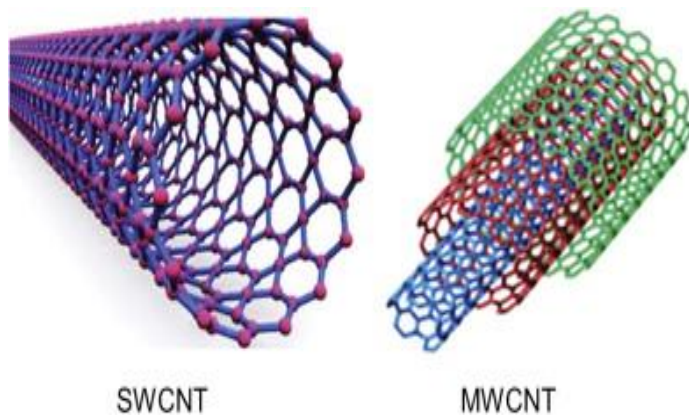

Fig3:- Types of CNT

A solitary divider carbon nanotube (or SWCNT) comprises of only one cylinder, and the straightforward assembling procedure of this gadget makes it an extremely encouraging as other option to today's MOSFET. A SWCNT can go about as either a conductor or a semiconductor relying upon the point of the particle course of action along the tube. Multi walled CNT (MWCNT) comprises of numerous moved layer (concentric tubes) of graphene.

III.CARBON NANO TUBE FIELD EFFECT TRANSISTOR (CNTFET)

CNTFET alludes to a field-impact transistor that uses a solitary carbon nanotube or a variety of carbon nanotubes as the channel material rather than mass silicon in the customary MOSFET structure. It is a three-terminal gadget comprising of a semiconducting nanotube bringing two contacts (source and deplete), and going about as a transporter channel, which is turned on or off electrically through the third contact (door).
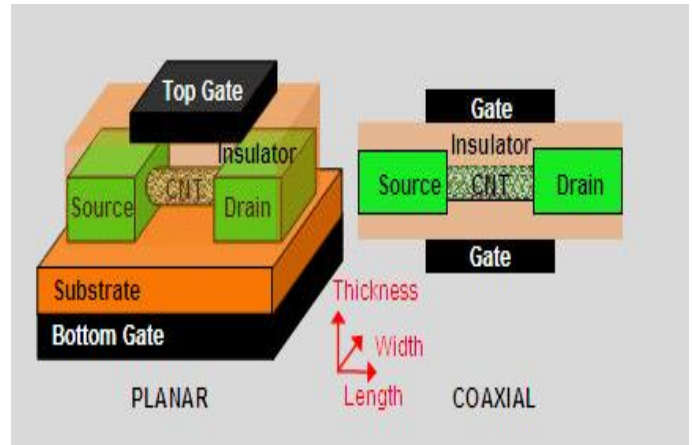

Fig4:- Structure of CNTFET

A single carbon nanotube is situated as an extension between two cathodes. The terminals turned into the source and deplete of the transistor, and the nanotube assumed the part of the channel. Applying the suitable voltage to door the nanotube is on or off. In the nanotube gadget, the transistor activity happens at the contact focuses between the metal terminals and the carbon nanotube. Semiconducting CNTs have been utilized to manufacture CNTFETs, which demonstrate guarantee because of their better electrical attributes over silicon based MOSFETs . As far as the gadget operation component, CNFET can be ordered as either Schottky Barrier (SB) controlled FET or MOSFET-like FET.

IV.   6T SRAM USING CNTFET

Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. It has two stable states which are used to denote "0" and "1". Two additional transistors(M5, M6) help in controlling the access to the cross coupled unit formed by the four transistors during read and write operations. So typically it takes six transistors to store one memory bit. The design of a basic SRAM cell is shown in Figure 5. Access to the cell is enabled by the word line (WL) which controls the two access transistors M5 and M6. These two transistors allow the access of the memory cell to the bit lines 'BL' and 'BLbar'. Bit lines are used to transfer data for both read and write operations. The dual bit lines i.e. 'BL' and 'BLbar' improves noise margins over a single bit line. The operation of CNFETs based memories is very similar to that of CMOS except for minor differences in device orientation.

Write Operation
The compose cycle starts by applying the esteem to be composed and its supplement to the bit lines. With a specific end goal to compose a '0', we would apply a "0" to the bit line "BL" and its supplement "1" to the 'BLbar'. A "1" is composed by altering the estimations of the bit lines i.e. by setting "BL" to "1" and "BLbar" to '0'. "WL" is then made high and the esteem that will be put away is hooked in.
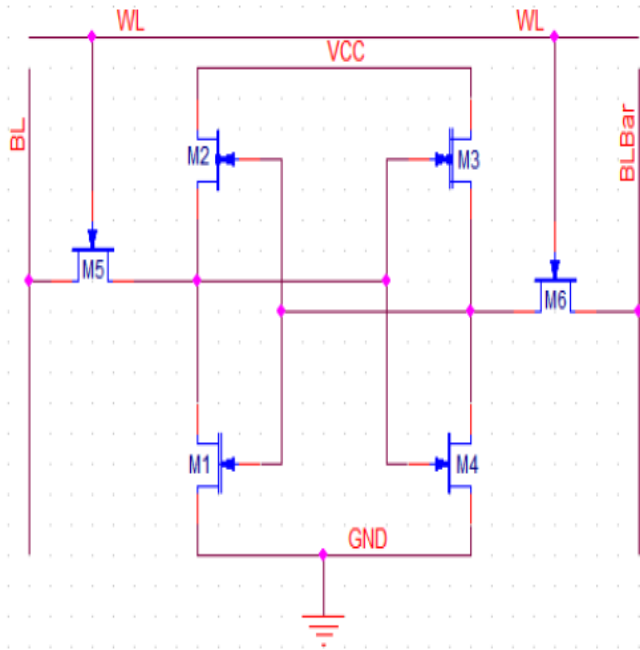
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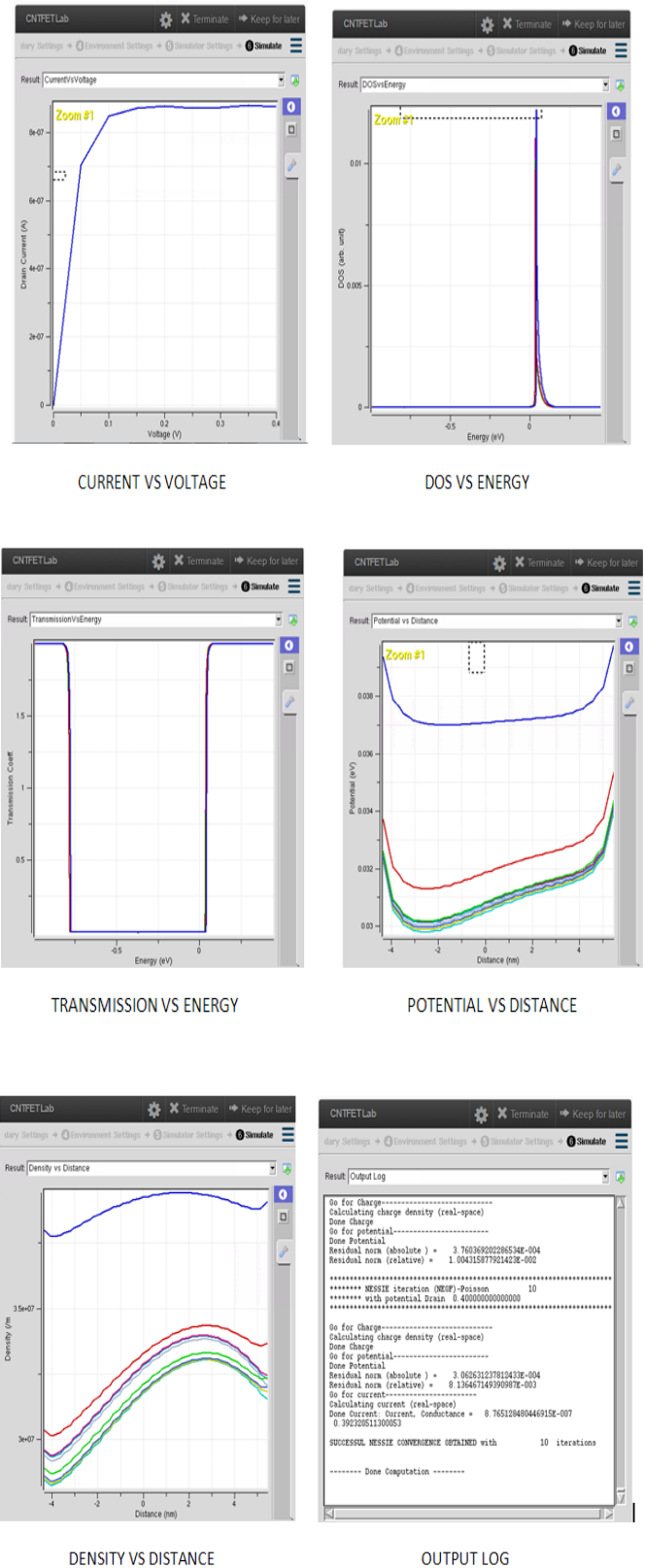
Fig5:- 6T SRAM using CNTFET

Read Operation

The read cycle begins by asserting the word line 'WL',and enabling both the access transistors M5 and M6. Then the values stored in 'Q' and 'Qbar' are transferred to the bit lines 'BL' and 'BLbar'. On 'BLbar' the values are transferred through transistors M1 and M6. On the BL side through transistors M4 and M5 which pull the bit line towards VDD (at the point when a "1" is put away at Q). In the event that the substance of the memory was a 0, the turn around would happen and "BLbar" would be pulled towards 1 and "BL" towards 0.

Idle State

For Idle state express, the word line is not affirmed and get to transistors M5 and M6 detach the cell from the bit lines. The two cross coupled inverters framed by M1, M2 and M3 M4 will keep on reinforcing each different the length of they are disengaged from any outer circuits.

V. CNTFET STIMULATION IN NANOHUB

We have used www.nanohub.org to stimulate CNTFET and these are the characteristic outputs[6]:-

CURRENT VS VOLTAGE

DOS VS ENERGY

TRANSMISSION VS ENERGY

POTENTIAL VS DISTANCE

DENSITY VS DISTANCE

OUTPUT LOG

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VI. CONCLUSION

A novel carbon nanotube field impact transistor (CNTFET) based single-finished 6T SRAM bitcell with a different read-port is proposed. Our proposed configuration demonstrates better strength un-der PVT variety than CMOS-based single-finished 6T SRAM outline and offers the focal points over CNTFET-based standard 6T SRAM bitcells as far as execution, soundness and power dissemination. Carbon-based gadgets indicate promising elements, with the goal that they are considered as potential contender to supplant silicon based MOSFETs later on. In this paper a SRAM Cell is composed utilizing CNTFETs at 32nm Technology to decrease compose control dispersal and to lessen the read delay. This circuit is composed and re-enacted in HSPICE utilizing Stanford CNFET display at 32nm innovation. MOSFET like CNTFET model is utilized to actualize 6T SRAM. This model is utilized for planning 6T SRAM circuits whose coding has been done in HSPICE, the yield waveform is shown. Execution of 6T SRAM recreation utilizing MOSFET and CNTFET is thought about. Execution utilizing CNTFET model is superior to the MOSFET based outline. CNT is a future trade for semiconductor based microelectronics.

FUTURE SCOPE

Assist investigation inside the foresaid space will be focused on development and position controlled amalgamation of nanotubes of given distance across. The most attractive future work required in CNTFETs will be the transistor with higher unwavering quality, shabby generation cost, or the one with more improved exhibitions. Execution utilizing CNTFET model is superior to the MOSFET based plan. As we scale down the transistor estimate it will be hard to drive information line so issue it can be overcome by sense intensifier in memory exhibit.

ACKNOWLEDGMENT

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