Speed enhancement and leakage reduction in advanced WDR image sensors

APARNA.P
ME VLSI DESIGN
Srinivasan Engineering College
chinju2014@gmail.com

G.SARANYA REVATHI
Associate Professor
Srinivasan Engineering College
sarshan8@gmail.com

***Abstract*— Static leakage current is the main source of power consumption in most of the systems, mostly which are in stable state in most of their operation time. In this paper a novel concept, AB^2 C (Adaptive Bulk Biasing Control) is used to reduce this leakage current in most of their standby mode of operation. It accelerates the performance during active cycles. Adaptive Bulk Biasing Control scheme is integrated with an advanced WDR image sensor as a test case. The memory cell in the WDR image sensor is a standard 6T SRAM bitcell, whose speed and delay can be scaled by using 7T SRAM. For every doubling of the RAM size the delay is found to be increased by one gate delay**

The AB^2 C provides 21% power reduction compared to standard systems and up to 41% as compared to accelerated systems.7T SRAM can perform better than 6T SRAM at low voltages

***Keywords*— Advanced Bulk Biasing Control, Advanced WDR image sensors, Static Random Access Memory, leakage reduction, gate delay**

I. INTRODUCTION

Active pixel sensors are the imagers that led to the development of advanced image sensors [1]. In these systems, several components are integrated within the pixel and periphery, enabling complex functionality and are different from the traditional CCD sensor arrays. Advanced image sensors provide a number of advantages in cost, power and speed. They can be used for image processing, target tracking and dynamic range expansion [2]. CMOS image sensors are rapidly advancing in high speed imaging. CMOS sensors utilize the natural advantage of a column-parallel readout from the pixels compared to high-speed CCDs, with a degree of parallelism represented by the number of panels. High-speed design focuses on challenges such as column-multiplexing, reduction of system noise and analog-to-digital conversion.

SRAM are very important component in many of the VLSI chips. The existing SRAM can be divided in to two groups, standard six transistor (6T) and seven transistor (7T) A 1-Mpixel digital image sensor with rolling shutter running at 500frames/s was presented, three years ago [3]. An improvement in data rate of an order of magnitude compared to the state-of the art high-speed CMOS sensors was showed. Since that time, the progress was steady, but gave only about a factor of 2 increases in data throughput over three years. The efforts were centered on the development of the pixels with a featuring competitive performance and full-frame shutter. The state-of-the-art in the year 2002 is believed to be a1000 frames/s sensor with a shutter pixel. The progress in high-speed CMOS imaging for many years in a row will still be defined by means of column-parallel architectures. Advanced image sensors utilize a higher pixel-level degree of parallelism may be an additional path to high-speed image capture [4].

A variety of techniques have been proposed for speed enhancement in VLSI circuits. These include the use of on-chip parallel 10-b analog-to-digital converters (ADCs), global shutter CMOS image sensor manufactured in Tower Jazz 0.18 μm CIS technology and application of negative voltages to wells and substrates. The later technique dynamically raises the threshold voltage by means of reverse body bias (RBB) or lowered it by means of forward body bias (FBB). Varying the threshold voltage enable acceleration of the device speed during operational cycles and leakage reduction during idle periods.

AB^2C technique, originally proposed by Fish et al [5].is based on the employment of body biasing for leakage in image sensors for the enhancement of speed .In this technique the reverse body bias is applied dynamically using a network of resistors to the row of pixels, when the rows are not accessed. Since it have a bulk capacitance, dynamic discharging and charging has side effects such as bulk charging delay, noise or interference and additional power consumption. These problems can be reduced by means of gradual voltage application in the AB^2C scheme.

Even though AB^2C scheme are used for integration with image sensors operating in the rolling shutter operation mode, it can also be applied to a serially accessed memory array, and as a test case, we integrated It into a wide dynamic range (WDR) advanced image sensor employing an on-chip SRAM. The advanced WDR image sensors have improved functionality, performance, robustness, and flexibility over the original.

II. EFFECTS OF BODY BIASING

A. Body Biasing

The threshold voltage of a transistor can be represented as

$$V_T = V_{T0} + \gamma\ [\sqrt{2\Phi_b - V_{BS}} - \sqrt{2\Phi_b}\quad (1)$$

Where V_{T0} is the zero biasing voltage, that is set during fabrication; γ is the body-effect coefficient; ϕ_b is the Fermi potential and V_{BS} is the body-to-source voltage. *Body effect*; is the change in the threshold by creating a potential between the source and body terminals of the transistor .The speed enhancement is done by means of the body biasing in many of the digital circuits only up to 60 nm . The effectiveness of the technique degrades, as technology scales due to several factors, such as the higher influence of *drain induced barrier lowering* (DIBL) and other parameters on sub threshold leakage [6] and the increase of *band-to band Tunnelling* current (BTBT) as a result of applying RBB. Body biasing techniques are quiet interested for both improving variation sensitivity as well as performance enhancement in advanced processes.

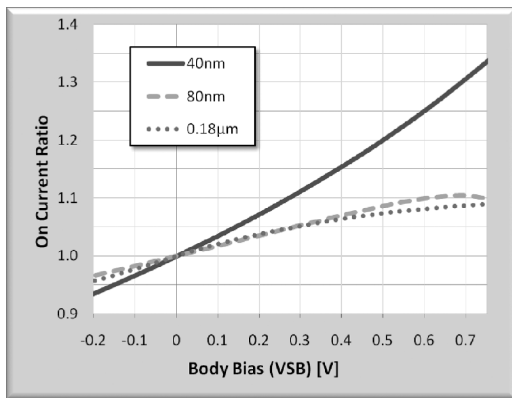
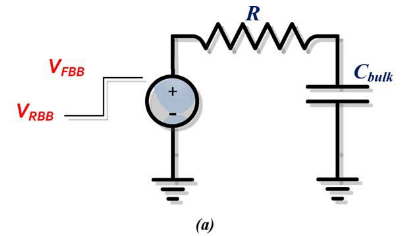


Fig .1 .The effectiveness of body biasing for performance enhancement at different process nodes The figure is plotted for minimum sized devices with $V_{GS} = V_{DS} = V_{DD}$

Lowering the threshold voltage that increases a device's *ON* current leads to the performance enhancement. A forward body bias is applied, and has the positive side-effect of reducing the standard deviation of the threshold voltage distribution. Fig. 1 shows the effect of forward body biasing on the saturation current (with $V_{GS} = V_{DS} = V_{DD}$) of a minimum sized nMOS transistor at various (low power) process nodes. The figure shows the drain current increases, as compared to a zero-biased equivalent transistor.

B. Application of Body Biasing

In addition to the dynamic control and the system performance enhancement this technique can be used for adapting circuits for performance under process variations. For the body biasing separate well are required for each transistor for different body potential. So it requires the implementation of techniques such as DTCMOS [7] though the size requirement for each transistors are very large.ie A specific circuit with limited number of devices or an entire block of devices with a common well potentials can only make use of the body biasing. Only the later can be considered in the case of a pixel or bitcell arrays with thousands or millions of devices



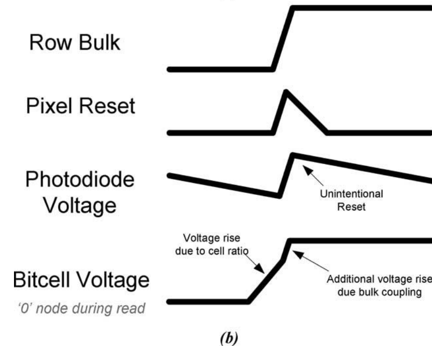


Fig. 2. Step charging the bulk of a pixel/bit cell row. (a) RC modeling of a step charge operation. (b) Possible disturbances that can be caused to a pixel or bitcell during readout.

A row wise addressing is commonly used for cell access .Accordingly FBB provides an efficient method for performance enhancement. The n-well and p -well in each cell in a certain row should be common .These well are modelled as a lumped RC network.

III. BODY BIASING WITH AB^2C SCHEME

A. Gradual Bulk Biasing

Consider the circuit shown Fig. 3(a) with 2N capacitors (each representing the bulk. capacitance of a single row) connected in parallel with approximately equal resistances between them. Apply a potential, V_{bias} , to one of the middle capacitors, a constant voltage drop will be symmetrically applied to the remaining capacitors, as they progress towards the opposite voltage supply and can be further extended by connecting the two end nodes and grounding them. A ring of RC circuits symmetrically biased around the virtual line connecting the biased node with the grounded one . The biasing point can easily be moved to a different bulk without upsetting the symmetry, by changing the connection node of both the bias voltage and the ground supply. This is analogous to changing the bias point of the active row.

This scheme results in a gradual voltage drop between the two biasing points. This transition to an adjacent row causes a slight voltage change of ΔV at each node . This small change has a very small disturbance effect as compared to the full step charge, especially since the change is gradual at then on-directly biased nodes. Therefore, a forward biased node can be set at one end of the circuit and a reverse bias can be set at the opposite end, without the need for large drivers or the danger of applying a large abrupt voltage step.

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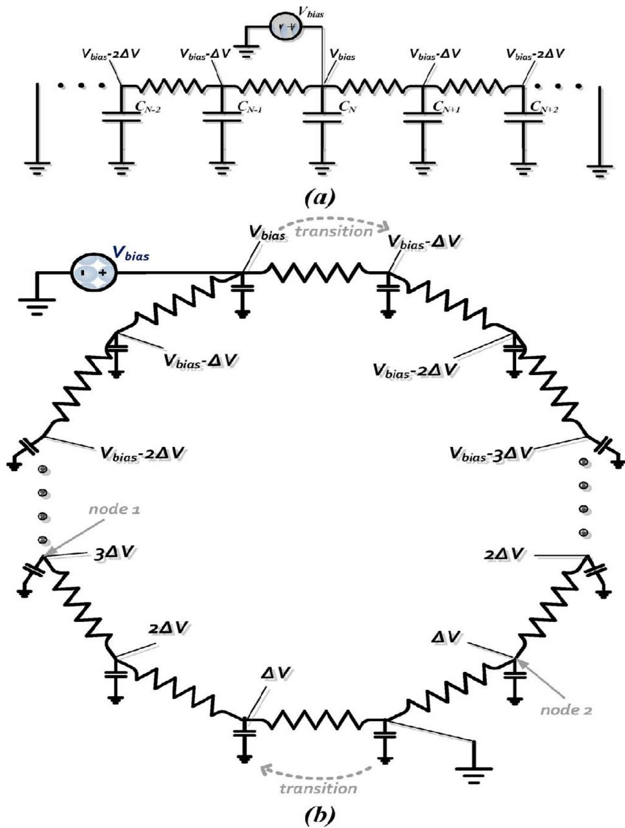

Fig.3. RC modelling of gradual step charging setup. (a) Application of bias voltage to the middle row of resistive connected parallel bulk capacitances. (b)Extension of the bulk biasing setup to a symmetric ring

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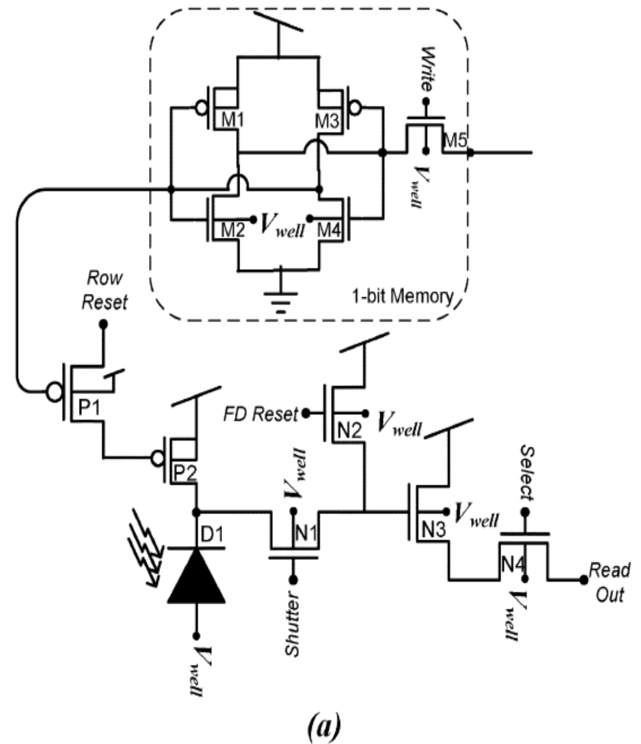
Ends of the arrays, where the original circuit lost correct biasing structure. Second, the resistors are replaced with constant biased nMOS transistors [8]. This creates adaptable, high.

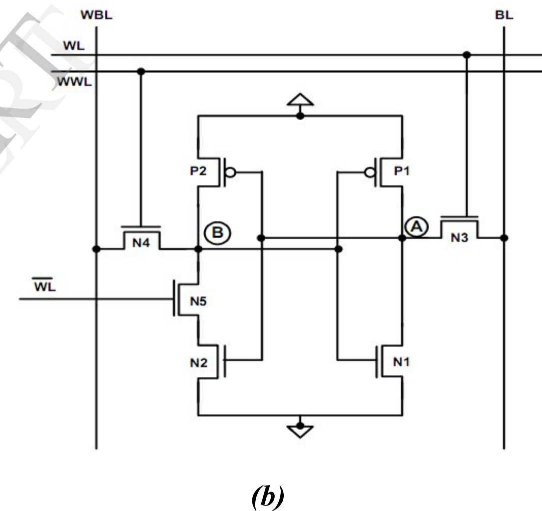
6T SRAM bit cell with minimum sized pMOS and access transistors (M1, M3, M5, and M6) and slightly larger pull-down nMOS (M2 and M4) is used as the standard memory cell.1-bt in pixel resistance, small area resistors, and enables further flexibility, as will be shown herein. Third, the AB^2C improved concept is suitable for utilization in SRAM arrays. In this paper we show an example of its application to a serially accessed SRAM array that is operated in cohesion with a pixel array, as part of a wide dynamic range advanced image sensor.

IV AB^2C SCHEME APPLICATION

A. Pixel and SRAM Bitcell

The WDR pixel and SRAM bitcell are shown in the Fig 5 (a) and (b).





(b)

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The seven transistors memory cell is designed by adding a data protection NMOS Transistor N5 between node B and transistor N2 [1]. While SRAM cell is being accessed, WL is in activated state, 0 and N5 is OFF. Since N5 prevents the volt age at Node B From decreasing, the data bit is not reserved even if Node A voltage greatly exceeds Shown in Figure 3 Seven transistor SRAM consists of three word lines which are WWL, WL , WL and two complementary bit lines BL and WBL. WL and WL are complementary and WL is used to control the word lines WWL and WL. The write operation for SRAM 7T is same as that of 6T SRAM cell. In write operation one of the bit line is charged and the other

discharged and the word lines WWL and WL are closed in order to write in the nodes A and B. During data retention period, when the SRAM cell is not being accessed, word line signal WL is 1 and NMOS transistor N5 is ON. The use of two CMOS inverters results in high cell stability. During read operation, the logical threshold voltage of the CMOS inverter driving node B increases greatly when the data protection NMOS transistor N5 is turned off. For this re as on, the re ad value at A = 0 remains large even when access NMOS transistor N3 is turned on and node A voltage increases

The voltage dividing effect takes place at the inverter which stores 0, will be pulled up. In order to stop this transition the 7th transistor at the other node is turned off so that the node which stores 1 will not be pulled down b y the driver transistor as it acts a switch between the node and the driver transistor. In read operation the SRAM cell is isolated from the bit lines and the bit lines are precharged to V_{DD}. When the word lines are closed the bit lines which is connected to the node which stores 0 will be discharged through pass transistor while the other bit line stays high

The synthesis results can be better analyzed by tabular representation

TABLE I
STATIC NOISE RESPONSE

SRAM Type	**Write operation**	**Delay (ps)**	**Read operation**	**Delay (ps)**
6T SRAM	Write 0	340	Read 0	387.5
7T SRAM		270		360.7
6T SRAM	Write 1	320	Read 1	270.3
7T SRAM		260		253.5

TABLE 2

Voltages		**SRAM 6T**	**SRAM 7T**
Vdd	**Vss**	**Read Delay (ps)**	**Read Delay (ps)**
1.07	0	15	09.22
1.07	0.12	315.94	14.36
0.96	0.12	46.65	26.62
0.96	0.24	54.68	32.02
0.84	0.24	63.13	57.53
0.84	0.36	77.24	67.36
0.72	0.36	88.98	79.4
1.2	0	09.5	4.6

V. CONCLUSIONS

An improved AB^2 C scheme provides a leakage reduction and /or performance enhancement when integrated with an advanced WDR image sensors. A 21% leakage reduction was achieved for the fabricated sensor as compared to an equivalent non-biased sensor with a negligible increase in dynamic power or performance reduction. A 44% leakage reduction was achieved for a performance enhanced system employing forward body biasing.

The implementation of the scheme integrated with WDR image sensors in Xilinx ISE 13.2 software

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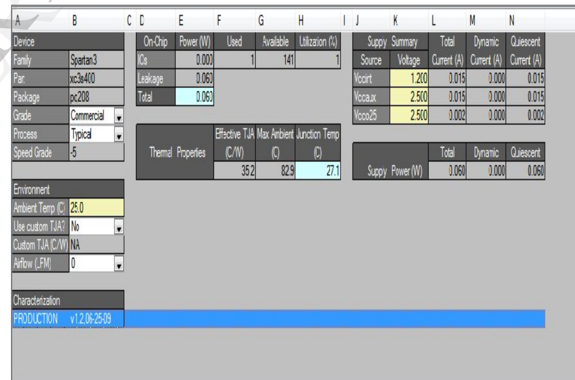

The 7T SRAM performs better than 6T at lower voltages,with minimum delay.so the speed of the operation can be enhanced by changing the 6T SRAM by 7T SRAM

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