# Solvothermal Synthesis, Fabrication and Characterization of ULSI Nano interconnects using Nano Silver (Ag)

K. Aravindh
Department of Electronics and Communication Engineering,
V.S.B.Engineering College, Karur

R. Dhayabarani M.E.
Associate Professor,
Department of Electronics and Communication Engineering,
V.S.B.Engineering College, Karur

***Abstract:*** **In order to satisfy Moore's prediction law digital circuit fabrication technology has undergone various stages of evolution from Small Scale Integration (SSI) to Very Large Scale Integration (VLSI). Further for future scaling; industrialists and researchers are very much concentrated in Ultra Large Scale Integration (ULSI) technology; where interconnect issues turn out be serious bottle neck limiting the overall performance of the circuit. In our paper; we have proposed a solution that will hold good for the interconnect issues with future technologies. After going through a serious of pros and cons with copper element as interconnect in ULSI technology we have analyzed the suitability and need for silver metal among various different metal elements as substitute element to replace conventional copper as interconnect. To start up with; initially Silver nano-particles were synthesized from its precursor Silver Nitrate (AgNO3) by a novel solvothermal and filtration process; SEM images and XRD analysis of prepared silver nano-particles were carried out and the results were checked to conform the formation of silver nano-particles. Thus prepared silver nano-particles were used to draw interconnect patterns and these patterns were characterized to prove its identity to find application as interconnect in ULSI technology.**

***Key words: Moore's Law; Interconnect Issues; Silver Nano-Particles; Solvothermal Process; Filtration Process; ULSI***

## 1. INTRODUCTION

Interconnect, as the name describes is a medium to inter-connect two or more devices on a chip. The function of an interconnect is to distribute clock and other signals to the various functional blocks of a CMOS integrated circuit, along with providing necessary power and ground connections [1]. In order to understand the need for an interconnect system in proper functioning of a chip we need to study the importance of clock/power /ground signal.

### *1.1 IMPORTANCE OF CLOCK SIGNAL:*

A Clock signal is generally referred to as "the heartbeat" of the any digital circuit chips. A digital clock signal is basically a square wave voltage similar as the one shown below [2]:

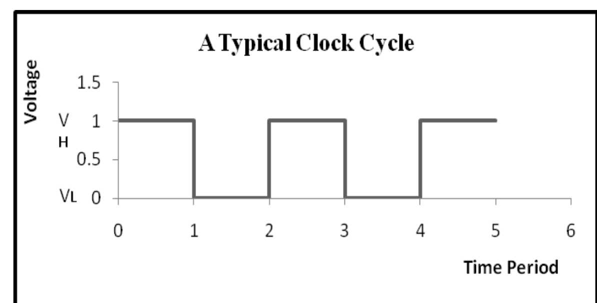


Figure No. 1: A Typical Clock Signal

where $V_H$ - Highest Clock Voltage
$V_L$ -Lowest Clock Voltage

In electronics and especially synchronous digital circuits, a clock signal is a particular type of signal that oscillates between a high and a low state and is utilized like a metronome to coordinate actions of circuits[5]. Although the word signal has a number of other meanings, the term here is used for "transmitted energy that can carry information". Most integrated circuits (ICs) of sufficient complexity use a clock signal in order to synchronize different parts of the circuit, cycling at a rate less than the worst-case internal propagation delays. As ICs become more complex, the problem of supplying accurate and synchronized clocks to all the circuits becomes increasingly difficult. The clock distribution network distributes the clock signal(s) from a common point to all the elements that need it. Since this function is vital to the operation of a synchronous system, much attention has been given to the characteristics of these clock signals and the electrical networks used in their distribution. Clock signals are typically loaded with the greatest fan out and operate at the highest speeds of any signal within the synchronous system. Since the data signals are provided with a temporal reference by the clock signals, the clock waveforms must be particularly clean and sharp. Furthermore, these clock signals are particularly affected by technology scaling (Moore's law), in that long global interconnect lines become significantly more resistive as

line dimensions are decreased. This increased line resistance is one of the primary reasons for the increasing significance of clock distribution on synchronous performance. Finally, the control of any differences and uncertainty in the arrival times of the clock signals can severely limit the maximum performance of the entire system and create catastrophic race conditions in which an incorrect data signal may latch within a register. The proper design of the clock distribution network helps ensure that critical timing requirements are satisfied and that no race conditions exist .Novel structures are currently under development to ameliorate these issues and provide effective solutions.

*1.2 INTERCONNECTS :*

The fundamental development requirement for interconnect is to meet the high-speed transmission needs of chips despite further scaling of feature sizes. The *Interconnect* chapter of the 1994 National Technology Roadmap for Semiconductors (NTRS)[1] described the first needs for new conductor and dielectric materials that would be necessary to meet the projected overall technology requirements. With the publication of the 1997 edition of the NTRS, the introduction of copper-containing chips was imminent. The 1999 International Roadmap highlights a continued change to new materials, now being introduced at an unprecedented pace. In 2001, these materials introductions continue, but a solution must for the problem associated with increases in conductor resistivity stayed unknown. The slower than projected pace of low-κ dielectric introduction for MPUs and ASICs is one of the central issues for the 2003 ITRS Interconnect area.The 2005 ITRS shows the calculated electron scattering induced Cu resistivity rise for future technology generations, as well as the resultant effect on resistance and capacitance (RC) performance metrics. A crosstalk metric was also introduced in 2007. Managing the rapid rate of materials introduction and the concomitant complexity represents the overall near-term challenge. For 2011, Interconnect performance is at the forefront as a key challenge to achieve overall chip performance. In 2012 reports from IRTS its concluded that Cu and low-κ interconnects will probably represent the final "conventional" interconnect technology. There are no metals with significantly lower resistivity than Cu. But it is eminent that Ag has significantly lower resistivity than Cu from Table No.1 which has a comparison of various metals.

Table No.1: shows the resistivity of several materials. The values are correct at 20 degrees Celsius.[2]

| Elements | Resistivity at 20 °C (Ω.m) | Elements | Resistivity at 20 °C (Ω.m) |
|---|---|---|---|
| Aluminum | $2.82 \times 10^{-8}$ | Lead | $2.2 \times 10^{-7}$ |
| Carbon (Graphite) | $3.5 \times 10^{-5}$ | Manganin | $4.82 \times 10^{-7}$ |
| Constantan | $4.9 \times 10^{-7}$ | Mercury | $9.8 \times 10^{-7}$ |
| Copper | $1.7 \times 10^{-8}$ | Platinum | $1.1 \times 10^{-7}$ |
| Germanium | $4.6 \times 10^{-1}$ | Quartz (fused) | $7.5 \times 10^{17}$ |
| Glass | $10^{10}$ to $10^{14}$ | Silicon | $6.40 \times 10^{2}$ |
| Gold | $2.44 \times 10^{-8}$ | ***Silver*** | ***$1.59 \times 10^{-8}$*** |
| Iron | $1.0 \times 10^{-7}$ | Tungsten | $5.6 \times 10^{-8}$ |

Even though a suitable replacement is found in our paper the most Critical Challenges faced at nm scaling and their respective issues is given in Table No.2.

Table No.2: Critical challenges and issues with interconnect design for future.[3]

| MOST CRITICAL CHALLENGES AT NANOMETER SCALING | SUMMARY OF ISSUES |
|---|---|
| **Material** Introduction of new materials to meet conductivity requirements | The rapid introductions of new materials/processes that are necessary to meet conductivity requirements create integration and material characterization challenges. |
| **Manufacturable Integration** Engineering manufacturable interconnect structures, processes and new materials | Integration complexity, CMP damage, resist poisoning, dielectric constant degradation. Lack of interconnect/packaging architecture design optimization tool |
| **Reliability** Achieving necessary reliability | New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling, and control of failure mechanisms will be key. |
| **Cost & Yield for Manufacturability** Manufacturability and defect management that meet overall cost/performance requirements | As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion. |

## 2. MATERIALS AND METHODS

*2.1. Chemicals Used:*

Silver nano-particles were reduced from its precursor salt silver nitrate ($AgNO_3$) with the help of Sodium borohydride ($NaBH_4$). Both silver nitrate ($AgNO_3$) and sodium borohydride ($NaBH_4$) were procured from E-Merck. All the chemicals are GR grade without any purification.

*2.2. Experimental procedure*

Silver nano-particles were synthesized by a novel method known as solvothermal process followed by filtering process.

**STEP1**: Preparation of 0.1M Silver Nitrate ($AgNO_3$) solution. Take 1.6987g $AgNO_3$ and add 100ml distilled water in SMF, now cover the beaker in black color carbon ribbon paper (or) black cloth. To find the weight of Silver Nitrate ($AgNO_3$) the following formula is used,

$$W = (M.W*molarity*100)/1000 \text{ -------- } (1)$$

**STEP2**: Preparation of 0.1M of Sodium Borohydride ($NaBH_4$) solution.
By using the same formula 0.3783g weight of $NaBH_4$ is measured and 100ml of distilled water is added. In solvothermal process freshly prepared 0.1M Silver nitrate ($AgNO_3$) salt solution is stirred by using mechanical stirrer at a rotating speed of 1200 rpm. Similarly prepared 0.1M of Sodium borohydride ($NaBH_4$) solution is added to Silver Nitrate($AgNO_3$) solution drop by drop for 10minutes, now the solution slowly turns into brown color. Insert the RB(Round Bottom) flask on top of the SMF. The RBflask is designed with water inlet one side and water outlet on the other. Magnetic rod is inserted into the beaker and continuous stirring is carried out for 24hrs.
Overall chemical reaction carried out is written as, $\mathbf{AgNO_3 + NaBH_4 \rightarrow Ag^0 + 0.5\ H_2 + 0.5\ B_2H_6 + NaNO}$
Finally we get the clear solution in bottom of the silver formed after that to remove the solution by using the filteration process to take the filter paper and distelled water to remove the solution after getting silver and filter paper to heat at $80^0$C in heat oven at 1hr after to be formed pure silver nanoparticles of range 90 nm to few microns.

## 3. RESULTS AND DISCUSSIONS:

### *3.1 SEM & XRD Analysis:*
The SEM images of prepared silver nano-particles are shown below:

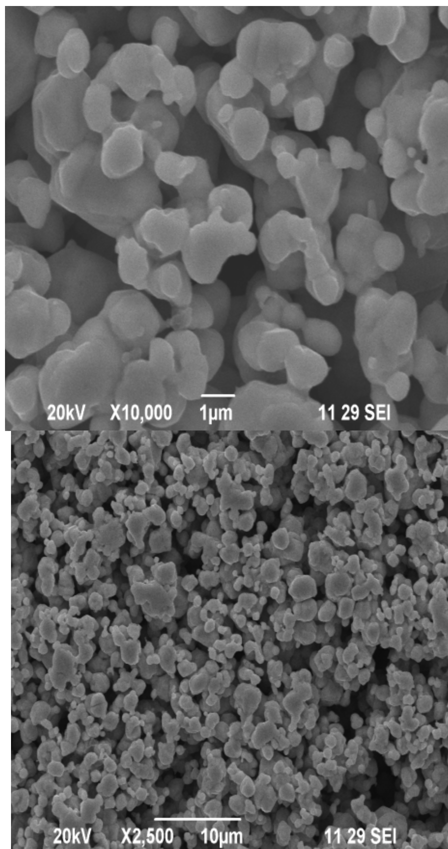

Figure No. 2: SEM image of Nano Silver

Silver nano-particles prepared has been investigated by x-ray diffraction analysis. The XRD indicates the formation of silver nanoparticles (Ag) and helps to identify contamination in the prepared Silver nano-particles.

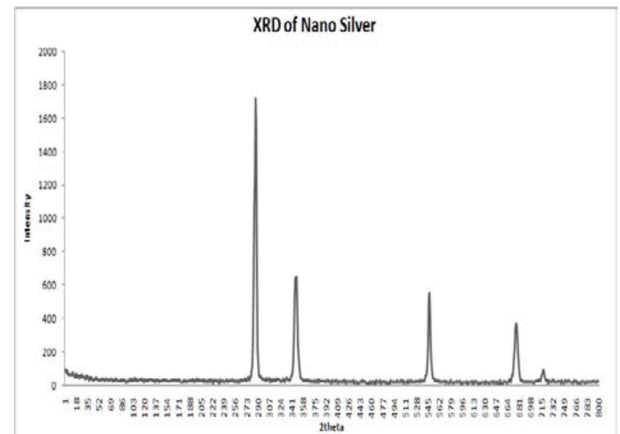

Figure No. 3: XRD plot of Nano Silver

### *3.2 Characterization of Nano Silver Interconnects:*
The structure of Interconnect patterns is shown below:

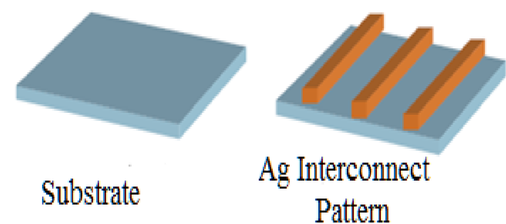

Figure No. 4: Proposed Structure of Silver Interconnect Patterns on Flexible Substrate

The VI characteristics of the interconnect lines are drawn with the help of NI Lab view discrete components measurements.

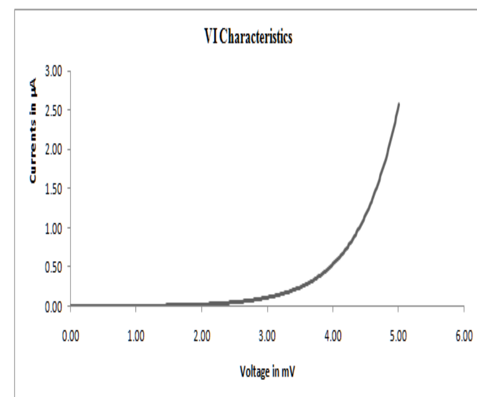

Figure No.5: VI characteristics of Nano Silver Interconnects

## 4. CONCLUSIONS:
The resistivity of the Nano silver Interconnects, whose length is 1cm and width is 10µm, is found to be 0.0785µΩ.m at room temperature (30°C), which is proved to be much more conducting compared to an ordinary silver at 20°C. Hence, nano silver based interconnects can be used in IC chip replacing conventional Copper interconnects.

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