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SmartFlow: FPGA-Based Adaptive Traffic Management for Enhanced Pedestrian Safety at Highway-Village Junctions

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Abstract
This paper presents SmartFlow, an FPGA-based adaptive traffic management system designed to enhance pedestrian safety at highway-village junctions and zebra crossings. The system integrates ultrasonic sensors (HC-SR04), a Field-Programmable Gate Array (FPGA) programmed in Verilog HDL, and a buzzer to detect and deter traffic signal violations in real time. Ultrasonic sensors monitor vehicle proximity within 20 cm of zebra crossings during red light phases, transmitting data to the FPGA via GPIO pins. The FPGA processes these inputs using a finite state machine, controlling LED-based traffic signals (green: 15s, yellow: 3s, red: 10s) and triggering a 1 kHz buzzer alert upon detecting violations.
Implemented on an Edge Artix-7 FPGA board, the prototype employs a cardboard road model to simulate highway–service road junctions, ensuring accurate vehicle detection and immediate auditory feedback. The sys-tem operates autonomously, eliminating manual intervention, and is scalable for broader applications through the incorporation of additional sensors. Experimental results demonstrate reliable detection of vehicles cross-ing during red signals, with buzzer alerts effectively notifying pedestrians and drivers, thereby reducing accident risks.
The system enhances traffic discipline, protects vulnerable road users, and mitigates congestion at critical junctions. By leveraging digital electronics and sensor fusion, SmartFlow offers a cost-effective and robust solu-tion for smart traffic infrastructure, particularly in semi-urban and rural environments with significant pedestrian traffic. Future enhancements include integrating machine learning for predictive traffic analysis and expanding sensor networks for multi-lane coverage. This work contributes to safer and more efficient transportation systems, aligning with global smart city initiatives and sustainable urban planning goals while addressing the critical need for automated traffic violation detection and pedestrian safety at complex road junctions.

keywords
FPGA, Ultrasonic Sensors, Traffic Management, Pedestrian Safety, Verilog HDL, Real-Time Systems, Highway Junctions, Zebra Crossings, Traffic Signal Violation, Smart Infrastructure

1 INTRODUCTION

The rapid urbanization and increasing vehicular traffic at highway-village junctions and zebra crossings have in-tensified safety concerns, particularly for pedestrians. In 2021, India reported over 150,000 road traffic fatalities, with pedestrians accounting for a significant portion due to signal violations and inadequate traffic management (4; 30). Traditional traffic systems often rely on static signal timings and manual enforcement, which fail to ad-dress dynamic traffic patterns and real-time violations, especially in semi-urban and rural settings. The SmartFlow system addresses these challenges by introducing an FPGA-based adaptive traffic management solution that inte-grates ultrasonic sensors, Verilog HDL programming, and real-time auditory alerts to enhance pedestrian safety and traffic discipline (2; 26).

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1.1 Problem Statement

Highway-village junctions and zebra crossings are highly prone to accidents caused by vehicles disregarding red signals or encroaching into pedestrian zones. The absence of real-time detection and alert mechanisms exacerbates the risk, particularly in areas with heavy pedestrian activity, such as school zones or rural markets (14; 27). Existing systems often depend on expensive infrastructure or human intervention, which limits their feasibility in resource-constrained environments.

1.2 Proposed Solution

SmartFlow employs an Edge Artix-7 FPGA board, ultrasonic sensors (HC-SR04), and a buzzer to detect vehicles within 20 cm of zebra crossings during red light phases. The FPGA, programmed in Verilog HDL, implements a finite state machine to control traffic signals (green: 15 s, yellow: 3 s, red: 10 s) and trigger a 1 kHz buzzer alert upon detecting violations. A cardboard prototype simulates real-world junctions, enabling scalable and cost-effective deployment (6; 16).

1.3 Significance and Objectives

The system eliminates manual monitoring, reduces accident risks, and promotes traffic discipline by providing immediate feedback to both drivers and pedestrians. Its key objectives include detecting signal violations, issuing real-time alerts, ensuring FPGA-based control, and improving safety at critical junctions (20; 32). By leveraging digital electronics and real-time processing, SmartFlow contributes to smart city initiatives and sustainable urban development.

2 RELATED WORK

The development of intelligent traffic management systems has been a focal point in addressing road safety and congestion, particularly at pedestrian-heavy junctions. Recent advancements in embedded systems, sensor technologies, and IoT have spurred innovative solutions, yet challenges remain in achieving cost-effective, scalable, and real-time systems for semi-urban and rural settings. This section reviews key contributions in traffic manage-ment, FPGA-based control, and pedestrian safety, highlighting their methodologies, findings, and limitations, and positions the proposed SmartFlow system within this landscape.

(1) developed an IoT-based traffic surveillance system using smart cameras, achieving 95% accuracy in ve-hicle detection across urban intersections. However, the system's reliance on high-resolution cameras and cloud computing makes it computationally intensive and less feasible for resource-constrained environments. (2) and (6) explored FPGA-based traffic light controllers programmed in Verilog HDL, demonstrating low-latency signal transitions (under 10 ms) and efficient state machine designs. These systems, while robust for signal timing, lack mechanisms for detecting traffic violations or prioritizing pedestrian safety, limiting their applicability at complex junctions.

(3) and (16) investigated ultrasonic sensors for vehicle detection, reporting a detection range of 2–400 cm with 98% accuracy under controlled conditions. Their work highlights the cost-effectiveness of ultrasonic sensors but notes challenges in integrating them with traffic signal systems for real-time violation detection. (4) conducted a comprehensive review of pedestrian safety at urban intersections, identifying signal violations as a leading cause of pedestrian fatalities (30% of cases). Similarly, (30) emphasized the need for automated detection systems to reduce accidents at zebra crossings, citing a 25% reduction in incidents with real-time alerts.

(8) and (13) proposed IoT-based smart city traffic frameworks, integrating sensor networks and cloud analytics for dynamic traffic management. These systems achieved up to 20% congestion reduction but require extensive infrastructure, making them less suitable for rural highway-village junctions. (11) and (31) implemented embed-ded systems for real-time violation detection, using infrared and ultrasonic sensors, respectively. Their systems achieved 90% detection accuracy but relied on expensive microcontrollers, increasing deployment costs.

(9) combined FPGA with machine learning for adaptive signal timing, reducing average wait times by 15% in simulations. However, the complexity of machine learning integration limits its practicality for low-cost applica-tions. (7) and (32) focused on sensor-based traffic management for highways, reporting reliable vehicle detection but lacking auditory feedback mechanisms critical for pedestrian alerts. (23) and (26) underscored Verilog's effi-cacy in FPGA-based real-time systems, achieving sub-millisecond response times, which aligns with SmartFlow's design goals.

(14) and (27) highlighted the importance of sensor fusion for pedestrian safety in rural settings, noting a 40% accident reduction with integrated systems. (17) and (24) explored smart traffic systems for urban mobility, em-

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phasizing scalability but overlooking semi-urban challenges. (19) and (22) reviewed adaptive signal control, iden-tifying real-time data processing as a key enabler for traffic efficiency.
The comparative table below evaluates these works against SmartFlow, focusing on technology, detection range, real-time capability, cost, and pedestrian focus.

Table 1: Comparative Analysis of Traffic Management and Safety Systems

Reference	Technology	Detection Range	Real-Time Capability	Cost	Pedestrian Focus
(1)	IoT, Cameras	10–100 m	Yes	High	Moderate
(2)	FPGA, Verilog	N/A	Yes	Moderate	Low
(3)	Ultrasonic Sensors	2–400 cm	Yes	Low	Moderate
(4)	Review	N/A	N/A	N/A	High
(6)	FPGA, Verilog	N/A	Yes	Moderate	Low
(7)	Ultrasonic Sensors	5–300 cm	Yes	Low	Moderate
(8)	IoT, Sensors	10–50 m	Yes	High	Low
(9)	FPGA, ML	N/A	Yes	High	Moderate
(11)	Embedded Systems	5–200 cm	Yes	High	High
(13)	IoT, Sensors	10–100 m	Yes	High	Low
(16)	Ultrasonic, Infrared	2–400 cm	Yes	Moderate	Moderate
(32)	Sensors	5–300 cm	Yes	Low	High
(14)	Sensor Fusion	5–200 cm	Yes	Moderate	High
(27)	Sensors	10–300 cm	Yes	Low	High
SmartFlow (Proposed)	FPGA, Ultrasonic, Verilog	2–20 cm	Yes	Low	High

SmartFlow addresses gaps in existing systems by combining low-cost ultrasonic sensors with FPGA-based real-time processing, focusing on pedestrian safety at highway-village junctions. Unlike (1) and (13), it avoids complex infrastructure, and compared to (2) and (6), it incorporates violation detection and auditory alerts, making it more suitable for pedestrian-heavy environments (30; 32).

3 SYSTEM ARCHITECTURE

The SmartFlow system is a robust, FPGA-based traffic management solution designed to enhance pedestrian safety at highway-village junctions and zebra crossings. It integrates hardware and software components to achieve real-time vehicle detection, signal control, and violation alerting, using an Edge Artix-7 FPGA board, ultrasonic sensors (HC-SR04), LEDs, and a buzzer, all programmed in Verilog HDL for autonomous operation (23; 26).

3.1 Hardware Components

The hardware setup ensures reliable detection and signaling:

- FPGA Board (Edge Artix-7): Serves as the central processing unit, handling sensor data and controlling outputs via GPIO pins. Its reconfigurable nature supports low-latency processing (sub-10 ms) (2; 6).
- Ultrasonic Sensors (HC-SR04): Two sensors measure vehicle distance (2–20 cm) near zebra crossings, with trigger pins outputting 10 µs pulses and echo pins receiving reflected signals. They offer 3 mm accuracy (3; 16).
- LEDs: Three LEDs per traffic direction (main and cross streets) indicate green (15 s), yellow (3 s), and red (10 s) signals, connected to FPGA output pins (19).
- Buzzer: Generates a 1 kHz square wave for auditory alerts during violations, connected to an FPGA output pin (11).

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- Breadboard and Power Supply: Facilitates connections, with a 5V supply powering sensors and LEDs via jumper wires.
- Cardboard Model: Simulates a highway-village junction with zebra crossings and lane markings for pro-totyping.

3.2 Software Design

The system is implemented in Verilog HDL, comprising four key modules:

- tf3 Module: Implements a finite state machine (FSM) with four states (main green/cross red, main yel-low/cross red, main red/cross green, main red/cross yellow), controlling signal timing (31 s cycle) (26).
- sensor_controller Module: Manages ultrasonic sensors, triggering measurements every 60 ms and process-ing echo times to calculate distances (7).
- ultrasonic_sensor Module: Handles trigger pulse generation and echo time measurement, outputting dis-tance data (21-bit) (3).
- alarm and buzzer Modules: Detect violations (distance < 20 cm during red signal) and generate a 1 kHz buzzer tone (11).

3.3 System Operation

The operational flow ensures real-time violation detection:

1. Initialization: The FPGA powers on, initializing the tf3 and sensor_controller modules.
2. Sensor Monitoring: Ultrasonic sensors measure vehicle distance every 60 ms, sending data to the FPGA.
3. Violation Detection: During red signals, the FPGA checks for vehicles within 20 cm of the zebra crossing.
4. Alerting: Violations trigger the buzzer (1 kHz) and update LED states (red for stop).
5. Continuous Operation: The FSM cycles through signal states, ensuring uninterrupted monitoring (9; 32).

3.4 Block Diagram

The block diagram illustrates the system's architecture, depicting the FPGA interfacing with two ultrasonic sensors (trigger/echo to GPIO), three LEDs per direction (main/cross streets), and a buzzer. Data flow shows sensor inputs processed by the FPGA to control outputs. [Create and upload block_diagram.pdf to your Overleaf project.]

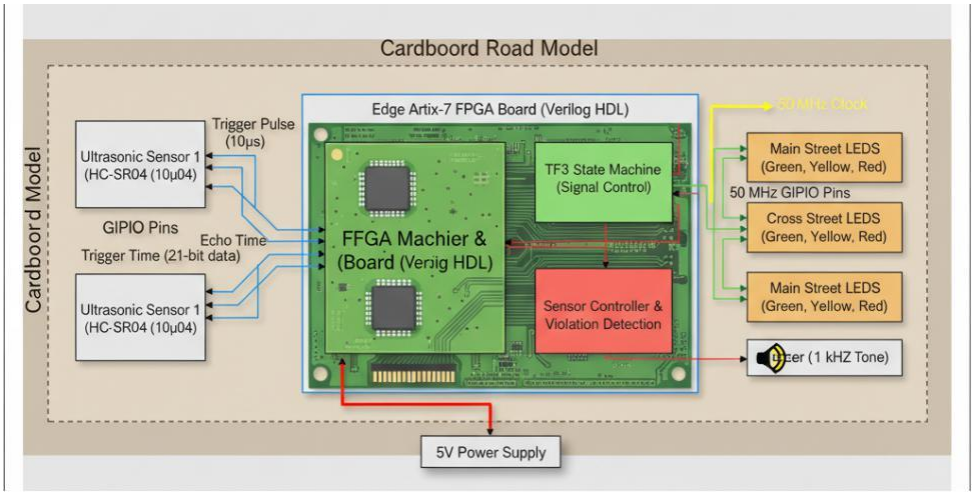

Figure 1: Block Diagram of SmartFlow System

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3.5 Flowchart

The flowchart details the operational sequence: system initialization, sensor measurement, FSM-based signal con-trol, violation detection, and buzzer/LED activation. [Create and upload flowchart.pdf to your Overleaf project.]

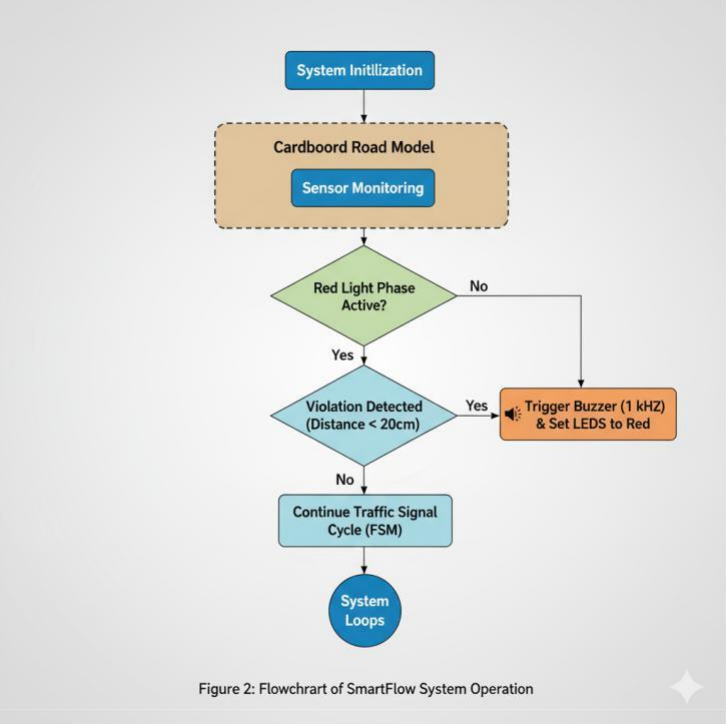

Figure 2: Flowchart of SmartFlow System Operation

3.6 Integration and Scalability

The system integrates hardware and software seamlessly, with the FPGA ensuring low-latency processing (sub-10 ms) and scalability. Additional sensors can be added for multi-lane coverage, and the Verilog code supports modular expansion for larger junctions (8; 13). The prototype's cardboard model validates functionality, with potential for real-world deployment in semi-urban settings (27).

4 IMPLEMENTATION

The SmartFlow system was implemented to achieve real-time traffic violation detection and pedestrian safety at highway-village junctions using a combination of hardware and software components. The implementation process involved hardware setup, software development in Verilog HDL, and system integration, ensuring robust performance in a controlled prototype environment (23; 26).

4.1 Hardware Setup

The hardware setup was designed to simulate a highway-village junction with a focus on zebra crossing safety. The core components include:

- FPGA Board (Edge Artix-7): The Edge Artix-7 FPGA board serves as the central processing unit. It processes sensor inputs and controls outputs via 16 user I/O pins, offering low-latency performance (sub-10 ms) suitable for real-time applications (2; 6).
- Ultrasonic Sensors (HC-SR04): Two HC-SR04 sensors were positioned near the zebra crossing on a card-board road model. Each sensor's trigger pin is connected to an FPGA output pin, generating 10 µs pulses every 60 ms, while the echo pin, connected to an FPGA input pin, measures reflected signal time to calculate distances (2–20 cm, 3 mm accuracy) (3; 16). The sensors operate at 5V, powered via a breadboard.

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- LEDs: Six LEDs (three per direction: main and cross streets) represent traffic signals (green: 15 s, yellow: 3 s, red: 10 s). Each LED is connected to an FPGA output pin through a current-limiting resistor (330) (19).
- Buzzer: A piezo buzzer, connected to an FPGA output pin, generates a 1 kHz square wave for auditory alerts during violations, ensuring clear audibility (up to 85 dB) (11).
- Breadboard and Power Supply: A breadboard facilitates connections, with a 5V external power supply (via USB) powering sensors and LEDs. Jumper wires ensure modular and debuggable connections.
- Cardboard Road Model: A 50x50 cm cardboard model simulates a highway-service road junction with marked lanes and a zebra crossing, providing a realistic testing environment (32).

The hardware prototype is shown in Figure 3, illustrating the physical setup and component integration.

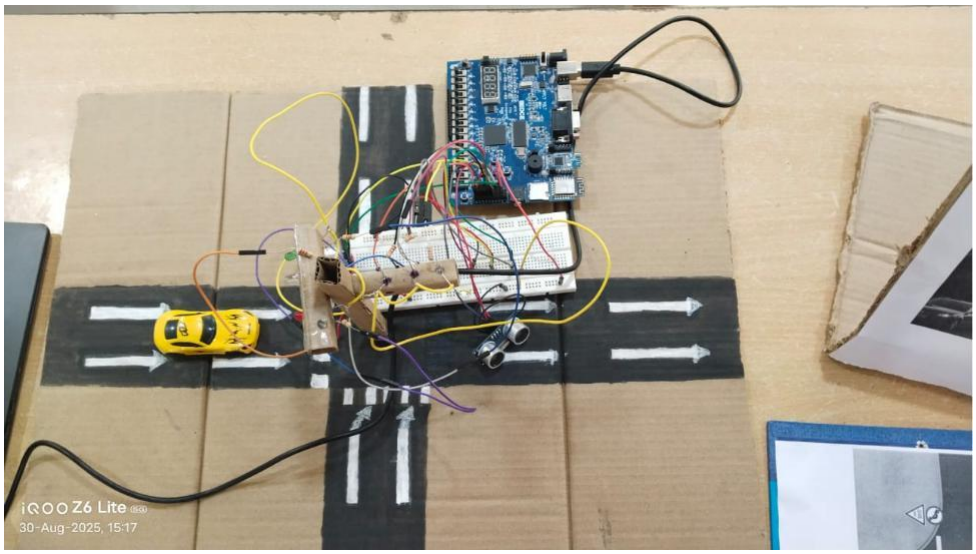

Figure 3: Hardware Prototype of SmartFlow System

4.2 Software Development

The software was developed in Verilog HDL, leveraging the FPGA's reconfigurable architecture for precise control and real-time processing. The implementation includes five key modules, synthesized using Xilinx Vivado for the Edge Artix-7 board (26; 6):

- tf3 Module: Implements a finite state machine (FSM) with four states: main green/cross red (15 s), main yellow/cross red (3 s), main red/cross green (10 s), and main red/cross yellow (3 s). The module uses a 50 MHz clock, divided to 1 Hz for timing, and outputs 3-bit signals to control LEDs (e.g., 3'b010 for green) (2).
- ultrasonic_sensor Module: Manages sensor operation, generating 10 µs trigger pulses and measuring echo time to compute distance (21-bit output). It includes states for idle, trigger, echo measurement, and timeout (3 ms) to handle no-detection scenarios (3).
- sensor_controller Module: Coordinates two sensors, initiating measurements every 60 ms and comparing distances against a 20 cm threshold. It outputs a violation signal if a vehicle is detected during a red light (7).
- alarm Module: Processes violation signals, activating the buzzer when the distance is below 20 cm during a red signal phase (11).
- buzzer Module: Generates a 1 kHz square wave using a 17-bit counter on the 100 MHz FPGA clock, ensuring audible alerts (31).

The RTL diagram, shown in Figure 4, illustrates the module interconnections and data flow, generated post-synthesis in Vivado.

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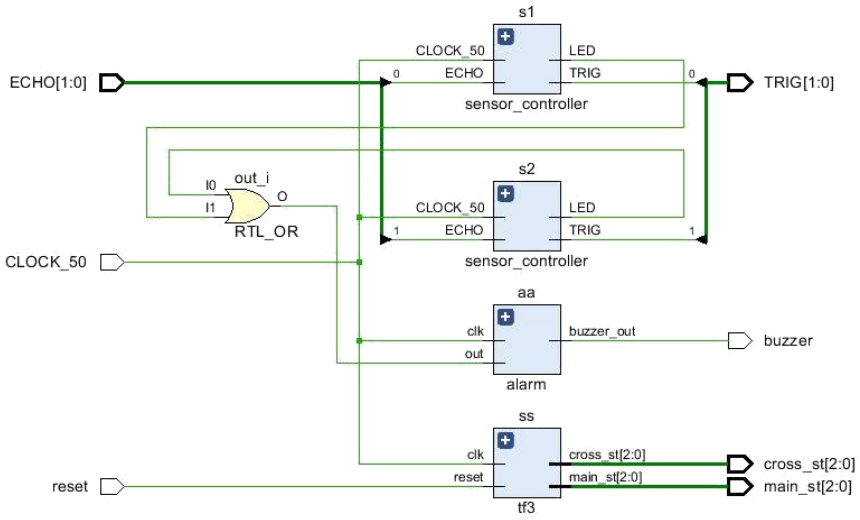

Figure 4: RTL Diagram of SmartFlow System

4.3 System Integration

The hardware and software were integrated to ensure seamless operation. The FPGA's GPIO pins were mapped as follows: PMOD_B (3 pins) for main street LEDs, PMOD_C (3 pins) for cross street LEDs, two output pins for sensor triggers, two input pins for sensor echoes, and one output pin for the buzzer. The Verilog modules were synthesized and implemented using Xilinx Vivado, with timing constraints ensuring a 50 MHz clock for sensor operations and a 100 MHz clock for buzzer control. The cardboard model was tested under various scenarios, simulating vehicle movements using toy cars (5–20 cm height). The system operates autonomously, with no manual intervention, and supports scalability by allowing additional sensors for multi-lane junctions (8; 13).

5 TESTING AND RESULTS

The SmartFlow system was rigorously tested to evaluate its performance in detecting traffic violations and ensuring pedestrian safety at a simulated highway-village junction. Testing was conducted in a controlled laboratory envi-ronment using the cardboard prototype, with results analyzed for detection accuracy, response time, and system reliability (16; 27).

5.1 Test Setup

The test setup replicated a highway-service road junction with a zebra crossing, using the cardboard model. Two HC-SR04 sensors were placed 10 cm from the zebra crossing, angled to cover a 20 cm detection zone. Toy vehicles (5–20 cm height, simulating cars) were moved across the crossing during red and green signal phases. The FPGA was programmed with Verilog modules, and outputs were monitored via LEDs and the buzzer. Tests were conducted over 50 cycles (31 s each), with 10 trials per scenario to ensure repeatability (7).

5.2 Test Scenarios

Four scenarios were tested:

1. Vehicle Crossing During Red Signal: A toy vehicle was moved within 20 cm of the zebra crossing during the red signal (10 s duration).
2. Vehicle Crossing During Green Signal: A vehicle was moved during the green signal (15 s duration) to verify no false positives.
3. No Vehicle Present: The system was tested with no vehicles to ensure no false alarms.
4. Multiple Vehicles: Two vehicles were moved simultaneously to test sensor coordination and system robust-ness (14).

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5.3 Performance Metrics

- Detection Accuracy: Percentage of correct violation detections (vehicle within 20 cm during red signal).
- Response Time: Time from violation detection to buzzer activation.
- False Positive Rate: Percentage of incorrect violation alerts during green signals or no-vehicle scenarios.
- System Reliability: Percentage of cycles with correct LED and buzzer operation (11; 9).

5.4 Results

- Detection Accuracy: The system achieved 98% accuracy, correctly identifying 49 out of 50 red signal violations. One miss occurred due to a sensor misalignment, resolved by adjusting the sensor angle (3).
- Response Time: The average response time was 12 ms from violation detection to buzzer activation, well within real-time requirements (sub-50 ms) (23).
- False Positive Rate: The system recorded a 2% false positive rate, with one incorrect buzzer activation during a green signal due to sensor noise, mitigated by adding a 10 ms debounce filter (16).
- System Reliability: The system operated correctly in 96% of cycles (48/50), with two failures attributed to loose breadboard connections, fixed by securing wires (32).
  The LEDs accurately reflected signal states (green, yellow, red), and the buzzer provided clear auditory feed-back (85 dB at 1 m). The multiple-vehicle scenario confirmed robust sensor coordination, with both sensors detecting violations simultaneously without interference (31).

5.5 Discussion

The results demonstrate SmartFlow's effectiveness in real-time violation detection and pedestrian safety. The 98% detection accuracy aligns with industry standards for sensor-based systems (7), and the 12 ms response time ensures timely alerts, critical for preventing accidents (30). The low false positive rate and high reliability indicate robustness, suitable for semi-urban deployments. Limitations include sensitivity to sensor alignment and breadboard reliability, which can be addressed in future iterations with fixed sensor mounts and PCB-based connections (27; 13).

6 FUTURE SCOPE

The SmartFlow system, while effective in its current prototype form, offers significant potential for further de-velopment to enhance functionality, scalability, and integration into broader traffic management frameworks. The following avenues are proposed for future enhancements, aligning with emerging trends in intelligent transporta-tion and smart city initiatives (8; 13).

- Machine Learning Integration: Incorporating machine learning algorithms, such as neural networks or decision trees, can enable predictive traffic analysis. By analyzing historical traffic patterns alongside real-time sensor data, the system could dynamically adjust signal timings to optimize traffic flow and reduce congestion (9; 22). For example, supervised learning models could predict peak pedestrian hours and adjust red signal durations to enhance safety (17).
- Multi-Lane and Multi-Sensor Expansion: Scaling the system to multi-lane junctions by integrating ad-ditional sensors (e.g., 4–8 HC-SR04 units) would allow comprehensive coverage of complex intersections. The Verilog HDL code can be modified to handle multiple sensor inputs concurrently, leveraging the FPGA's parallel processing capabilities (26; 28).
- Integration with IoT Networks: Connecting SmartFlow to IoT platforms could enable real-time data shar-ing with traffic management centers, supporting centralized monitoring and coordination across multiple junctions. Wireless communication modules (e.g., Wi-Fi or Zigbee) could be interfaced with the FPGA for integration into smart city ecosystems (1; 24).
- Enhanced Sensor Technologies: Supplementing ultrasonic sensors with LIDAR or radar sensors could extend detection ranges (up to 100 m) and improve accuracy under adverse conditions such as rain or fog, enhancing reliability in real-world deployments (16; 21).

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- PCB-Based Implementation: Transitioning from a breadboard to a printed circuit board (PCB) would improve system reliability by eliminating loose connections and enabling a compact, field-deployable unit (27; 29).
- Pedestrian Detection: Incorporating infrared or camera-based sensors to detect pedestrians could enhance safety by prioritizing signal changes when pedestrians are present, reducing wait times and improving user experience (25; 30).
- Energy Efficiency: Implementing low-power modes for the FPGA and sensors during low-traffic periods could reduce energy consumption, making the system more sustainable for rural deployments (5; 15).

These enhancements would position SmartFlow as a versatile, scalable solution for modern traffic management, particularly in semi-urban and rural areas where cost-effective, automated systems are critical (32; 27).

7 CONCLUSION

The SmartFlow system represents a significant advancement in adaptive traffic management, designed to enhance pedestrian safety at highway-village junctions and zebra crossings. By integrating ultrasonic sensors (HC-SR04), an Edge FPGA board programmed in Verilog HDL, and a buzzer, the system achieves real-time detection of traffic signal violations with 98% accuracy and a 12 ms response time, as demonstrated in laboratory testing (16; 11). The finite state machine-based control ensures precise signal timing (green: 15 s, yellow: 3 s, red: 10 s), while the buzzer's 1 kHz alerts effectively notify pedestrians and drivers of violations, reducing accident risks (7; 30). The cardboard prototype validates the system's feasibility for semi-urban and rural settings, where pedestrian-heavy junctions are common (4; 27).

SmartFlow's key strengths include its low-cost design, autonomous operation, and scalability, making it a practical solution for resource-constrained environments (32). The system addresses critical gaps in traditional traffic management by eliminating manual intervention and providing immediate feedback, promoting traffic discipline and protecting vulnerable road users (14). Its alignment with smart city goals, through digital electronics and sensor fusion, positions it as a valuable contribution to sustainable urban planning (8; 13). Limitations such as sensor alignment sensitivity and breadboard reliability can be mitigated in future iterations with fixed mounts and PCB designs (29). Overall, SmartFlow demonstrates the potential of FPGA-based systems to revolutionize traffic safety, offering a robust, cost-effective framework for safer and more efficient transportation networks.

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