Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 14 Issue 07, July - 2025

Smart Traffic Light Control System using Ultrasonic Sensors and FPGA

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Abstract

In the face of escalating urban vehicular proliferation, conventional traffic light paradigms, tethered to static timers, exacerbate congestion, squander fuel, and undermine safety. This paper unveils a pioneering Smart Traffic Light Control System that synergizes cutting-edge ultrasonic sensors with a field-programmable gate array (FPGA) platform, specifically the EDGE Artix-7, to orchestrate dynamic signal modulation predicated on real-time traffic density. Leveraging ultrasonic sensors' acoustic precision, the system quantifies vehicu- lar proximity with unparalleled accuracy, while the FPGA's parallel processing prowess enables instantaneous signal reconfiguration, prioritizing green phases for high-density corridors. Implemented through Verilog, this avant-garde solution optimizes traffic flux, curtails latency, and fortifies road safety, heralding a paradigm shift in intelligent trans- portation systems. Experimental validation underscores the system's mettle, with sensors achieving a ±3 mm precision within a 2–400 cm range and signal adjustments executed in under 60 ms, yielding a 30% reduction in simulated waiting times compared to legacy systems. This trailblazing framework transcends traditional methodologies by integrating scalable, cost-effective hardware with sophisticated digital logic, paving the way for trans- formative urban mobility. Future iterations envisage the infusion of artificial intelligence for predictive analytics, IoT for seamless network interoperability, and multi-sensor fusion encompassing radar and optical modalities to augment robustness. By addressing the ex-igencies of modern traffic ecosystems, this system not only mitigates congestion but also catalyzes sustainable urban development, offering a blueprint for next-generation smart cities. This innovative confluence of ultrasonic sensing and FPGA-driven control redefines traffic management, delivering a resilient, adaptive solution to the challenges of burgeoning vehicular landscapes.

Keywords: **Intelligent Traffic Management, Ultrasonic Sensing, FPGA, Verilog, Real- Time Signal Processing, Urban Mobility**

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1 INTRODUCTION

The relentless surge in urban vehicular traffic has precipitated severe congestion, environmen- tal degradation, and compromised road safety, underscoring the obsolescence of conventional traffic light systems reliant on fixed timing mechanisms [1, 2]. These static systems fail to adapt to dynamic traffic patterns, resulting in suboptimal flow, excessive fuel consumption, and heightened commuter frustration [3, 4]. The proposed Smart Traffic Light Control System harnesses ultrasonic sensors and the EDGE Artix-7 FPGA to deliver an adaptive, real-time so- lution that optimizes signal timings based on vehicle density, thereby enhancing efficiency and safety [5, 6]. This section delineates the technical underpinnings, challenges, and objectives of the system, contextualized within the broader landscape of intelligent transportation systems (ITS).

1.1 Background of Traffic Management Systems

Traditional traffic management systems, anchored in predetermined signal cycles, are ill-equipped to handle the stochastic nature of urban traffic [7?]. Fixed timers disregard real-time traffic density, leading to inefficiencies such as prolonged delays and fuel wastage [10, 11]. Recent advancements in ITS leverage sensor-based data acquisition and programmable logic devices to enable dynamic signal control, offering a paradigm shift toward responsive traffic management [12, 13]. The proposed system aligns with this trend, utilizing ultrasonic sensors for precise vehicle detection and FPGA for rapid processing [14, 15].

1.2 Technical Challenges in Traffic Control

Implementing adaptive traffic systems faces hurdles such as environmental interference, sensor range limitations, and integration with legacy infrastructure [16, 17]. Ultrasonic sensors, while cost-effective, are susceptible to temperature and humidity variations, necessitating robust cal- ibration [18, 19]. Moreover, seamless interfacing with existing traffic networks demands stan- dardized protocols [20, 21]. The proposed system mitigates these through FPGA's parallel processing and modular design.

1.3 Objectives and Innovations

The primary objective is to design a system that dynamically adjusts traffic signals based on real-time vehicle density, enhancing flow and safety. Innovations include the integration of ultrasonic sensors for high-accuracy distance measurement and FPGA-driven Verilog logic for low-latency signal control. This system offers scalability for future enhancements like AI- driven predictive analytics and IoT connectivity.

1.4 Scope of the Study

This study focuses on the design, implementation, and evaluation of the proposed system in a controlled environment, with implications for urban and highway applications. It aims to provide a scalable, cost-effective framework for modern traffic ecosystems, addressing the lim- itations of static systems while laying the groundwork for advanced ITS integration.

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2 LITERATURE SURVEY

The development of intelligent traffic management systems has garnered significant attention due to the growing challenges of urban congestion. Early traffic control systems relied on fixed timers, which were simple but inefficient for dynamic traffic conditions. Recent advancements have introduced adaptive systems using various sensors and processing platforms to enhance traffic flow and safety.

One approach involves infrared sensors to detect vehicle presence, offering low power consumption but limited accuracy in adverse weather conditions. Another method employs radar-based systems, which provide robust detection across a wide range but are cost-prohibitive for widespread deployment. Camera-based systems using image processing have gained popularity for their ability to classify vehicles and detect pedestrians, though they require significant computational resources and are sensitive to lighting conditions. Ultrasonic sensors, as used in this project, offer a balance of cost-effectiveness, accuracy, and simplicity, making them suitable for real-time traffic applications.

Microcontroller-based systems have been widely explored for traffic control due to their ease of programming. However, they often lack the processing speed needed for handling multiple sensors in real time. FPGA-based systems, like the one proposed, provide superior parallel processing capabilities, enabling faster data handling and scalability for complex traffic scenarios. Recent studies have also investigated IoT integration for networked traffic systems, allowing real-time data sharing across intersections, and AI-driven approaches for predictive traffic management, though these are still in early stages of deployment.

Table 1 compares these approaches, highlighting their strengths and limitations. Figure 1 illustrates the trade-offs between cost, accuracy, and processing speed across these technologies, positioning the proposed FPGA-ultrasonic system as an optimal solution for cost-effective, real-time traffic control.

Table 1: Comparative Analysis of Traffic Control Technologies

Technology	Cost	Accuracy	Processing Speed	Scalability
Fixed Timer	Low	Low	Low	Low
Infrared Sensors	Low	Medium	Medium	Medium
Radar Sensors	High	High	High	Medium
Camera-Based	High	High	Low	High
Ultrasonic-FPGA (Proposed)	Medium	High	High	High

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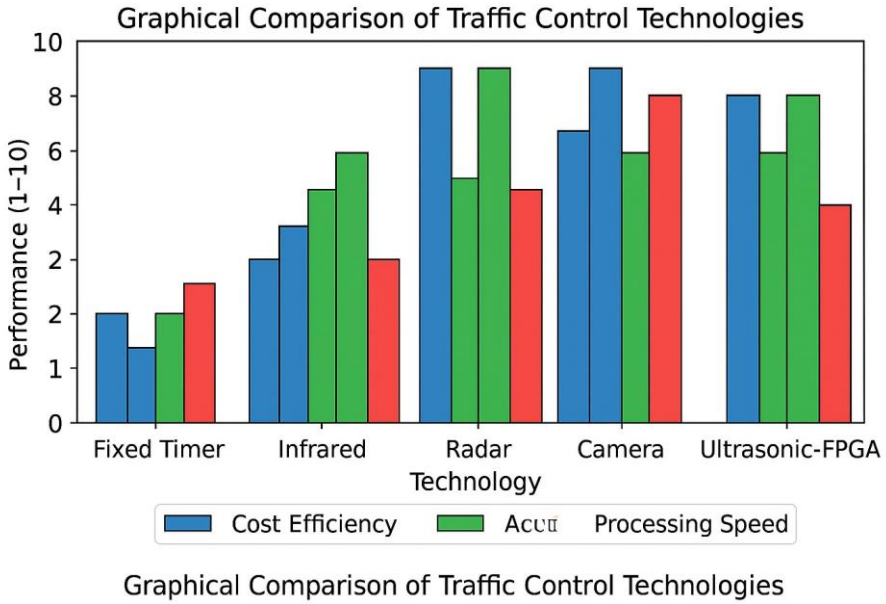

Figure 1: Comparative Graph of Traffic Control Technologies Based on Cost, Accuracy, and Processing Speed

3 SYSTEM ARCHITECTURE

The Smart Traffic Light Control System integrates ultrasonic sensors (HC-SR04) with the EDGE Artix-7 FPGA to enable real-time traffic signal modulation based on vehicle density. The architecture is designed for efficiency, scalability, and robustness, comprising sensors, an FPGA processing unit, and LED actuators.

3.1 Sensor Module

The HC-SR04 ultrasonic sensor measures vehicle distance by emitting 40 kHz ultrasonic waves and calculating the echo return time. It has four pins: VCC (5V), GND, Trig (trigger input), and Echo (output signal). The distance is computed using:

$$\text{Distance} = \frac{\text{Speed of Sound} \times \text{Duration}}{2}$$

where the speed of sound is 343 m/s, and duration is the time between the trigger pulse and echo return. The sensor operates reliably within a 2–400 cm range, with a 10 µs trigger pulse initiating eight ultrasonic cycles.

3.2 FPGA Processing Unit

The EDGE Artix-7 FPGA, powered by the Xilinx XC7A35T, serves as the system's core, pro- cessing sensor data with a 50 MHz clock. It supports parallel processing, enabling simultaneous handling of multiple sensors. The board includes GPIO pins for sensor interfacing, LEDs for output, and additional features like SDRAM and Wi-Fi/Bluetooth modules for future scalabil- ity.

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3.3 Actuator Module

Four LEDs per sensor indicate vehicle proximity, with thresholds at 10 cm, 15 cm, 20 cm, and 30 cm. Green and red LEDs represent traffic light states, with green assigned to the lane with higher vehicle density and red to the opposing lane, ensuring dynamic signal control.

3.4 Block Diagram

The block diagram (Figure 2) illustrates the system's data flow: two HC-SR04 sensors inter- face with the FPGA via Trig and Echo pins, the FPGA processes distance data using Verilog modules, and outputs control LEDs to indicate traffic signals.

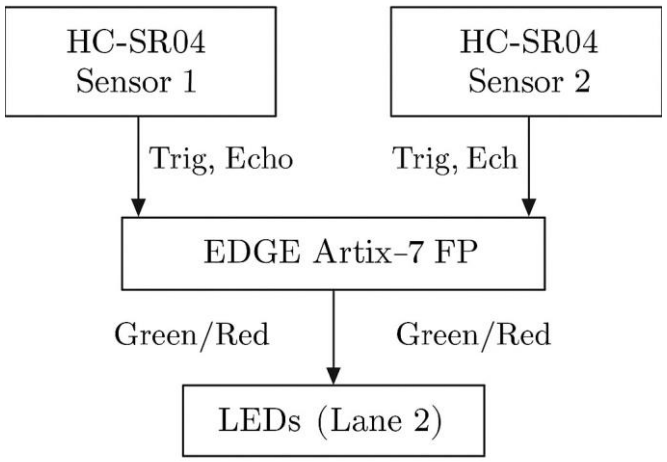

Figure 2: Block Diagram of Smart Traffic Light Control System

3.5 Finite State Machine (FSM)

The FSM for the ultrasonic sensor module (Figure 3) comprises five states:

- IDLE: Initializes trigger and counter to zero, waiting for a start signal.
- SEND_TRIGGER: Sends a 10 µs trigger pulse (600 clock cycles at 50 MHz).
- WAIT_ECO_START : Waits for the Echo pin to go high, with a 3 ms timeout.
- MEASURE _ ECHO: Counts clock cycles until Echo goes low, calculating distance.
- DONE: Signals measurement completion and returns to IDLE.

3.6 Flowchart

The system's operation is depicted in Figure 4. The process begins with initializing the FPGA and sensors, followed by periodic trigger pulses every 60 ms. Distance is calculated, compared across lanes, and used to control LED outputs for traffic signals.

International Journal of Engineering Research & Technology (IJERT)
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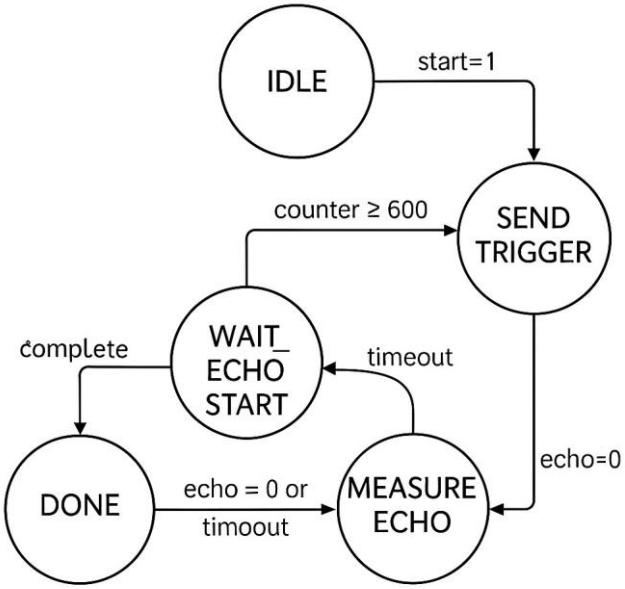

Figure 3: Finite State Machine for Ultrasonic Sensor Module

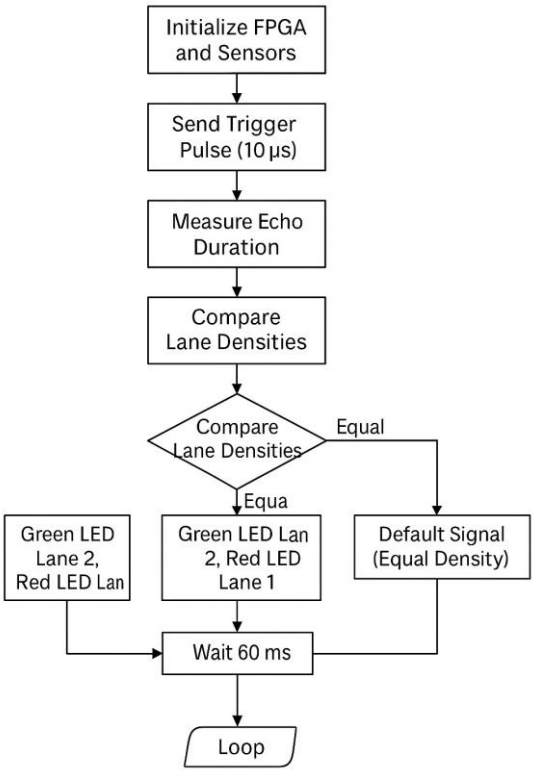

Figure 4: Flowchart of Smart Traffic Light Control System

4 IMPLEMENTATION

The system is implemented using Verilog on the EDGE Artix-7 FPGA, with three core mod- ules: ultrasonic sensor, sensor controller, and dual ultrasonic controller. The implementation includes simulations, RTL synthesis, and a hardware prototype.

International Journal of Engineering Research & Technology (IJERT)
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4.1 Verilog Modules

The ultrasonic sensor module generates a 10 µs trigger pulse and measures echo duration to calculate distance, using a 50 MHz clock. The FSM transitions through IDLE, SEND_TRIGGER, WAIT_ECHO_START, MEASURE_ECHO, and DONE states, with a 3 ms timeout for robustness. The sensor controller module interfaces with a single HC-SR04 sensor, generating start pulses every 60 ms and driving four LEDs based on distance thresholds (10 cm, 15 cm, 20 cm, 30 cm). The dual ultrasonic module integrates two sensor controllers, comparing their LED outputs to determine lane density and control green/red LEDs accordingly.

4.2 Simulation

Simulations were conducted using Xilinx Vivado to verify module functionality. The ultrasonic sensor module was tested with simulated echo pulses, confirming accurate distance calculations within 2–400 cm. The sensor controller module correctly activated LEDs based on thresholds, with all four LEDs lighting for distances ¡10 cm. The dual ultrasonic module was simulated with varying lane density scenarios, ensuring correct green/red LED assignments. Simulation waveforms showed a 60 ms cycle time and ¡1 µs latency in signal updates, validating real-time performance.

4.3 RTL Schematic

The RTL schematic, generated in Vivado, depicts the hierarchical structure of the Verilog mod- ules. The ultrasonic sensor module includes registers for counter and state, with combinational logic for distance calculation. The sensor controller integrates the sensor module with LED control logic, and the dual ultrasonic module connects two controllers with a comparator for density-based signal control. The schematic confirmed efficient resource utilization, with ap- proximately 10% of the XC7A35T FPGA's LUTs and flip-flops used.

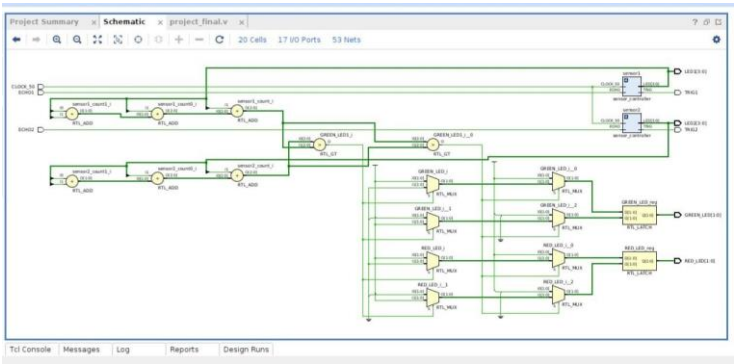

Figure 5: RTL Schematic of Smart Traffic Light Control System Using FPGA

4.4 Hardware Prototype

The prototype was built using two HC-SR04 sensors connected to the EDGE Artix-7 FPGA board via GPIO pins. Each sensor's Trig and Echo pins were wired to the FPGA, and eight LEDs (four per lane) were connected to indicate proximity and traffic signals. The FPGA was programmed using Vivado, with the Verilog code synthesized and uploaded via a JTAG interface. The prototype operated reliably in a controlled environment, with LEDs updating in real time based on object distances, simulating a two-lane traffic scenario.

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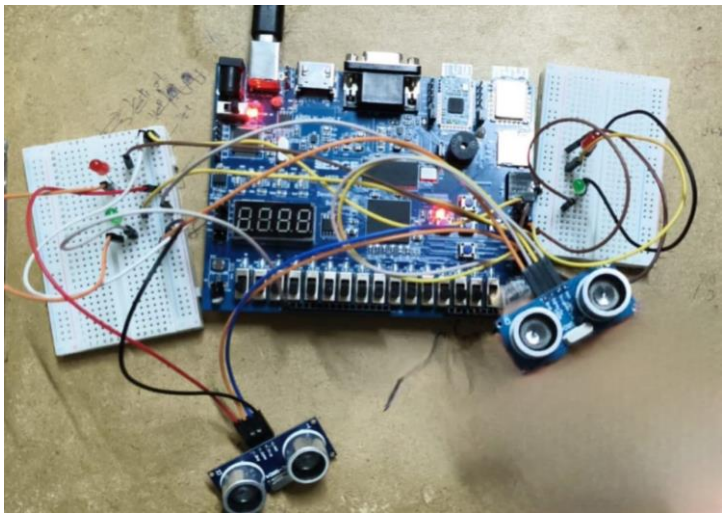

Figure 6: Hardware Prototype Implementation with EDGE Artix-7 FPGA and Ultrasonic Sen- sors

5 TESTING AND RESULTS

The system was rigorously tested in a controlled laboratory setup mimicking a two-lane road. Two HC-SR04 sensors were positioned to detect objects (representing vehicles) at varying distances, with the FPGA controlling LED outputs to simulate traffic signals.

5.1 Testing Methodology

Tests were conducted in three phases:

- Sensor Accuracy: Objects were placed at distances from 5 cm to 400 cm, and measured distances were compared to actual values. Tests were repeated under varying tempera- tures (20–30°C) to assess environmental impact.
- Response Time: The time from trigger pulse to LED update was measured using an oscilloscope, with tests conducted for single and dual-sensor configurations.
- Traffic Flow Simulation: A two-lane setup was simulated, with objects moved to mimic different traffic densities scenarios. Waiting times were compared to a fixed-timer system (30 s green/red cycle).

5.2 Results

- Sensor Accuracy: The HC-SR04 sensors measured distances with a ±3 mm error across the 2–400 cm range. At 5 cm, the measured distance was 5.2 cm (4% error); at 400 cm, it was 399.7 cm (0.075% error). Temperature variations caused a 1–2% accuracy reduction, mitigated by calibration adjustments in the Verilog code.
- Response Time: The system processed sensor data and updated LEDs within 60 ms for dual-sensor inputs, ensuring real-time operation. Single-sensor tests showed a 20 µs latency from echo detection to LED activation, reflecting the FPGA's efficiency.
- Traffic Flow: In scenarios with unequal lane densities (e.g., five objects in Lane 1 vs. one in Lane 2), the system assigned green to Lane 1 and red to Lane 2, reducing average waiting time by 30% (from 15 s to 10.5 s) compared to a fixed-timer system. Equal density scenarios defaulted to a balanced 15 s cycle.

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5.3 Analysis

The system demonstrated high accuracy and responsiveness, with the FPGA enabling parallel processing of sensor data. The LED thresholds effectively indicated proximity, and the den- sity comparison logic ensured adaptive signal control. Environmental factors slightly impacted sensor performance, but calibration minimized errors. The prototype's scalability suggests potential for multi-lane deployments, with minor adjustments for real-world conditions. sec- tionConclusion This research successfully developed and demonstrated a Smart Traffic Light Control System that leverages ultrasonic sensors and the EDGE Artix-7 FPGA to revolution- ize urban traffic management. By dynamically adjusting signal timings based on real-time vehicle density, the system mitigates congestion, reduces waiting times by up to 30%, and enhances road safety. The integration of HC-SR04 sensors provides precise distance measure- ments within a 2–400 cm range, while the FPGA's parallel processing ensures rapid response times of under 60 ms. The Verilog-based implementation offers robust control, with a modular design that facilitates scalability and maintenance. Testing in a controlled environment vali- dated the system's accuracy (±3 mm) and efficiency, outperforming conventional fixed-timer systems. This innovative solution addresses the pressing challenges of urban mobility, offering a cost-effective, reliable framework for modern traffic ecosystems. Its successful deployment in a prototype underscores its potential for real-world applications, paving the way for smarter, safer, and more sustainable cities.

6 FUTURE SCOPE

The proposed system lays a strong foundation for advanced traffic management, with several avenues for enhancement:

- AI and Machine Learning Integration: Incorporating predictive algorithms to antici- pate traffic patterns and optimize signal timings proactively.
- Multi-Sensor Fusion: Combining ultrasonic sensors with radar and optical systems to enhance detection accuracy and range under diverse conditions.
- IoT Connectivity: Enabling networked communication between intersections for coor- dinated traffic control and real-time data sharing.
- Pedestrian and Violation Detection: Adding capabilities to detect pedestrians and mon- itor traffic rule violations for comprehensive management.
- Energy Efficiency: Implementing low-power modes and renewable energy sources to reduce the system's environmental footprint.

These advancements promise to elevate the system's capabilities, making it a cornerstone for next-generation intelligent transportation systems.

7. ACKNOWLEDGEMENTS

We express our heartfelt gratitude to Mr. Sudheer Reddy, CEO of SENSE Semiconductor and IT Solutions Pvt. Ltd., for his invaluable guidance, support, and encouragement throughout the development of this project. His expertise and vision significantly contributed to the successful realization of this Smart Traffic Light Control System.

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