Simultaneous power and aging optimization based on dynamic supply voltage assignment

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Abstract -As technology scales, negative bias temperature instability (NBTI) has become a major reliability for circuit designers. Reducing power consumption is one of the design goals. In this paper a variation supply voltage assignment technique (SVA) combining dual voltage assignment and dynamic voltage scaling is provide a geometric platform, to perform minimize circuit power below an aging responsive timing limitation. Our technique can moderate on average 62% of the NBTI-Induced circuit delay degradation. So, our approach saves more energy.

Keywords—Dynamic power, leakage power, negative bias temperature instability (NBTI), supply voltage assignment (SVA).

1. INTRODUCTION

With the continuous scaling of CMOS technology, negative bias temperature instability (NBTI) is raising as one of the major dependability degradation mechanisms. NBTI is an aging effect which regularly increases the threshold voltage (V_{th}) of pMOS transistors when they are negatively biased, thus increasing the gate delay. In the meantime leakage power has become a large portion of the total power consumption. Furthermore, the growing process and device variations are rising as key influencing factors of circuit performance. Conventional worst-case design will show the way to an over-pessimistic estimation.

As an alternative, statistical static timing analysis (SSTA) is an efficient technique to evaluate the increasing variations as a substitute of the conventional STA .Researchers have explored many techniques to moderate NBTI-induced degradation, such as NBTI-aware combination , gate and transistor sizing , input vector control (IVC) , internal node control (INC) .These techniques are all "one-time" permanent solutions, which give the circuits a high guard-band power, leading to large positive slacks during the initial time, therefore result in large area and power overhead .

In this paper we attempt to develop a new technique which can moderate NBTI-induced degradation and reduce power simultaneously. usual power reduction techniques, such as dual v_{dd} or dual v_{th} , reduce power by the give up of some positive slacks, thus show the way to the increase of the number of critical paths, and make the performance of critical paths degrades. We use dual v_{dd} and dynamic v_{dd} scaling, which increases the voltage of critical paths to make certain their performance, and decreases the voltage of non-critical paths to reduce power. Since the partition of dual v_{dd} islands and the scaling method have large impact on both circuit

performance and power, consistency and power should be at the same time considered when partitioning the dual v_{dd} islands and scaling the voltage values. The involvement of this paper can be summarized as follows.

• We propose a variation-aware SVA technique combining dual v_{dd} assignment and dynamic v_{dd} scaling. The high v_{dd} is used to Compensate for NBTI-induced degradation; while the low v_{dd} is used to reduce power. During circuit operation, the optimal v_{dd} values are dynamically determined according to the aging-aware timing limitation.

• The experimental results show that our approach can moderate on average 62% of NBTI induced degradation. Compared with guard-banding v_{dd} and single scaling approach, our method can effectively save the energy.

2. MODEL REVIEW

A. Gate delay model

Gate delay model is used to represent the Supply Voltage Assignment

i. Dual V_{dd} Assignment.
ii. Dynamic V_{dd} Scaling.

(i) Dual V_{dd} Assignment

Divide all the gates into two sets: HVGS (high gate set) and LVGS (low gate set). If the slack of gate i S(i) is smaller than a given threshold value (V_{th}) then gate i is called "NBTI-aware critical gate". All the NBTI-aware critical gates are included in HVGS.

(ii)Dynamic V_{dd} Scaling

A multiple way Scaling is applied to further refine the supply voltage assignment of gates to reduce the total power consumption. Since the statistical platform is used, delay upper bound (upper bound: μ + 3б, μ is the mean value, and б is the standard deviation) is used instead of the absolute delay.

The timing constraint is chosen as the nominal delay upper bound at a given time node of each circuit. Once the circuit delay upper bound exceeds the constraint, the voltages need to be scaled. This means the circuit delay upper bound will never exceed the constraint.

- Dynamically determine the optimal time nodes and the voltage values.
- A multiple supply voltage scaling techniques for low power designs.
- It simultaneously scales down as many gates as possible to lower supply voltages.

B. NBTI Model for V_{TH} Degradation:

However in order to estimate the performance degradation of a circuit, the NBTL model should handle multiple cycles of the stress and recovery phases. Therefore, a multicycle analytical model should be used. An analytical model to handle multicycle Ac stress condition and creation of interface traps after N cycle of Ac stress can be evaluated by a recursion formula.

The interface traps can be expressed,

$$Nit[n+1)\tau] = \frac{\beta}{\beta+1} + \frac{Nit}{1+\beta}[c + (\frac{Nit(n\tau)}{Nit})^4]^4$$

C. Power model

They are used two techniques:

i. Adaptive body biasing
ii. Adaptive supply voltage

- They adjusted the supply/bias voltage to recover the circuit performance.
- The inputs are input of NBTI model. The output fed to ABB technique and ASV technique.
- These two outputs given to power analysis.

- ABB and ASV increase the leakage by 23% on average.

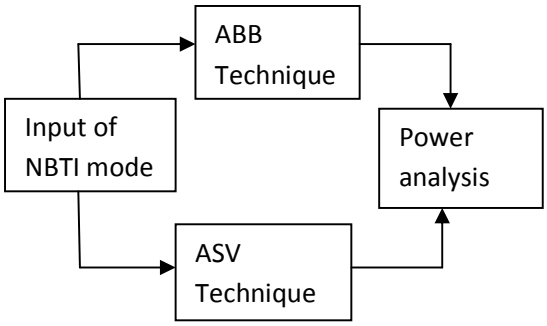

Fig .5(a): Power delay model

Dynamic power is calculated as follows:

$$P_{dyn} = \frac{1}{2} f \sum_{v=1}^{N} \propto_v C_v V_{dd}^2 \qquad (5.1)$$

Where,

$\propto_v$ --------- Switching probability of gate v,

F ---------clock frequency,

N ---------Gate number in the circuit.

A leakage lookup table is created by simulating all the gates in the standard cell library, under all possible input patterns. Thus the leakage power of gate v can be expressed as

$$P_{1kg}^{(v)} = \sum_{input} P1kg(v, input) \times prob(v, input) \qquad (5.2)$$

Where,

p1kg ---------- leakage power and v, input --------- Input signal probability of gate v when the input pattern is input .

D. Variation model

Many variations strongly affect the gate delay, such as threshold voltage V_{th}, channel length L_{eff}, oxide thickness T_{ox}, and so on. Since gate delay and leakage power both strongly depends on the threshold voltage. Dual V_{dd}, the high V_{dd} is used to compensate for NBTI-induced degradation on critical gates, while the low V_{dd} is used to reduce power on other gates. Our target is to reduce power as much as possible under an aging-aware timing constraint.

In guard-banding approach, a fixed supply voltage is set to each circuit, to ensure that the circuit delay upper bound will never exceed the constraint. Since NBTI effect degrades the circuit continuously, the circuit delay at T_{life} should be guaranteed. The results of guard-banding method are shown in the three sub-columns in "Guard-banding" column. Guard-banding approach increases 38% of the average leakage power and 17% of the average dynamic power, to guarantee the timing constraint. A gate delay and leakage power both strongly depend on the threshold voltage.

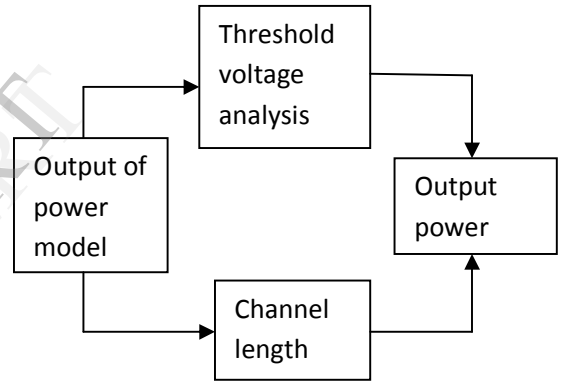

Fig 6.1: Variation model

3.**S**UPPLY **V**OLTAGE **A**SSIGNMENT (SVA) **T**ECHNIQUE

Based on the NBTI model, gate V_{th} will increase and then results in degradation in circuit speed. To counteract the degradation, V_{dd} must gradually increase. However, increasing V_{dd} will directly increase leakage. We notice that it is not necessary to increase all gates' V_{dd}, because non-critical gates have delay slack. So instead of using one scaling supply voltage, we propose to use dual V_{dd}, the high V_{dd} is used to compensate for NBTI degradation on critical gates, while low

V_{dd} is used to reduce leakage power on other gates who do not affect the circuit delay. Furthermore, In our technique, all the protection parameters are dynamically calculated according, to the circuit performance constraints

There are two steps in our technique

A. Dual V_{dd} assignment:

Divide all the gates into two sets:

i. HVS (high V_{dd} set) and

ii. LVS (low V_{dd} set);

B. Dynamic V_{dd} Scaling

A. Dual V_{dd} assignment

In the beginning, the nominal delay and leakage power at time 0 are calculated. Then we determine two gate sets: HVS (high V_{dd} set) and LVS (low V_{dd} set). Since a low V_{dd} gate cannot directly drive a high V_{dd} gate, a level converter should be used. In order to avoid level converters, HVS includes all the critical gates and all the predecessors of critical gates; LVS is composed of all the rest gates who do not directly affect the circuit delay. Generally speaking, HVS is larger than LVS for most circuits. Based on the proportion between HVS and LVS of each circuit, we can approximately estimate the potential of NBTI-induced degradation mitigation and leakage reduction by our technique.

B. Dynamic V_{dd} scaling

In our technique, we set a delay specification for each circuit, which is chosen as the delay value of each circuit when t=10 days. At time 0, we first calculate mean value and standard deviation of delay and leakage, then determine the optimal V_{ddhigh}(t1) and V_{ddlow}(t1) which will be assigned in the following time interval [t0, t1]. The HVS gates are assigned V_{ddhigh} while LVS gates are assigned V_{ddlow}.

The detailed determination of Vddhigh and Vddlow will be described in the below. With new V_{ddhigh}(t1) and V_{ddlow}(t1), we can estimate V_{th} degradation of each gate at later time as same as the method and then predict the next time node t1 at which the circuit delay will exceed the specification and we need to scale supply voltages again. The same procedure including three operations: determine optimal V_{ddhigh} (ti+1), V_{ddlow} (ti+1) and predict the next time node ti+1, will be repeated at each time node ti, until circuit lifetime ends.

4.**O**PTIMIZATION **T**ECHNIQUE

A. Precomputation-based optimization for low power:

A sequential circuit optimization technique which precomputed the output logic values of the circuit one clock cycle before they are required. The precomputed logic values are used in the following clock cycle to reduce the switching activity at the internal nodes of a circuit. However certain class of the circuits, the precomputation scheme can save significant power.

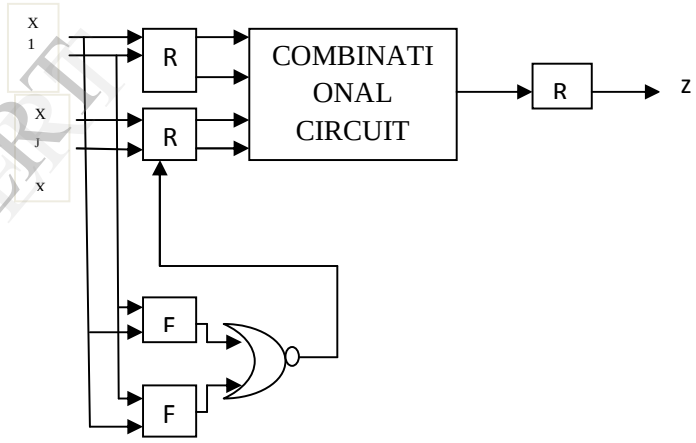

Fig. 4(a): Percomputation architecture.

The precomputation architecture is shown. The block comb represents a combinational logic fed by registers R1 and R2 and has one output as shown in fig.A set of input x1 through xm are fed to register R1, while set of input xj through xn are fed to register R1 are also fed to logic block

marked f1 and f2, which are predictor functions given by the following relation.

f1=1=>z=1

f2=1=>z=0

It can be observed that f1 and f2 will never simultaneously evaluate to logic 1.therefore, during clock cycle t, if either f1 or f2 evaluates to 1, then the load enable line of register R2 is turned off and hence, the output of register R2 during clock cycle t+1 do not change. However, the output of register R1 change and, hence, Z evaluate to the correct logic value. It can be noted that only a subset of the input values to the combinational logic is changing. Therefore, the switching activities at the internal nodes of combinational circuits are minimized. However, depending on the complexity,the logic functions f1 and f2, the switching activity at the internal nodes of f1 and f2 can be significant. Hence, for the precomputation scheme to work effectively, the set of input fed to register R2 shoud be large, while the complexity of the logic blocks f1 and f2 should be small. One would also like to have signal probability of (f1+f2). ie).,p(f1)+p(f2)-p(f1)p(f2), to be large for the scheme to work effectively. In the function saving function and reduce switching activity.

5.**E**XPECTED **R**ESULTS

Using precomputation based optimization for low power techniques to reduce switching activity and power consumption. So it can be 80% power saving and single scan cycle access.

6.**C**ONCLUSION

Power and reliability have become two key design goals with technology scales. In this paper, a SVA technique combining dual assignment and dynamic v_{dd} scaling is proposed on a statically platform, to minimize NBTI-induced performance degradation and circuit power consumption. It saves 62% of the NBTI-induced circuit delay degradation. So we develop from the SVA combining precomputation based optimization for low power technique. In this technique provide reducing switching activity and peak power consumption. And also high speed single scan cycle access.

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